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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	·
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	13
Program Memory Size	3.5КВ (2К х 14)
Program Memory Type	OTP
EEPROM Size	
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c622-04i-ss

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

NOTES:

### 4.2.2.3 INTCON Register

The INTCON register is a readable and writable register, which contains the various enable and flag bits for all interrupt sources except the comparator module. See Section 4.2.2.4 and Section 4.2.2.5 for a description of the comparator enable and flag bits.

**Note:** Interrupt flag bits get set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>).

	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF
	bit 7			<u>.</u>		<u>.</u>		bit 0
bit 7	GIE: Globa	I Interrupt E	nable bit					
	1 = Enables	s all un-mas	sked interrup	ots				
1.11.0		s all interru	pts					
0 110	PEIE: Perip		upt Enable i	DIT 	-			
	1 = Enables 0 = Disable	s all un-mas	sked periphe eral interrun	eral interrupt	S			
bit 5		0 Overflow	Interrunt En	able bit				
bit o	1 = Enables	s the TMR0	interrupt					
	0 = Disable	s the TMR	) interrupt					
bit 4	bit 4 INTE: RB0/INT External Interrupt Enable bit							
	1 = Enables	s the RB0/I	NT external	interrupt				
	0 = Disable	s the RB0/I	NT external	interrupt				
bit 3	RBIE: RB F	ort Change	Interrupt E	nable bit				
	1 = Enables	s the RB po	rt change in	iterrupt				
L:4 0			oft change in	iterrupi				
DIL ∠		J OVernow i		g Dit	- ared in coff	+		
	1 = TMR0 r 0 = TMR0 r	register did	not overflow	(ที่มีประ มีฮ มีฮ /	aleu ili son	ware		
bit 1	INTF: RB0/	INT Externa	al Interrupt F	-lag bit				
	1 = The RB	30/INT exter	nal interrup	t occurred (n	nust be clea	ared in softw	are)	
	0 = The RB	30/INT exter	nal interrupt	t did not occ	ur			
bit 0	<b>RBIF</b> : RB F	ort Change	Interrupt Fl	lag bit				
	1 = When a	at least one	of the RB<7	':4> pins cha	anged state	(must be cle	ared in soft	ware)
	0 = None o	f the RB<1	4> pins nave	e changea s	tate			
	Larandi							
	Legend:							

REGISTER 4-3:	INTCON REGISTER (ADDRESS 0BH OR 8BH)	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented	bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

### 6.0 TIMER0 MODULE

The Timer0 module timer/counter has the following features:

- 8-bit timer/counter
- · Readable and writable
- 8-bit software programmable prescaler
- · Internal or external clock select
- · Interrupt on overflow from FFh to 00h
- · Edge select for external clock

Figure 6-1 is a simplified block diagram of the Timer0 module.

Timer mode is selected by clearing the T0CS bit (OPTION<5>). In Timer mode, the TMR0 will increment every instruction cycle (without prescaler). If Timer0 is written, the increment is inhibited for the following two cycles (Figure 6-2 and Figure 6-3). The user can work around this by writing an adjusted value to TMR0.

Counter mode is selected by setting the T0CS bit. In this mode, Timer0 will increment either on every rising or falling edge of pin RA4/T0CKI. The incrementing edge is determined by the source edge (T0SE) control bit (OPTION<4>). Clearing the T0SE bit selects the rising edge. Restrictions on the external clock input are discussed in detail in Section 6.2.

The prescaler is shared between the Timer0 module and the Watchdog Timer. The prescaler assignment is controlled in software by the control bit PSA (OPTION<3>). Clearing the PSA bit will assign the prescaler to Timer0. The prescaler is not readable or writable. When the prescaler is assigned to the Timer0 module, prescale value of 1:2, 1:4, ..., 1:256 are selectable. Section 6.3 details the operation of the prescaler.

### 6.1 TIMER0 Interrupt

Timer0 interrupt is generated when the TMR0 register timer/counter overflows from FFh to 00h. This overflow sets the T0IF bit. The interrupt can be masked by clearing the T0IE bit (INTCON<5>). The T0IF bit (INTCON<2>) must be cleared in software by the Timer0 module interrupt service routine before reenabling this interrupt. The Timer0 interrupt cannot wake the processor from SLEEP, since the timer is shut off during SLEEP. See Figure 6-4 for Timer0 interrupt timing.



### FIGURE 6-2: TIMER0 (TMR0) TIMING: INTERNAL CLOCK/NO PRESCALER

Counter)	( PC-1	X PC	( PC+1 )	PC+2	PC+3	PC+4	<u>PC+5</u> χ	PC+6
Instruction Fetch	1 1 1	MOVWF TMR	0MOVF TMR0,V	MOVF TMR0,V	MOVF TMR0,W	MOVF TMR0,V	MOVF TMR0,W	I
TMR0	T0 X	T0+1 )	T0+2	I	NT0		NT0+1 \	NT0+2 \
Instruction	1 1 1	1 1 1	<b>≜</b>	<b>≜</b>	1	<b>≜</b>	<b>↑</b>	<b>≜</b>
Executed	1	1	Write TMR0	Read TMR0	Read TMR0	Read TMR0	Read TMR0	Read TMR0

### 6.3 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module, or as a postscaler for the Watchdog Timer, respectively (Figure 6-6). For simplicity, this counter is being referred to as "prescaler" throughout this data sheet. Note that there is only one prescaler available which is mutually exclusive between the Timer0 module and the Watchdog Timer. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the Watchdog Timer and vice-versa.

The PSA and PS<2:0> bits (OPTION<3:0>) determine the prescaler assignment and prescale ratio.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., CLRF 1, MOVWF 1, BSF 1, x....etc.) will clear the prescaler. When assigned to WDT, a CLRWDT instruction will clear the prescaler along with the Watchdog Timer. The prescaler is not readable or writable.



### FIGURE 6-6: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER

NOTES:

## 7.0 COMPARATOR MODULE

The comparator module contains two analog comparators. The inputs to the comparators are multiplexed with the RA0 through RA3 pins. The On-Chip Voltage Reference (Section 8.0) can also be an input to the comparators.

The CMCON register, shown in Register 7-1, controls the comparator input and output multiplexers. A block diagram of the comparator is shown in Figure 7-1.

### REGISTER 7-1: CMCON REGISTER (ADDRESS 1Fh)

	R-0	R-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0			
	C2OUT	C10UT	—	—	CIS	CM2	CM1	CM0			
	bit 7							bit 0			
bit 7	<b>C2OUT</b> : Comparator 2 output 1 = C2 VIN+ > C2 VIN- 0 = C2 VIN+ < C2 VIN-										
bit 6	<b>C1OUT</b> : Comparator 1 output 1 = C1 VIN+ > C1 VIN- 0 = C1 VIN+ < C1 VIN-										
bit 5-4	Unimplem	ented: Read	d as '0'								
bit 3	CIS: Comparator Input Switch When CM<2:0>: = 001: 1 = C1 VIN- connects to RA3 0 = C1 VIN- connects to RA0 When CM<2:0> = 010: 1 = C1 VIN- connects to RA3 C2 VIN- connects to RA2 0 = C1 VIN- connects to RA2 0 = C1 VIN- connects to RA0 C2 VIN- connects to RA1										
bit 2-0	CM<2:0>: (	Comparator	mode.								
	Logondi										

L	.egend:			
F	R = Readable bit	W = Writable bit	U = Unimplemented	bit, read as '0'
-	n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

The code example in Example 7-1 depicts the steps required to configure the comparator module. RA3 and RA4 are configured as digital output. RA0 and RA1 are configured as the V- inputs and RA2 as the V+ input to both comparators.

### EXAMPLE 7-1: INITIALIZING COMPARATOR MODULE

MOVLW	0x03	;Init comparator mode
MOVWF	CMCON	;CM<2:0> = 011
CLRF	PORTA	;Init PORTA
BSF	STATUS, RPO	;Select Bank1
MOVLW	0x07	;Initialize data direction
MOVWF	TRISA	;Set RA<2:0> as inputs
		;RA<4:3> as outputs
		;TRISA<7:5> always read `0'
BCF	STATUS, RPO	;Select Bank 0
CALL	DELAY 10	;10µs delay
MOVF	CMCON,F	;Read CMCONtoend change condition
BCF	PIR1,CMIF	;Clear pending interrupts
BSF	STATUS, RPO	;Select Bank 1
BSF	PIE1,CMIE	;Enable comparator interrupts
BCF	STATUS, RPO	;Select Bank 0
BSF	INTCON, PEIE	;Enable peripheral interrupts
BSF	INTCON, GIE	;Global interrupt enable

## 7.2 Comparator Operation

A single comparator is shown in Figure 7-2 along with the relationship between the analog input levels and the digital output. When the analog input at VIN+ is less than the analog input VIN-, the output of the comparator is a digital low level. When the analog input at VIN+ is greater than the analog input VIN-, the output of the comparator is a digital high level. The shaded areas of the output of the comparator in Figure 7-2 represent the uncertainty due to input offsets and response time.

### 7.3 Comparator Reference

An external or internal reference signal may be used depending on the comparator Operating mode. The analog signal that is present at VIN- is compared to the signal at VIN+, and the digital output of the comparator is adjusted accordingly (Figure 7-2).





### 7.3.1 EXTERNAL REFERENCE SIGNAL

When external voltage references are used, the comparator module can be configured to have the comparators operate from the same or different reference sources. However, threshold detector applications may require the same reference. The reference signal must be between VSs and VDD, and can be applied to either pin of the comparator(s).

### 7.3.2 INTERNAL REFERENCE SIGNAL

The comparator module also allows the selection of an internally generated voltage reference for the comparators. Section 10, Instruction Sets, contains a detailed description of the Voltage Reference Module that provides this signal. The internal reference signal is used when the comparators are in mode CM<2:0>=010 (Figure 7-1). In this mode, the internal voltage reference is applied to the VIN+ pin of both comparators.

### 9.5.1 RB0/INT INTERRUPT

External interrupt on RB0/INT pin is edge triggered, either rising if INTEDG bit (OPTION<6>) is set, or falling, if INTEDG bit is clear. When a valid edge appears on the RB0/INT pin, the INTF bit (INTCON<1>) is set. This interrupt can be disabled by clearing the INTE control bit (INTCON<4>). The INTF bit must be cleared in software in the interrupt service routine before reenabling this interrupt. The RB0/INT interrupt can wake-up the processor from SLEEP, if the INTE bit was set prior to going into SLEEP. The status of the GIE bit decides whether or not the processor branches to the interrupt vector following wake-up. See Section 9.8 for details on SLEEP and Figure 9-18 for timing of wakeup from SLEEP through RB0/INT interrupt.

### 9.5.2 TMR0 INTERRUPT

An overflow (FFh  $\rightarrow$  00h) in the TMR0 register will set the T0IF (INTCON<2>) bit. The interrupt can be enabled/disabled by setting/clearing T0IE (INTCON<5>) bit. For operation of the Timer0 module, see Section 6.0.

### 9.5.3 PORTB INTERRUPT

An input change on PORTB <7:4> sets the RBIF (INTCON<0>) bit. The interrupt can be enabled/disabled by setting/clearing the RBIE (INTCON<4>) bit. For operation of PORTB (Section 5.2).

Note:	If a change on the I/O pin should occur
	when the read operation is being executed
	(start of the Q2 cycle), then the RBIF
	interrupt flag may not get set.

### 9.5.4 COMPARATOR INTERRUPT

See Section 7.6 for complete description of comparator interrupts.



### FIGURE 9-16: INT PIN INTERRUPT TIMING

# PIC16C62X

BCF	Bit Clear f	BTFSC	Bit Test, Skip if Clear			
Syntax:	[ <i>label</i> ]BCF f,b	Syntax:	[ <i>label</i> ]BTFSC f,b			
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ 0 \leq b \leq 7 \end{array}$	Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ 0 \leq b \leq 7 \end{array}$			
Operation:	$0 \rightarrow (f \le b >)$	Operation:	skip if (f <b>) = 0</b>			
Status Affected:	None	Status Affected:	None			
Encoding:	01 00bb bfff ffff	Encoding:	01 10bb bfff ffff			
Description:	Bit 'b' in register 'f' is cleared.	Description:	If bit 'b' in register 'f' is '0', then the			
Words:	1		next instruction is skipped.			
Cycles:	1		tion fetched during the current			
Example	BCF FLAG_REG, 7		instruction execution is discarded, and a NOP is executed instead, making this a two-cycle instruction.			
	Before Instruction FLAG REG = 0xC7					
	After Instruction	Words:	1			
	FLAG REG = 0x47	Cycles:	1(2)			
		Example	HERE BTFSC FLAG,1			
BSF	Bit Set f		TRUE • DE			
Syntax:	[ <i>label</i> ]BSF f,b		•			
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ 0 \leq b \leq 7 \end{array}$		Before Instruction PC = address HERE			
Operation:	$1 \rightarrow (f \le b >)$		After Instruction			
Status Affected:	None		PC = address TRUE			
Encoding:	01 01bb bfff ffff		if FLAG<1>=1,			
Description:	Bit 'b' in register 'f' is set.		PC = address FALSE			
Words:	1					
Cycles:	1					
Example	BSF FLAG_REG, 7					

Before Instruction FLAG\_REG = 0x0A After Instruction

FLAG\_REG = 0x8A

BTFSS Bit Test f, Skip if Set		CALL	Call Subroutine		
Syntax:	[ <i>label</i> ]BTFSS f,b	Syntax:	[ <i>label</i> ] CALL k		
Operands:	$0 \leq f \leq 127$	Operands:	$0 \leq k \leq 2047$		
Operation:	0 ≤ b < 7 skip if (f <b>) = 1</b>	Operation:	(PC)+ 1→ TOS, k → PC<10:0>, (PCLATH<4:3>) → PC<12:11>		
Encoding:		Status Affected:	None		
Encouring.	If hit 'h' in register 'f' is '1', then the	Encoding:	10 Okkk kkkk kkkk		
Description.	next instruction is skipped. If bit 'b' is '1', then the next instruc- tion fetched during the current instruction execution, is discarded and a NOP is executed instead, making this a two-cycle instruction.	Description:	Call Subroutine. First, return address (PC+1) is pushed onto the stack. The eleven bit immedi- ate address is loaded into PC bits <10:0>. The upper bits of the PC are loaded from PCLATH. CALL is		
Words:	1		a two-cycle instruction.		
Cycles:	1(2)	vvords:	1		
Example	HERE BTFSS FLAG,1	Cycles:	2		
	TRUE • DE	Example	HERE CALL THER E		
	Before Instruction PC = address HERE After Instruction if FLAG<1> = 0, PC = address FALSE if FLAG<1> = 1, PC = address TRUE		PC = Address HERE After Instruction PC = Address THERE TOS = Address HERE+1		
		CLRF	Clear f		
		Syntax:	[ <i>label</i> ] CLRF f		
		Operands:	$0 \le f \le 127$		
		Operation:	$\begin{array}{l} 00h \rightarrow (f) \\ 1 \rightarrow Z \end{array}$		
		Status Affected:	Z		
		Encoding:	00 0001 1fff ffff		
		Description:	The contents of register 'f' are cleared and the Z bit is set.		
		Words:	1		
		Cycles:	1		
		Example	CLRF FLAG_REG		
			Before Instruction FLAG_REG = 0x5A After Instruction FLAG_REG = 0x00 Z = 1		



### 12.1 DC Characteristics: PIC16C62X-04 (Commercial, Industrial, Extended) PIC16C62X-20 (Commercial, Industrial, Extended) PIC16LC62X-04 (Commercial, Industrial, Extended) (CONT.)

PIC16C62X PIC16LC62X				dard O ating te dard O ating te	peratii mpera peratir mpera	ng Cond ture -4 -4 ng Cond ture -4	ditions (unless otherwise stated) $0^{\circ}C \leq TA \leq +85^{\circ}C$ for industrial and $0^{\circ}C \leq TA \leq +70^{\circ}C$ for commercial and $0^{\circ}C \leq TA \leq +125^{\circ}C$ for extended ditions (unless otherwise stated) $0^{\circ}C \leq TA \leq +85^{\circ}C$ for industrial and $0^{\circ}C \leq TA \leq +85^{\circ}C$ for industrial and
				$-40^{\circ}$ C $\leq$ TA $\leq$ +125°C for extended Operating voltage VDD range is the PIC16C62X range.			
Param . No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
D022 D022A D023 D023A D022A D022A D022A D023	ΔIWDT ΔIBOR ΔICOM P ΔIVREF ΔIWDT ΔIBOR ΔICOM P	WDT Current <sup>(5)</sup> Brown-out Reset Current <sup>(5)</sup> Comparator Current for each Comparator <sup>(5)</sup> VREF Current <sup>(5)</sup> WDT Current <sup>(5)</sup> Brown-out Reset Current <sup>(5)</sup> Comparator Current for each Comparator <sup>(5)</sup>	  	6.0 350 — 6.0 350 —	20 25 425 100 300 15 425 100	μΑ μΑ μΑ μΑ μΑ μΑ	$VDD=4.0V$ $(125^{\circ}C)$ $BOD \text{ enabled, } VDD = 5.0V$ $VDD = 4.0V$ $VDD = 4.0V$ $VDD=3.0V$ $BOD \text{ enabled, } VDD = 5.0V$ $VDD = 3.0V$
D023A	$\Delta$ IVREF	VREF Current <sup>(5)</sup>	—	_	300	μA	VDD = 3.0V
1A	Fosc	LP Oscillator Operating Frequency RC Oscillator Operating Frequency XT Oscillator Operating Frequency HS Oscillator Operating Frequency	0 0 0 0		200 4 4 20	kHz MHz MHz MHz	All temperatures All temperatures All temperatures All temperatures
1A	Fosc	LP Oscillator Operating Frequency RC Oscillator Operating Frequency XT Oscillator Operating Frequency HS Oscillator Operating Frequency	0 0 0 0		200 4 4 20	kHz MHz MHz MHz	All temperatures All temperatures All temperatures All temperatures

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in Active Operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tri-stated, pulled to VDD,

MCLR = VDD; WDT enabled/disabled as specified.

**3:** The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or VSS.

4: For RC osc configuration, current through REXT is not included. The current through the resistor can be estimated by the formula: Ir = VDD/2REXT (mA) with REXT in kΩ.

5: The  $\Delta$  current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

### 12.3 DC CHARACTERISTICS: PIC16CR62XA-04 (Commercial, Industrial, Extended) PIC16CR62XA-20 (Commercial, Industrial, Extended) PIC16LCR62XA-04 (Commercial, Industrial, Extended)

PIC16CR62XA-04 PIC16CR62XA-20			Standard Operating Conditions (unless otherwise stated)Operating temperature $-40^{\circ}$ C $\leq$ TA $\leq$ +85°C for industrial and $0^{\circ}$ C $\leq$ TA $\leq$ +70°C for commercial and $-40^{\circ}$ C $\leq$ TA $\leq$ +125°C for extended					
PIC16LCR62XA-04			Stan Oper	dard O ating te	perati empera	ng Cor ature -	$\begin{array}{llllllllllllllllllllllllllllllllllll$	
Param. No.	Sym	Characteristic	Min	Тур†	Мах	Units	Conditions	
D001	Vdd	Supply Voltage	3.0	_	5.5	V	See Figures 12-7, 12-8, 12-9	
D001	Vdd	Supply Voltage	2.5	—	5.5	V	See Figures 12-7, 12-8, 12-9	
D002	Vdr	RAM Data Retention Voltage <sup>(1)</sup>	-	1.5*	—	V	Device in SLEEP mode	
D002	Vdr	RAM Data Retention Voltage <sup>(1)</sup>	—	1.5*	_	V	Device in SLEEP mode	
D003	VPOR	VDD start voltage to ensure Power-on Reset	-	Vss		V	See section on Power-on Reset for details	
D003	VPOR	VDD start voltage to ensure Power-on Reset	—	Vss		V	See section on Power-on Reset for details	
D004	SVDD	VDD rise rate to ensure Power-on Reset	0.05*	—	_	V/ms	See section on Power-on Reset for details	
D004	SVDD	VDD rise rate to ensure Power-on Reset	0.05*	—	_	V/ms	See section on Power-on Reset for details	
D005	VBOR	Brown-out Detect Voltage	3.7	4.0	4.35	V	BOREN configuration bit is cleared	
D005	VBOR	Brown-out Detect Voltage	3.7	4.0	4.35	V	BOREN configuration bit is cleared	
D010	IDD	Supply Current <sup>(2)</sup>	-	1.2	1.7	mA	Fosc = 4 MHz, VDD = 5.5V, WDT disabled, XT mode, (Note 4)*	
			_	500	900	μA	Fosc = 4 MHz, VDD = 3.0V, WDT disabled, XT mode, (Note 4)	
			_	1.0	2.0	mA	Fosc = 10 MHz, VDD = 3.0V, WDT disabled, HS mode, (Note 6)	
				4.0	7.0	mA	FOSC = 20 MHz, VDD = 5.5V, WD1 disabled*, HS	
				3.0	0.0 70		FOSC = 20  MHz $VDD = 4.5V$ WDT disabled HS mode	
				55	10	μΛ	Fose = $32 \text{ kHz}$ , VDD = $3.0\text{V}$ , WDT disabled, LP mode	
D010	IDD	Supply Current <sup>(2)</sup>	-	1.2	1.7	mA	Fosc = 4.0 MHz, VDD = 5.5V, WDT disabled, XT mode, ( <b>Note 4</b> )*	
			-	400	800	μA	Fosc = 4.0 MHz, VDD = 2.5V, WDT disabled, XT mode (Note 4)	
			—	35	70	μA	Fosc = 32 kHz, VDD = 2.5V, WDT disabled, LP mode	

#### 12.4 DC Characteristics: PIC16C62X/C62XA/CR62XA (Commercial, Industrial, Extended) PIC16LC62X/LC62XA/LCR62XA (Commercial, Industrial, Extended) (CONT.)

PIC16C	$\begin{array}{l lllllllllllllllllllllllllllllllllll$								
PIC16LC62X/LC62XA/LCR62XA			$\begin{array}{llllllllllllllllllllllllllllllllllll$						
Param. No.	Sym	Characteristic	Min	Min Typ† Max Units Conditions					
D040	Vih	Input High Voltage I/O ports with TTL buffer	2.0V	_	1/22	V	VDD = 4.5V to 5.5V		
D041		with Schmitt Trigger input	0.25 VDD + 0.8V		VDD VDD		otherwise		
D041			0.8 VDD	_	VDD	V			
D043 D043A		OSC1 (XT, HS and LP) OSC1 (in RC mode)	0.7 VDD 0.9 VDD	—	VDD	V	(Note 1)		
D070	IPURB	PORTB weak pull-up current	50	200	400	μA	VDD = 5.0V, VPIN = VSS		
D070	IPURB	PORTB weak pull-up current	50	200	400	μA	VDD = 5.0V, VPIN = VSS		
	lı∟	Input Leakage Current <sup>(2, 3)</sup> I/O ports (Except PORTA)			±1.0	μA	Vss $\leq$ VPIN $\leq$ VDD, pin at hi-impedance		
D060		PORTA	_	_	±0.5	μA	Vss $\leq$ VPIN $\leq$ VDD, pin at hi-impedance		
D061		RA4/T0CKI	_	_	±1.0	μA	$Vss \leq V \text{PIN} \leq V \text{DD}$		
D063		OSC1, MCLR			±5.0	μΑ	Vss $\leq$ VPIN $\leq$ VDD, XT, HS and LP osc configuration		
	lı∟	Input Leakage Current <sup>(2, 3)</sup>							
					±1.0	μΑ	$Vss \leq V PIN \leq V DD, \ pin \ at \ hi\text{-impedance}$		
D060		PORTA	—	—	±0.5	μA	$Vss \le VPIN \le VDD$ , pin at hi-impedance		
D061		RA4/T0CKI	—	—	±1.0	μA	$Vss \leq V \text{PIN} \leq V \text{DD}$		
D063		OSC1, MCLR	-		±5.0	μA	Vss $\leq$ VPIN $\leq$ VDD, XT, HS and LP osc configuration		
	Vol	Output Low Voltage							
D080		I/O ports	—	—	0.6	V	$IOL = 8.5 \text{ mA}, \text{ VDD} = 4.5 \text{V}, -40^{\circ} \text{ to } +85^{\circ}\text{C}$		
			—	—	0.6	V	IOL = 7.0 mA, VDD = 4.5V, +125°C		
D083		OSC2/CLKOUT (RC only)	—	0.6 V IOL = 1.6 mA, VDD = 4.5		$IOL = 1.6 \text{ mA}, \text{ VDD} = 4.5 \text{V}, -40^{\circ} \text{ to } +85^{\circ}\text{C}$			
			_	—	0.6	V	Iol = 1.2 mA, VDD = 4.5V, +125°C		

These parameters are characterized but not tested.

Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not t tested.

Note 1: In RC oscillator configuration, the OSC1 pin is a Schmitt Trigger input. It is not recommended that the PIC16C62X(A) be driven with external clock in RC mode.

2: The leakage current on the MCLR pin is strongly dependent on applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

**3:** Negative current is defined as coming out of the pin.

## 12.5 DC CHARACTERISTICS: PIC16C620A/C621A/C622A-40<sup>(7)</sup> (Commercial) PIC16CR620A-40<sup>(7)</sup> (Commercial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated)Operating temperature $0^{\circ}C \leq TA \leq +70^{\circ}C$ for commercial							
Param No.	Sym	Characteristic	Min Typ† Max		Unit	Unit Conditions				
	VIL	Input Low Voltage								
		I/O ports								
D030		with TTL buffer	Vss	—	0.8V 0.15Vdd	V	VDD = 4.5V to 5.5V, otherwise			
D031		with Schmitt Trigger input	Vss		0.2VDD	V				
D032		MCLR, RA4/T0CKI, OSC1 (in RC mode)	Vss	—	0.2Vdd	V	(Note 1)			
D033		OSC1 (in XT and HS)	Vss	—	0.3VDD	V				
		OSC1 (in LP)	Vss	_	0.6Vdd - 1.0	V				
	Vih	Input High Voltage								
		I/O ports								
D040		with TTL buffer	2.0V	—	VDD	V	VDD = 4.5V to 5.5V, otherwise			
D044		with Ochavitt Triansations t	0.25 VDD + 0.8		VDD					
D041					VDD					
D042		MCLR RA4/TUCKI		_	VDD	V				
D043 D043A		OSC1 (AT, HS and LP)		_	VDD	v	(Note 1)			
D070	IPURB	PORTB Weak Pull-up Current	50	200	400	μА	$V_{DD} = 5.0V$ . VPIN = Vss			
	liL	Input Leakage Current <sup>(2, 3)</sup>								
		I/O ports (except PORTA)			±1.0	μA	VSS $\leq$ VPIN $\leq$ VDD, pin at hi-impedance			
D060		PORTA	_	_	±0.5	μA	Vss $\leq$ VPIN $\leq$ VDD, pin at hi-impedance			
D061		RA4/T0CKI	—	—	±1.0	μA	$Vss \le VPIN \le VDD$			
D063		OSC1, MCLR	_	—	±5.0	μA	$Vss \leq VPIN \leq VDD,$ XT, HS and LP osc configuration			
	Vol	Output Low Voltage								
D080		I/O ports	_	—	0.6	V	IOL = 8.5 mA, VDD = 4.5V, -40° to +85°C			
			—	—	0.6	V	IOL = 7.0 mA, VDD = 4.5V, +125°C			
D083		OSC2/CLKOUT (RC only)	—	—	0.6	V	IOL = 1.6 mA, VDD = 4.5V, -40° to +85°C			
		(2)	_		0.6	V	IOL = 1.2 mA, VDD = 4.5V, +125°C			
	Vон	Output High Voltage <sup>(3)</sup>								
D090		I/O ports (except RA4)	VDD-0.7	—	—	V	IOH = -3.0 mA, VDD = 4.5V, -40° to +85°C			
			VDD-0.7	—	—	V	IOH = -2.5 mA, VDD = 4.5V, +125°C			
D092		OSC2/CLKOUT (RC only)	VDD-0.7	—	—	V	IOH = -1.3 mA, VDD = 4.5V, -40° to +85°C			
*0450	1/25	On an Duain Ulink Matterna	VDD-0.7	_		V	IOH = -1.0 mA, VDD = 4.5V, +125°C			
"D150	VOD	Open Drain High Voltage			8.5	V	RA4 pin			
		Capacitive Loading Specs on Output Pins								
D100	Cosc2	OSC2 pin			15	pF	In XT, HS and LP modes when external clock used to drive OSC1			
D101	Сю	All I/O pins/OSC2 (in RC mode)			50	pF				

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in Active Operation mode are:

OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD, MCLR = VDD; WDT enabled/disabled as specified.
 The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in bi-impedance state and tied to VDD or VSS.

 mode, with all I/O pins in hi-impedance state and tied to VDD or VSs.
 For RC osc configuration, current through REXT is not included. The current through the resistor can be estimated by the formula Ir = VDD/ 2REXT (mA) with REXT in kΩ.

5: The  $\Delta$  current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

6: Commercial temperature range only.

7: See Section 12.1 and Section 12.3 for 16C62X and 16CR62X devices for operation between 20 MHz and 40 MHz for valid modified characteristics.

## 12.6 DC Characteristics:

## PIC16C620A/C621A/C622A-40<sup>(3)</sup> (Commercial) PIC16CR620A-40<sup>(3)</sup> (Commercial)

DC CHARACTERISTICS Power Supply Pins		Standard Operating Conditions (unless otherwise stated) Operating temperature $0^{\circ}C \leq TA \leq +70^{\circ}C$ for commercial				
Characteristic Sym Min			Тур <sup>(1)</sup>	Max	Units	Conditions
Supply Voltage	Vdd	4.5	_	5.5	V	HS Option from 20 - 40 MHz
Supply Current <sup>(2)</sup>	IDD	_	5.5 7.7	11.5 16	mA mA	Fosc = 40 MHz, VDD = 4.5V, HS mode Fosc = 40 MHz, VDD = 5.5V, HS mode
HS Oscillator Operating Frequency	Fosc	20	_	40	MHz	OSC1 pin is externally driven, OSC2 pin not connected
Input Low Voltage OSC1	Vi∟	Vss	_	0.2VDD	V	HS mode, OSC1 externally driven
Input High Voltage OSC1 VIH 0.8		0.8Vdd	_	Vdd	V	HS mode, OSC1 externally driven

\* These parameters are characterized but not tested.

**Note 1:** Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in Active Operation mode are:

OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to Vss,

T0CKI = VDD, MCLR = VDD; WDT disabled, HS mode with OSC2 not connected.

**3:** For device operation between DC and 20 MHz. See Table 12-1 and Table 12-2.

## 12.7 AC Characteristics: PIC16C620A/C621A/C622A-40<sup>(2)</sup> (Commercial) PIC16CR620A-40<sup>(2)</sup> (Commercial)

AC CHARACTERISTICS All Pins Except Power Supply Pir		Standard Operating Conditions (unless otherwise stated)Operating temperature $0^{\circ}C \leq TA \leq +70^{\circ}C$ for commercial				
Characteristic	Min	Typ <sup>(1)</sup>	Max	Units	Conditions	
External CLKIN Frequency	Fosc	20	_	40	MHz	HS mode, OSC1 externally driven
External CLKIN Period	Tosc	25		50	ns	HS mode (40), OSC1 externally driven
Clock in (OSC1) Low or High Time	TosL, TosH	6			ns	HS mode, OSC1 externally driven
Clock in (OSC1) Rise or Fall Time	TosR, TosF	_	—	6.5	ns	HS mode, OSC1 externally driven
OSC1↑ (Q1 cycle) to Port out valid	TosH2IoV	_		100	ns	—
OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TosH2iol	50	_	—	ns	

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: For device operation between DC and 20 MHz. See Table 12-1 and Table 12-2.

## 12.8 Timing Parameter Symbology

The timing parameter symbols have been created with one of the following formats:

1. TppS2ppS

2. TppS

1.1.			
т			
F	Frequency	Т	Time
Lowerca	ase subscripts (pp) and their meanings:		
рр			
ck	CLKOUT	OSC	OSC1
io	I/O port	tO	ТОСКІ
mc	MCLR		
Upperca	ase letters and their meanings:		
S			
F	Fall	Р	Period
н	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-Impedance

### FIGURE 12-11: LOAD CONDITIONS



# PIC16C62X









## 14.0 PACKAGING INFORMATION

18-Lead Ceramic Dual In-line with Window (JW) – 300 mil (CERDIP)



		INCHES*		MILLIMETERS			
Dimension	MIN	NOM	MAX	MIN	NOM	MAX	
Number of Pins	n		18			18	
Pitch	р		.100			2.54	
Top to Seating Plane	Α	.170	.183	.195	4.32	4.64	4.95
Ceramic Package Height	A2	.155	.160	.165	3.94	4.06	4.19
Standoff	A1	.015	.023	.030	0.38	0.57	0.76
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Ceramic Pkg. Width	E1	.285	.290	.295	7.24	7.37	7.49
Overall Length	D	.880	.900	.920	22.35	22.86	23.37
Tip to Seating Plane	L	.125	.138	.150	3.18	3.49	3.81
Lead Thickness	С	.008	.010	.012	0.20	0.25	0.30
Upper Lead Width	B1	.050	.055	.060	1.27	1.40	1.52
Lower Lead Width	В	.016	.019	.021	0.41	0.47	0.53
Overall Row Spacing §	eB	.345	.385	.425	8.76	9.78	10.80
Window Width	W1	.130	.140	.150	3.30	3.56	3.81
Window Length	W2	.190	.200	.210	4.83	5.08	5.33

\* Controlling Parameter
 § Significant Characteristic
 JEDEC Equivalent: MO-036
 Drawing No. C04-010

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