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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	13
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c622-20e-ss

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NOTES:

FIGURE 3-1: BLOCK DIAGRAM



4.2.2.3 INTCON Register

The INTCON register is a readable and writable register, which contains the various enable and flag bits for all interrupt sources except the comparator module. See Section 4.2.2.4 and Section 4.2.2.5 for a description of the comparator enable and flag bits.

Note: Interrupt flag bits get set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>).

	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x				
	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF				
	bit 7			<u>.</u>		<u>.</u>		bit 0				
bit 7	GIE: Globa	I Interrupt E	nable bit									
	1 = Enables	s all un-mas	sked interrup	ots								
1.11.0		s all interru	pts									
0 110	PEIE: Perip		upt Enable i	DIT 	-							
	1 = Enables 0 = Disable	s all un-mas	sked periphe eral interrun	eral interrupt	S							
bit 5		0 Overflow	Interrunt En	able bit								
bit o	1 = Enables	s the TMR0	interrupt									
	0 = Disable	s the TMR) interrupt									
bit 4	INTE: RB0/	INTE: RB0/INT External Interrupt Enable bit										
	1 = Enables the RB0/INT external interrupt											
	0 = Disable	s the RB0/I	NT external	interrupt								
bit 3	RBIE: RB F	ort Change	Interrupt E	nable bit								
	1 = Enables	s the RB po	rt change in	iterrupt								
L:4 0			oft change in	iterrupi								
DIL ∠		J OVernow i		g Dit	- ared in coff	+						
	1 = TMR0 r 0 = TMR0 r	register did	not overflow	(ที่มีประ มีฮ มีฮ /	aleu ili son	ware						
bit 1	INTF: RB0/	INT Externa	al Interrupt F	-lag bit								
	1 = The RB	30/INT exter	nal interrup	t occurred (n	nust be clea	ared in softw	are)					
	0 = The RB	30/INT exter	nal interrupt	t did not occ	ur							
bit 0	RBIF : RB F	ort Change	Interrupt Fl	lag bit								
	1 = When a	at least one	of the RB<7	':4> pins cha	anged state	(must be cle	ared in soft	ware)				
	0 = None o	f the RB<1	4> pins nave	e changea s	tate							
	Larandi											
	Legend:											

REGISTER 4-3:	INTCON REGISTER (ADDRESS 0BH OR 8BH)	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented	bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

4.3 PCL and PCLATH

The program counter (PC) is 13-bits wide. The low byte comes from the PCL register, which is a readable and writable register. The high byte (PC<12:8>) is not directly readable or writable and comes from PCLATH. On any RESET, the PC is cleared. Figure 4-8 shows the two situations for the loading of the PC. The upper example in the figure shows how the PC is loaded on a write to PCL (PCLATH<4:0> \rightarrow PCH). The lower example in the figure shows how the PC is loaded during a CALL or GOTO instruction (PCLATH<4:3> \rightarrow PCH).

FIGURE 4-8: LOADING OF PC IN DIFFERENT SITUATIONS



4.3.1 COMPUTED GOTO

A computed GOTO is accomplished by adding an offset to the program counter (ADDWF PCL). When doing a table read using a computed GOTO method, care should be exercised if the table location crosses a PCL memory boundary (each 256 byte block). Refer to the application note, *"Implementing a Table Read"* (AN556).

4.3.2 STACK

The PIC16C62X family has an 8-level deep x 13-bit wide hardware stack (Figure 4-2 and Figure 4-3). The stack space is not part of either program or data space and the stack pointer is not readable or writable. The PC is PUSHed onto the stack when a CALL instruction is executed or an interrupt causes a branch. The stack is POPed in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not affected by a PUSH or POP operation.

The stack operates as a circular buffer. This means that after the stack has been PUSHed eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on).

- Note 1: There are no STATUS bits to indicate stack overflow or stack underflow conditions.
 - 2: There are no instructions/mnemonics called PUSH or POP. These are actions that occur from the execution of the CALL, RETURN, RETLW and RETFIE instructions, or the vectoring to an interrupt address.

5.0 I/O PORTS

The PIC16C62X have two ports, PORTA and PORTB. Some pins for these I/O ports are multiplexed with an alternate function for the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

5.1 PORTA and TRISA Registers

PORTA is a 5-bit wide latch. RA4 is a Schmitt Trigger input and an open drain output. Port RA4 is multiplexed with the T0CKI clock input. All other RA port pins have Schmitt Trigger input levels and full CMOS output drivers. All pins have data direction bits (TRIS registers), which can configure these pins as input or output.

A '1' in the TRISA register puts the corresponding output driver in a Hi-impedance mode. A '0' in the TRISA register puts the contents of the output latch on the selected pin(s).

Reading the PORTA register reads the status of the pins, whereas writing to it will write to the port latch. All write operations are read-modify-write operations. So a write to a port implies that the port pins are first read, then this value is modified and written to the port data latch.

The PORTA pins are multiplexed with comparator and voltage reference functions. The operation of these pins are selected by control bits in the CMCON (comparator control register) register and the VRCON (voltage reference control register) register. When selected as a comparator input, these pins will read as '0's.

FIGURE 5-1: BLOCK DIAGRAM OF RA1:RA0 PINS



Note:	On RESET, the TRISA register is set to all
	inputs. The digital inputs are disabled and
	the comparator inputs are forced to ground
	to reduce excess current consumption.

TRISA controls the direction of the RA pins, even when they are being used as comparator inputs. The user must make sure to keep the pins configured as inputs when using them as comparator inputs.

The RA2 pin will also function as the output for the voltage reference. When in this mode, the VREF pin is a very high impedance output and must be buffered prior to any external load. The user must configure TRISA<2> bit as an input and use high impedance loads.

In one of the Comparator modes defined by the CMCON register, pins RA3 and RA4 become outputs of the comparators. The TRISA<4:3> bits must be cleared to enable outputs to use this function.

EXAMPLE 5-1: INITIALIZING PORTA

CLRF	PORTA	;Initialize PORTA by setting ;output data latches
MOVLW	0X07	;Turn comparators off and
MOVWF	CMCON	;enable pins for I/O ;functions
BSF	STATUS, RPO	;Select Bank1
MOVLW	0x1F	;Value used to initialize
		;data direction
MOVWF	TRISA	;Set RA<4:0> as inputs
		;TRISA<7:5> are always
		;read as '0'.

FIGURE 5-2: BLOCK DIAGRAM OF RA2 PIN



5.2 PORTB and TRISB Registers

PORTB is an 8-bit wide, bi-directional port. The corresponding data direction register is TRISB. A '1' in the TRISB register puts the corresponding output driver in a High Impedance mode. A '0' in the TRISB register puts the contents of the output latch on the selected pin(s).

Reading PORTB register reads the status of the pins, whereas writing to it will write to the port latch. All write operations are read-modify-write operations. So a write to a port implies that the port pins are first read, then this value is modified and written to the port data latch.

Each of the PORTB pins has a weak internal pull-up ($\approx 200 \ \mu A \ typical$). A single control bit can turn on all the pull-ups. This is done by clearing the RBPU (OPTION<7>) bit. The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on Power-on Reset.

Four of PORTB's pins, RB<7:4>, have an interrupt on change feature. Only pins configured as inputs can cause this interrupt to occur (e.g., any RB<7:4> pin configured as an output is excluded from the interrupt on change comparison). The input pins (of RB<7:4>) are compared with the old value latched on the last read of PORTB. The "mismatch" outputs of RB<7:4> are OR'ed together to generate the RBIF interrupt (flag latched in INTCON<0>).

FIGURE 5-5: BLOCK DIAGRAM OF RB<7:4> PINS



This interrupt can wake the device from SLEEP. The user, in the interrupt service routine, can clear the interrupt in the following manner:

- a) Any read or write of PORTB. This will end the mismatch condition.
- b) Clear flag bit RBIF.

A mismatch condition will continue to set flag bit RBIF. Reading PORTB will end the mismatch condition and allow flag bit RBIF to be cleared.

This interrupt on mismatch feature, together with software configurable pull-ups on these four pins allow easy interface to a key pad and make it possible for wake-up on key-depression. (See AN552, "Implementing Wake-Up on Key Strokes.)

Note:	If a change on the I/O pin should occur							
	when the read operation is being executed							
	(start of the Q2 cycle), then the RBIF inter-							
	rupt flag may not get set.							

The interrupt-on-change feature is recommended for wake-up on key depression operation and operations where PORTB is only used for the interrupt on change feature. Polling of PORTB is not recommended while using the interrupt-on-change feature.





The code example in Example 7-1 depicts the steps required to configure the comparator module. RA3 and RA4 are configured as digital output. RA0 and RA1 are configured as the V- inputs and RA2 as the V+ input to both comparators.

EXAMPLE 7-1: INITIALIZING COMPARATOR MODULE

MOVLW	0x03	;Init comparator mode
MOVWF	CMCON	;CM<2:0> = 011
CLRF	PORTA	;Init PORTA
BSF	STATUS, RPO	;Select Bank1
MOVLW	0x07	;Initialize data direction
MOVWF	TRISA	;Set RA<2:0> as inputs
		;RA<4:3> as outputs
		;TRISA<7:5> always read `0'
BCF	STATUS, RPO	;Select Bank 0
CALL	DELAY 10	;10µs delay
MOVF	CMCON,F	;Read CMCONtoend change condition
BCF	PIR1,CMIF	;Clear pending interrupts
BSF	STATUS, RPO	;Select Bank 1
BSF	PIE1,CMIE	;Enable comparator interrupts
BCF	STATUS, RPO	;Select Bank 0
BSF	INTCON, PEIE	;Enable peripheral interrupts
BSF	INTCON, GIE	;Global interrupt enable

7.2 Comparator Operation

A single comparator is shown in Figure 7-2 along with the relationship between the analog input levels and the digital output. When the analog input at VIN+ is less than the analog input VIN-, the output of the comparator is a digital low level. When the analog input at VIN+ is greater than the analog input VIN-, the output of the comparator is a digital high level. The shaded areas of the output of the comparator in Figure 7-2 represent the uncertainty due to input offsets and response time.

7.3 Comparator Reference

An external or internal reference signal may be used depending on the comparator Operating mode. The analog signal that is present at VIN- is compared to the signal at VIN+, and the digital output of the comparator is adjusted accordingly (Figure 7-2).





7.3.1 EXTERNAL REFERENCE SIGNAL

When external voltage references are used, the comparator module can be configured to have the comparators operate from the same or different reference sources. However, threshold detector applications may require the same reference. The reference signal must be between VSs and VDD, and can be applied to either pin of the comparator(s).

7.3.2 INTERNAL REFERENCE SIGNAL

The comparator module also allows the selection of an internally generated voltage reference for the comparators. Section 10, Instruction Sets, contains a detailed description of the Voltage Reference Module that provides this signal. The internal reference signal is used when the comparators are in mode CM<2:0>=010 (Figure 7-1). In this mode, the internal voltage reference is applied to the VIN+ pin of both comparators.

9.3 RESET

The PIC16C62X differentiates between various kinds of RESET:

- a) Power-on Reset (POR)
- b) MCLR Reset during normal operation
- c) MCLR Reset during SLEEP
- d) WDT Reset (normal operation)
- e) WDT wake-up (SLEEP)
- f) Brown-out Reset (BOR)

Some registers are not affected in any RESET condition Their status is unknown on POR and unchanged in any other RESET. Most other registers are reset to a "RESET state" on Power-on Reset,

MCLR Reset, WDT Reset and MCLR Reset during SLEEP. They are not affected by a WDT wake-up, since this is viewed as the resumption of normal operation. TO and PD bits are set or cleared differently in different RESET situations as indicated in Table 9-2. These bits are used in software to determine the nature of the RESET. See Table 9-5 for a full description of RESET states of all registers.

A simplified block diagram of the on-chip RESET circuit is shown in Figure 9-6.

The $\overline{\text{MCLR}}$ Reset path has a noise filter to detect and ignore small pulses. See Table 12-5 for pulse width specification.





9.4.5 TIME-OUT SEQUENCE

On power-up the time-out sequence is as follows: First PWRT time-out is invoked after POR has expired. Then OST is activated. The total time-out will vary based on oscillator configuration and <u>PWRTE</u> bit status. For example, in RC mode with <u>PWRTE</u> bit erased (<u>PWRT</u> disabled), there will be no time-out at all. Figure 9-8, Figure 9-9 and Figure 9-10 depict time-out sequences.

Since the time-outs occur from the POR pulse, if $\overline{\text{MCLR}}$ is kept low long enough, the time-outs will expire. Then bringing $\overline{\text{MCLR}}$ high will begin execution immediately (see Figure 9-9). This is useful for testing purposes or to synchronize more than one PIC16C62X device operating in parallel.

Table 9-4 shows the RESET conditions for some special registers, while Table 9-5 shows the RESET conditions for all the registers.

9.4.6 POWER CONTROL (PCON)/ STATUS REGISTER

The power control/STATUS register, PCON (address 8Eh), has two bits.

Bit0 is $\overline{\text{BOR}}$ (Brown-out). $\overline{\text{BOR}}$ is unknown on Poweron Reset. It must then be set by the user and checked on subsequent RESETS to see if $\overline{\text{BOR}} = 0$, indicating that a brown-out has occurred. The $\overline{\text{BOR}}$ STATUS bit is a don't care and is not necessarily predictable if the brown-out circuit is disabled (by setting BODEN bit = 0 in the Configuration word).

Bit1 is POR (Power-on Reset). It is a '0' on Power-on Reset and unaffected otherwise. The user must write a '1' to this bit following a Power-on Reset. On a subsequent RESET, if POR is '0', it will indicate that a Power-on Reset must have occurred (VDD may have gone too low).

Oscillator Configuration	Powe	er-up	Brown-out Reset	Wake-up from SLEEP	
Coolinator Configuration	PWRTE = 0	PWRTE = 1	Brown out Rooot		
XT, HS, LP	72 ms + 1024 Tosc	1024 Tosc	72 ms + 1024 Tosc	1024 Tosc	
RC	72 ms		72 ms	_	

TABLE 9-1: TIME-OUT IN VARIOUS SITUATIONS

	TABLE 9-2 :	STATUS/PCON BITS AND THEIR SIGNIFICANCE
--	--------------------	---

POR	BOR	то	PD	
0	Х	1	1	Power-on Reset
0	Х	0	Х	Illegal, TO is set on POR
0	Х	Х	0	Illegal, PD is set on POR
1	0	Х	Х	Brown-out Reset
1	1	0	u	WDT Reset
1	1	0	0	WDT Wake-up
1	1	u	u	MCLR Reset during normal operation
1	1	1	0	MCLR Reset during SLEEP

Legend: u = unchanged, x = unknown

TABLE 9-3: SUMMARY OF REGISTERS ASSOCIATED WITH BROWN-OUT

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR Reset	Value on all other RESETS ⁽¹⁾
83h	STATUS				TO	PD				0001 1xxx	000q quuu
8Eh	PCON	_	_				_	POR	BOR	0x	uq

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0', q = value depends on condition.

Note 1: Other (non Power-up) Resets include MCLR Reset, Brown-out Reset and Watchdog Timer Reset during normal operation.

9.7 Watchdog Timer (WDT)

The Watchdog Timer is a free running on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the RC oscillator of the CLKIN pin. That means that the WDT will run, even if the clock on the OSC1 and OSC2 pins of the device has been stopped, for example, by execution of a SLEEP instruction. During normal operation, a WDT time-out generates a device RESET. If the device is in SLEEP mode, a WDT time-out causes the device to wake-up and continue with normal operation. The WDT can be permanently disabled by programming the configuration bit WDTE as clear (Section 9.1).

9.7.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms, (with no prescaler). The time-out periods vary with temperature, VDD and process variations from part to part (see

DC specs). If longer time-out periods are desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT under software control by writing to the OPTION register. Thus, time-out periods up to 2.3 seconds can be realized.

The CLRWDT and SLEEP instructions clear the WDT and the postscaler, if assigned to the WDT, and prevent it from timing out and generating a device RESET.

The $\overline{\text{TO}}$ bit in the STATUS register will be cleared upon a Watchdog Timer time-out.

9.7.2 WDT PROGRAMMING CONSIDERATIONS

It should also be taken in account that under worst case conditions (VDD = Min., Temperature = Max., max. WDT prescaler) it may take several seconds before a WDT time-out occurs.



FIGURE 9-17: WATCHDOG TIMER BLOCK DIAGRAM

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR Reset	Value on all other RESETS
2007h	Config. bits	—	BODEN	CP1	CP0	PWRTE	WDTE	FOSC1	FOSC0	—	—
81h	OPTION	RBPU	INTEDG	TOCS	TOSE	PSA	PS2	PS1	PS0	1111 1111	1111 1111

Legend: Shaded cells are not used by the Watchdog Timer.

Note: – = Unimplemented location, read as "0"

+ = Reserved for future use

RETFIE	Return from Interrupt								
Syntax:	[label]	RETFIE	-						
Operands:	None								
Operation:	$TOS \rightarrow PC, \\ 1 \rightarrow GIE$								
Status Affected:	None								
Encoding:	00	0000	0000	1001					
Description:	Return fro POPed a loaded in enabled b Interrupt (INTCON instructio	om Intern nd Top o the PC. by setting Enable b I<7>). Th n.	rupt. Stac f Stack (T Interrupts g Global bit, GIE iis is a two	k is OS) is s are o-cycle					
Words:	1								
Cycles:	2								
Example	RETFIE								
	After Inte	rrupt PC = GIE =	TOS 1						

RETLW	Return with Literal in W								
Syntax:	[<i>label</i>] RETLW k								
Operands:	$0 \leq k \leq 255$								
Operation:	$k \rightarrow (W);$ TOS \rightarrow PC								
Status Affected:	None								
Encoding:	11 01xx kkkk kkkk								
Description:	The W register is loaded with the eight bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a two-cycle instruction.								
Words:	1								
Cycles:	2								
Example	CALL TABLE;W contains table								
TABLE	;offset value • ;W now has table value •								
	ADDWF PC ;W = offset RETLW k1 ;Begin table RETLW k2 ;								
	• RETLW kn ;End of table								
	Before Instruction								
	W = 0x07 After Instruction W = value of k8								
RETURN	Return from Subroutine								
Svntax:	[<i>label</i>] RETURN								
Operands:	None								
Operation:	$TOS \rightarrow PC$								
Status Affected:	None								
Encoding:	00 0000 0000 1000								
Description:	Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a two-cycle instruction.								
Words:	1								
Cycles:	2								
Example	RETURN								
	After Interrupt PC = TOS								

SUBLW	Subtract W from Literal	SUBWF	Subtract W from f
Syntax:	[<i>label</i>] SUBLW k	Syntax:	[<i>label</i>] SUBWF f,d
Operands:	$0 \le k \le 255$	Operands:	$0 \le f \le 127$
Operation:	$k - (W) \rightarrow (W)$		d ∈ [0,1]
Status Affected:	C, DC, Z	Operation: Status	(f) - (W) \rightarrow (dest) C, DC, Z
Encoding:	11 110x kkkk kkkk	Affected:	
Description:	The W register is subtracted (2's complement method) from the eight bit literal 'k'. The result is placed in the W register.	Encoding: Description:	000010dfffffffSubtract (2's complement method)W register from register 'f'. If 'd' is 0,the result is stored in the W register.If 'd' is 1, the result is stored head in
Words:	1		register 'f'.
Cycles:	1	Words:	1
Example 1:	SUBLW 0x02	Cycles:	1
	Before Instruction	Example 1:	SUBWF REG1,1
	W = 1 $C = ?$		Before Instruction
	After Instruction		REG1= 3
	W = 1		W = 2 C = ?
Example 2:	Before Instruction		After Instruction
Example 2.	W = 2 $C = ?$		REG1= 1 W = 2 C = 1; result is positive
	After Instruction	Example 2:	Before Instruction
	W = 0 C = 1; result is zero		REG1= 2 W = 2
Example 3:	Before Instruction		C = ?
	W = 3 C = ?		After Instruction REG1= 0
	After Instruction		W = 2
	W = 0xFF	Example 3	C = 1; result is zero Before Instruction
	C – 0, result is negative		REG1= 1 W = 2 C = ?
			After Instruction
			REG1= 0xFF W = 2 C = 0; result is negative





2: The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.









Parameter No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
10*	TosH2ckL	OSC1↑ to CLKOUT↓ ⁽¹⁾		75 —	200 400	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
11*	TosH2ck H	OSC1↑ to CLKOUT↑ ⁽¹⁾	_	75 —	200 400	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
12*	TckR	CLKOUT rise time ⁽¹⁾		35 —	100 200	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
13*	TckF	CLKOUT fall time ⁽¹⁾		35 —	100 200	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
14*	TckL2ioV	CLKOUT \downarrow to Port out valid ⁽¹⁾	_	—	20	ns	
15*	TioV2ckH	Port in valid before CLKOUT ↑ ⁽¹⁾	Tosc +200 ns Tosc +400 ns	_	_	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
16*	TckH2iol	Port in hold after CLKOUT $\uparrow^{(1)}$	0	—		ns	
17*	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid	_	50	150 300	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
18*	TosH2iol	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	100 200	_	_	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
19*	TioV2osH	Port input valid to OSC1 [↑] (I/O in setup time)	0	—	—	ns	
20*	TioR	Port output rise time	_	10 —	40 80	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
21*	TioF	Port output fall time	_	10 —	40 80	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
22*	Tinp	RB0/INT pin high or low time	25 40	_	_	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
23	Trbp	RB<7:4> change interrupt high or low time	Тсү	—	—	ns	

TABLE 12-4: CLKOUT AND I/O TIMING REQUIREMENTS

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.

FIGURE 12-14: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING



FIGURE 12-15: BROWN-OUT RESET TIMING



TABLE 12-5:RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP
TIMER REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
30	TmcL	MCLR Pulse Width (low)	2000	—		ns	-40° to +85°C
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7*	18	33*	ms	VDD = 5.0V, -40° to +85°C
32	Tost	Oscillation Start-up Timer Period	_	1024 Tosc	_		Tosc = OSC1 period
33	Tpwrt	Power-up Timer Period	28*	72	132*	ms	VDD = 5.0V, -40° to +85°C
34	Tioz	I/O hi-impedance from MCLR low		—	2.0	μS	
35	TBOR	Brown-out Reset Pulse Width	100*	_		μs	$3.7V \leq V\text{DD} \leq 4.3V$

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 12-16: TIMER0 CLOCK TIMING



TABLE 12-6: TIMER0 CLOCK REQUIREMENTS	TABLE 12-6:	TIMER0 CLOCK REQUIREMENTS
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Parameter No.	Sym	Characteristic		Min	Тур†	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width	No Prescaler	0.5 Tcy + 20*	—	—	ns	
			With Prescaler	10*	—		ns	
41	Tt0L	T0CKI Low Pulse Width	No Prescaler	0.5 Tcy + 20*	—	-	ns	
			With Prescaler	10*	—	-	ns	
42	Tt0P	T0CKI Period		$\frac{\text{TCY} + 40}{\text{N}}^*$	-		ns	N = prescale value (1, 2, 4,, 256)

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.





APPENDIX A: ENHANCEMENTS

The following are the list of enhancements over the PIC16C5X microcontroller family:

- Instruction word length is increased to 14 bits. This allows larger page sizes both in program memory (4K now as opposed to 512 before) and register file (up to 128 bytes now versus 32 bytes before).
- 2. A PC high latch register (PCLATH) is added to handle program memory paging. PA2, PA1, PA0 bits are removed from STATUS register.
- 3. Data memory paging is slightly redefined. STATUS register is modified.
- Four new instructions have been added: RETURN, RETFIE, ADDLW, and SUBLW.
 Two instructions TRIS and OPTION are being phased out, although they are kept for compatibility with PIC16C5X.
- 5. OPTION and TRIS registers are made addressable.
- 6. Interrupt capability is added. Interrupt vector is at 0004h.
- 7. Stack size is increased to 8 deep.
- 8. RESET vector is changed to 0000h.
- RESET of all registers is revisited. Five different RESET (and wake-up) types are recognized. Registers are reset differently.
- 10. Wake-up from SLEEP through interrupt is added.
- 11. Two separate timers, Oscillator Start-up Timer (OST) and Power-up Timer (PWRT) are included for more reliable power-up. These timers are invoked selectively to avoid unnecessary delays on power-up and wake-up.
- 12. PORTB has weak pull-ups and interrupt-onchange feature.
- 13. Timer0 clock input, T0CKI pin is also a port pin (RA4/T0CKI) and has a TRIS bit.
- 14. FSR is made a full 8-bit register.
- 15. "In-circuit programming" is made possible. The user can program PIC16CXX devices using only five pins: VDD, VSS, VPP, RB6 (clock) and RB7 (data in/out).
- PCON STATUS register is added with a Poweron-Reset (POR) STATUS bit and a Brown-out Reset STATUS bit (BOD).
- 17. Code protection scheme is enhanced such that portions of the program memory can be protected, while the remainder is unprotected.
- 18. PORTA inputs are now Schmitt Trigger inputs.
- 19. Brown-out Reset reset has been added.
- 20. Common RAM registers F0h-FFh implemented in bank1.

APPENDIX B: COMPATIBILITY

To convert code written for PIC16C5X to PIC16CXX, the user should take the following steps:

- 1. Remove any program memory page select operations (PA2, PA1, PA0 bits) for CALL, GOTO.
- 2. Revisit any computed jump operations (write to PC or add to PC, etc.) to make sure page bits are set properly under the new scheme.
- 3. Eliminate any data memory page switching. Redefine data variables to reallocate them.
- 4. Verify all writes to STATUS, OPTION, and FSR registers since these have changed.
- 5. Change RESET vector to 0000h.

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