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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	·
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	13
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	OTP
EEPROM Size	
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c622a-04-ss

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		PIC16C620 ⁽³⁾	PIC16C620A ⁽¹⁾⁽⁴⁾	PIC16CR620A ⁽²⁾	PIC16C621 ⁽³⁾	PIC16C621A ⁽¹⁾⁽⁴⁾	PIC16C622 ⁽³⁾	PIC16C622A ⁽¹⁾⁽⁴⁾
Clock	Maximum Frequency of Operation (MHz)	20	40	20	20	40	20	40
Memory	EPROM Program Memory (x14 words)	512	512	512	1K	1K	2K	2K
	Data Memory (bytes)	80	96	96	80	96	128	128
Peripherals	Timer Module(s)	TMR0	TMR0	TMRO	TMR0	TMR0	TMR0	TMR0
	Comparators(s)	2	2	2	2	2	2	2
	Internal Reference Voltage	Yes						
Features	Interrupt Sources	4	4	4	4	4	4	4
	I/O Pins	13	13	13	13	13	13	13
	Voltage Range (Volts)	2.5-6.0	2.7-5.5	2.5-5.5	2.5-6.0	2.7-5.5	2.5-6.0	2.7-5.5
	Brown-out Reset	Yes						
	Packages	18-pin DIP, SOIC; 20-pin SSOP						

TABLE 1-1: PIC16C62X FAMILY OF DEVICES

All PICmicro[®] Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability. All PIC16C62X Family devices use serial programming with clock pin RB6 and data pin RB7.

Note 1: If you change from this device to another device, please verify oscillator characteristics in your application.

2: For ROM parts, operation from 2.0V - 2.5V will require the PIC16LCR62XA parts.

3: For OTP parts, operation from 2.5V - 3.0V will require the PIC16LC62X part.

4: For OTP parts, operation from 2.7V - 3.0V will require the PIC16LC62XA part.

FIGURE 4-6: DATA MEMORY MAP FOR THE PIC16C620A/CR620A/621A

File Address	5		File Address				
00h	INDF ⁽¹⁾	INDF ⁽¹⁾	80h				
01h	TMR0	OPTION	81h				
02h	PCL	PCL	82h				
03h	STATUS	STATUS	83h				
04h	FSR	FSR	84h				
05h	PORTA	TRISA	85h				
06h	PORTB	TRISB	86h				
07h			87h				
08h			88h				
09h			89h				
0Ah	PCLATH	PCLATH	8Ah				
0Bh	INTCON	INTCON	8Bh				
0Ch	PIR1	PIE1	8Ch				
0Dh			8Dh				
0Eh		PCON	8Eh				
0Fh			8Fh				
10h			90h				
11h			91h				
12h			92h				
13h			93h				
14h			94h				
15h			95h				
16h			96h				
17h			97h				
18h			98h				
19h			99h				
1Ah			9Ah				
1Bh			9Bh				
1Ch			9Ch				
1Dh			9Dh				
1Eh			9Eh				
1Fh	CMCON	VRCON	9Fh				
20h	General Purpose Register		A0h				
6Fh							
70h	General		F0h				
7011	Purpose	Accesses					
7Fh	Register	1011-1711	FFh				
	Bank 0	Bank 1					
Unimp	Unimplemented data memory locations, read as '0'.						
Note 1:	Not a physical re	gister.					

FIGURE 4-7: DATA MEMORY MAP FOR THE PIC16C622A

File Address	;		File Address
00h	INDF ⁽¹⁾	INDF ⁽¹⁾	80h
01h	TMR0	OPTION	81h
02h	PCL	PCL	82h
03h	STATUS	STATUS	83h
04h	FSR	FSR	84h
05h	PORTA	TRISA	85h
06h	PORTB	TRISB	86h
07h			87h
08h			88h
09h			89h
0Ah	PCLATH	PCLATH	8Ah
0Bh	INTCON	INTCON	8Bh
0Ch	PIR1	PIE1	8Ch
0Dh			8Dh
0Eh		PCON	8Eh
0Fh			8Fh
10h			90h
11h			91h
12h			92h
13h			93h
14h			94h
15h			95h
16h			96h
17h			97h
18h			98h
19h			99h
1Ah			9Ah
1Bh			9Bh
1Ch			9Ch
1Dn			
1En	014001		9En
1Fn	CMCON	VRCON	9Fn
20h	General	General	A0h
	Purpose	Purpose	
	Register	Register	BFh
			C0h
			0011
6Fh			– F0h
70h	General	Accesses	
	Register	70h-7Fh	EEh
/Fhl	Bank 0	Bank 1	
Unimp	elemented data me	mory locations, re	ead as '0'.
Note 1:	Not a physical re	egister.	

4.2.2.4 PIE1 Register

This register contains the individual enable bit for the comparator interrupt.

REGISTER 4-4:	PIE1 REGISTER (ADDRESS 8CH)							
	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0
		CMIE	—	_	—	_		
	bit 7							bit 0
bit 7	Unimpleme	nted: Read	d as '0'					
bit 6	CMIE: Com	parator Inte	errupt Enable	e bit				
	 1 = Enables the Comparator interrupt 0 = Disables the Comparator interrupt 							
bit 5-0	Unimpleme	nted: Read	d as '0'					
	Legend:							
	R = Readab	le bit	W = W	ritable bit	U = Unim	plemented	bit, read as '	0'
	- n = Value a	at POR	'1' = Bi	it is set	'0' = Bit i	s cleared	x = Bit is u	nknown

4.2.2.5 PIR1 Register

This register contains the individual flag bit for the comparator interrupt.

Note:	Interrupt flag bits get set when an interrupt
	condition occurs, regardless of the state of
	its corresponding enable bit or the global
	enable bit, GIE (INTCON<7>). User
	software should ensure the appropriate
	interrupt flag bits are clear prior to enabling
	an interrupt.

REGISTER 4-5: PIR1 REGISTER (ADDRESS 0CH)

_I\ 4 -J.	FINTNEO										
	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0			
	—	CMIF		_	—	_	—	_			
	bit 7							bit 0			
bit 7	Unimplem	ented: Rea	d as '0'								
bit 6	CMIF: Com	nparator Inte	errupt Flag b	it							
	1 = Compa	rator input h	nas changed								
	0 = Compa	rator input h	nas not chan	ged							
bit 5-0	Unimplem	ented: Rea	d as '0'								
	Legend:										
	R = Reada	ble bit	W = W	ritable bit	U = Unim	plemented	bit, read as '	0'			
	- n = Value	at POR	'1' = B	it is set	'0' = Bit is	s cleared	x = Bit is u	nknown			









6.3.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control (i.e., it can be changed "on-the-fly" during program execution). To avoid an unintended device RESET, the following instruction sequence (Example 6-1) must be executed when changing the prescaler assignment from Timer0 to WDT.)

EXAMPLE 6-1: CHANGING PRESCALER (TIMER0→WDT)

	-	
1.BCF	STATUS, RPO	;Skip if already in ;Bank 0
2.CLRWDT		;Clear WDT
3.CLRF	TMR0	;Clear TMR0 & Prescaler
4.BSF	STATUS, RPO	;Bank 1
5.MOVLW	'00101111'b;	;These 3 lines (5, 6, 7)
6.MOVWF	OPTION	;are required only if ;desired PS<2:0> are
7.CLRWDT		;000 or 001
8.MOVLW	'00101xxx'b	;Set Postscaler to
9.MOVWF	OPTION	;desired WDT rate
10.BCF	STATUS, RPO	;Return to Bank 0

To change prescaler from the WDT to the TMR0 module, use the sequence shown in Example 6-2. This precaution must be taken even if the WDT is disabled.

EXAMPLE 6-2:

CHANGING PRESCALER (WDT→TIMER0)

	•	
CLRWDT		;Clear WDT and
		;prescaler
BSF	STATUS, RPO	
MOVLW	b'xxxx0xxx'	;Select TMR0, new
		prescale value and
		, plock gourgo
		,CIOCK SOULCE
MOVWF	OPTION REG	
BCF	STATUS, RPO	

TABLE 6-1: REGISTERS ASSOCIATED WITH TIMER0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Value on All Other RESETS
01h	TMR0	Timer0	module regi	ister						XXXX XXXX	uuuu uuuu
0Bh/8Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
81h	OPTION	RBPU	INTEDG	TOCS	TOSE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
85h	TRISA	_	_		TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	1 1111	1 1111

Legend: — = Unimplemented locations, read as '0', u = unchanged, x = unknown

Note: Shaded bits are not used by TMR0 module.

The code example in Example 7-1 depicts the steps required to configure the comparator module. RA3 and RA4 are configured as digital output. RA0 and RA1 are configured as the V- inputs and RA2 as the V+ input to both comparators.

EXAMPLE 7-1: INITIALIZING COMPARATOR MODULE

MOVLW	0x03	;Init comparator mode
MOVWF	CMCON	;CM<2:0> = 011
CLRF	PORTA	;Init PORTA
BSF	STATUS, RPO	;Select Bank1
MOVLW	0x07	;Initialize data direction
MOVWF	TRISA	;Set RA<2:0> as inputs
		;RA<4:3> as outputs
		;TRISA<7:5> always read `0'
BCF	STATUS, RPO	;Select Bank 0
CALL	DELAY 10	;10µs delay
MOVF	CMCON,F	;Read CMCONtoend change condition
BCF	PIR1,CMIF	;Clear pending interrupts
BSF	STATUS, RPO	;Select Bank 1
BSF	PIE1,CMIE	;Enable comparator interrupts
BCF	STATUS, RPO	;Select Bank 0
BSF	INTCON, PEIE	;Enable peripheral interrupts
BSF	INTCON, GIE	;Global interrupt enable

7.2 Comparator Operation

A single comparator is shown in Figure 7-2 along with the relationship between the analog input levels and the digital output. When the analog input at VIN+ is less than the analog input VIN-, the output of the comparator is a digital low level. When the analog input at VIN+ is greater than the analog input VIN-, the output of the comparator is a digital high level. The shaded areas of the output of the comparator in Figure 7-2 represent the uncertainty due to input offsets and response time.

7.3 Comparator Reference

An external or internal reference signal may be used depending on the comparator Operating mode. The analog signal that is present at VIN- is compared to the signal at VIN+, and the digital output of the comparator is adjusted accordingly (Figure 7-2).





7.3.1 EXTERNAL REFERENCE SIGNAL

When external voltage references are used, the comparator module can be configured to have the comparators operate from the same or different reference sources. However, threshold detector applications may require the same reference. The reference signal must be between VSs and VDD, and can be applied to either pin of the comparator(s).

7.3.2 INTERNAL REFERENCE SIGNAL

The comparator module also allows the selection of an internally generated voltage reference for the comparators. Section 10, Instruction Sets, contains a detailed description of the Voltage Reference Module that provides this signal. The internal reference signal is used when the comparators are in mode CM<2:0>=010 (Figure 7-1). In this mode, the internal voltage reference is applied to the VIN+ pin of both comparators.

7.6 Comparator Interrupts

The comparator interrupt flag is set whenever there is a change in the output value of either comparator. Software will need to maintain information about the status of the output bits, as read from CMCON<7:6>, to determine the actual change that has occurred. The CMIF bit, PIR1<6>, is the comparator interrupt flag. The CMIF bit must be RESET by clearing '0'. Since it is also possible to write a '1' to this register, a simulated interrupt may be initiated.

The CMIE bit (PIE1<6>) and the PEIE bit (INTCON<6>) must be set to enable the interrupt. In addition, the GIE bit must also be set. If any of these bits are clear, the interrupt is not enabled, though the CMIF bit will still be set if an interrupt condition occurs.

Note:	If a change in the CMCON register
	(C1OUT or C2OUT) should occur when a
	read operation is being executed (start of
	the Q2 cycle), then the CMIF (PIR1<6>)
	interrupt flag may not get set.

The user, in the interrupt service routine, can clear the interrupt in the following manner:

- a) Any read or write of CMCON. This will end the mismatch condition.
- b) Clear flag bit CMIF.

A mismatch condition will continue to set flag bit CMIF. Reading CMCON will end the mismatch condition and allow flag bit CMIF to be cleared.

7.7 Comparator Operation During SLEEP

When a comparator is active and the device is placed in SLEEP mode, the comparator remains active and the interrupt is functional if enabled. This interrupt will

Vdd ∆Vt = 0.6V RIC Rs < 10K Δικ **I**LEAKAGE CPIN VT = 0.6V ±500 nA 5 pF Vss Input Capacitance Legend CPIN = Threshold Voltage Vт = Leakage Current at the pin due to various junctions ILEAKAGE = = Interconnect Resistance RIC Rs = Source Impedance Analog Voltage VA =

FIGURE 7-4: ANALOG INPUT MODEL

wake up the device from SLEEP mode when enabled. While the comparator is powered-up, higher SLEEP currents than shown in the power-down current specification will occur. Each comparator that is operational will consume additional current as shown in the comparator specifications. To minimize power consumption while in SLEEP mode, turn off the comparators, CM<2:0> = 111, before entering SLEEP. If the device wakes up from SLEEP, the contents of the CMCON register are not affected.

7.8 Effects of a RESET

A device RESET forces the CMCON register to its RESET state. This forces the comparator module to be in the comparator RESET mode, CM<2:0> = 000. This ensures that all potential inputs are analog inputs. Device current is minimized when analog inputs are present at RESET time. The comparators will be powered-down during the RESET interval.

7.9 Analog Input Connection Considerations

A simplified circuit for an analog input is shown in Figure 7-4. Since the analog pins are connected to a digital output, they have reverse biased diodes to VDD and Vss. The analog input therefore, must be between Vss and VDD. If the input voltage deviates from this range by more than 0.6V in either direction, one of the diodes is forward biased and a latchup may occur. A maximum source impedance of $10 \ k\Omega$ is recommended for the analog sources. Any external component connected to an analog input pin, such as a capacitor or a Zener diode, should have very little leakage current.

EXAMPLE 8-1: VOLTAGE REFERENCE CONFIGURATION

MOVLW	0x02	; 4 Inputs Muxed
MOVWF	CMCON	; to 2 comps.
BSF	STATUS, RPO	; go to Bank 1
MOVLW	0x0F	; RA3-RA0 are
MOVWF	TRISA	; inputs
MOVLW	0xA6	; enable VREF
MOVWF	VRCON	; low range
		; set VR<3:0>=6
BCF	STATUS, RPO	; go to Bank O
CALL	DELAY10	; 10µs delay

8.2 Voltage Reference Accuracy/Error

The full range of VSS to VDD cannot be realized due to the construction of the module. The transistors on the top and bottom of the resistor ladder network (Figure 8-1) keep VREF from approaching VSS or VDD. The voltage reference is VDD derived and therefore, the VREF output changes with fluctuations in VDD. The tested absolute accuracy of the voltage reference can be found in Table 12-2.

8.3 Operation During SLEEP

When the device wakes up from SLEEP through an interrupt or a Watchdog Timer time-out, the contents of the VRCON register are not affected. To minimize current consumption in SLEEP mode, the voltage reference should be disabled.

8.4 Effects of a RESET

A device RESET disables the voltage reference by clearing bit VREN (VRCON<7>). This reset also disconnects the reference from the RA2 pin by clearing bit VROE (VRCON<6>) and selects the high voltage range by clearing bit VRR (VRCON<5>). The VREF value select bits, VRCON<3:0>, are also cleared.

8.5 Connection Considerations

The voltage reference module operates independently of the comparator module. The output of the reference generator may be connected to the RA2 pin if the TRISA<2> bit is set and the VROE bit, VRCON<6>, is set. Enabling the voltage reference output onto the RA2 pin with an input signal present will increase current consumption. Connecting RA2 as a digital output with VREF enabled will also increase current consumption.

The RA2 pin can be used as a simple D/A output with limited drive capability. Due to the limited drive capability, a buffer must be used in conjunction with the voltage reference output for external connections to VREF. Figure 8-2 shows an example buffering technique.

FIGURE 8-2: VOLTAGE REFERENCE OUTPUT BUFFER EXAMPLE

TABLE 8-1: REGISTERS ASSOCIATED WITH VOLTAGE REFERENCE

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value On POR	Value On All Other RESETS
9Fh	VRCON	VREN	VROE	VRR		VR3	VR2	VR1	VR0	000- 0000	000- 0000
1Fh	CMCON	C2OUT	C10UT	_	-	CIS	CM2	CM1	CM0	00 0000	00 0000
85h	TRISA	_	_	_	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	1 1111	1 1111

Note: - = Unimplemented, read as "0"

9.0 SPECIAL FEATURES OF THE CPU

Special circuits to deal with the needs of real-time applications are what sets a microcontroller apart from other processors. The PIC16C62X family has a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection.

These are:

- 1. OSC selection
- 2. RESET Power-on Reset (POR) Power-up Timer (PWRT) Oscillator Start-up Timer (OST) Brown-out Reset (BOR)
- 3. Interrupts
- 4. Watchdog Timer (WDT)
- 5. SLEEP
- 6. Code protection
- 7. ID Locations
- 8. In-Circuit Serial Programming™

The PIC16C62X devices have a Watchdog Timer which is controlled by configuration bits. It runs off its own RC oscillator for added reliability. There are two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in RESET until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay of 72 ms (nominal) on power-up only, designed to keep the part in RESET while the power supply stabilizes. There is also circuitry to RESET the device if a brown-out occurs, which provides at least a 72 ms RESET. With these three functions on-chip, most applications need no external RESET circuitry.

The SLEEP mode is designed to offer a very low current Power-down mode. The user can wake-up from SLEEP through external RESET, Watchdog Timer wake-up or through an interrupt. Several oscillator options are also made available to allow the part to fit the application. The RC oscillator option saves system cost, while the LP crystal option saves power. A set of configuration bits are used to select various options.

RLF	Rotate	Left f th	oug	h Car	ry	
Syntax:	[label]	RLF	f,d			I
Operands:	0 ≤ f ≤ 1 d ∈ [0,1	27]				
Operation:	See des	scription	belo	w		
Status Affected:	С					
Encoding:	00	1101	d	fff	ffff]
Description:	rotated the Carr is place 1, the re register	one bit to ry Flag. If d in the \ esult is sf 'f.	regis the 'd' is V reg ored	left th s 0, the gister. I back	are irough e result If 'd' is in	
Words:	1					
Cycles:	1					
Example	RLF	REG1,	0			
	Before Instruction					
		REG1	=	111	0 0110	
	After In	C	=	0		
	7 1101 111	REG1	=	111	0 0110	
		W	=	110	0 1100	
		С	=	1		

RRF	Rotate Right f through Carry							
Syntax:	[<i>label</i>] RRF f,d							
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in [0,1] \end{array}$							
Operation:	See desc	ription b	elow	,				
Status Affected:	С							
Encoding:	00	1100	df	ff	ffff			
Description:	The contents of register 'f' are rotated one bit to the right through the Carry Flag. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'.							
			Regis	ter f]->			
Words:	1							
Cycles:	1							
Example	RRF REG1 , 0							
	Before In	structior	ı					
		REG1	=	1110	0110			
	After Inst	ruction	=	U				
		REG1	=	1110	0110			
		W	=	0111	0011			
		C	=	0				

SLEEP

Syntax:	[lahal	SI FFF)			
Gyntax.]	OLLLI				
Operands:	None					
Operation:	$\begin{array}{l} 00h \rightarrow WDT, \\ 0 \rightarrow WDT \text{ prescaler,} \\ 1 \rightarrow \overline{TO}, \\ 0 \rightarrow PD \end{array}$					
Status Affected:	TO, PD					
Encoding:	00	0000	0110	0011		
Description:	The power-down STATUS bit, PD is cleared. Time-out STATUS bit, TO is set. Watch- dog Timer and its prescaler are cleared. The processor is put into SLEEP mode with the oscillator stopped. See Section 9.8 for more details					
Words:	1					
Cycles:	1					
Example:	SLEEP					

SUBLW	Subtract W from Literal	SUBWF	Subtract W from f
Syntax:	[<i>label</i>] SUBLW k	Syntax:	[<i>label</i>] SUBWF f,d
Operands:	$0 \le k \le 255$	Operands:	$0 \le f \le 127$
Operation:	$k - (W) \rightarrow (W)$		d ∈ [0,1]
Status Affected:	C, DC, Z	Operation: Status	(f) - (W) \rightarrow (dest) C, DC, Z
Encoding:	11 110x kkkk kkkk	Affected:	
Description:	The W register is subtracted (2's complement method) from the eight bit literal 'k'. The result is placed in the W register.	Encoding: Description:	000010dfffffffSubtract (2's complement method)W register from register 'f'. If 'd' is 0,the result is stored in the W register.If 'd' is 1, the result is stored head in
Words:	1		register 'f'.
Cycles:	1	Words:	1
Example 1:	SUBLW 0x02	Cycles:	1
	Before Instruction	Example 1:	SUBWF REG1,1
	W = 1 $C = ?$		Before Instruction
	After Instruction		REG1= 3
	W = 1		W = 2 C = ?
Example 2:	Before Instruction		After Instruction
Example 2.	W = 2 $C = ?$		REG1= 1 W = 2 C = 1; result is positive
	After Instruction	Example 2:	Before Instruction
	W = 0 C = 1; result is zero		REG1= 2 W = 2
Example 3:	Before Instruction		C = ?
	W = 3 C = ?		After Instruction REG1= 0
	After Instruction		W = 2
	W = 0xFF	Example 3	C = 1; result is zero Before Instruction
	C – 0, result is negative		REG1= 1 W = 2 C = ?
			After Instruction
			REG1= 0xFF W = 2 C = 0; result is negative

SWAPF	Swap Ni	bbles in	f				
Syntax:	[label] SWAPF f,d						
Operands:	$0 \le f \le 127$ d $\in [0,1]$						
Operation:	(f<3:0>) → (dest<7:4>), (f<7:4>) → (dest<3:0>)						
Status Affected:	None						
Encoding:	00	1110	dfff	Ē	ffff		
Description:	I he upper and lower nibbles of register 'f' are exchanged. If 'd' is 0, the result is placed in W register. If 'd' is 1, the result is placed in register 'f'.						
Words:	1						
Cycles:	1						
Example	SWAPF	REG,	0				
	Before In	struction					
		REG1	=	0xA5			
	After Inst	ruction					
		REG1 W	= =	0xA5 0x5A			

TRIS	Load TRIS Register						
Syntax:	[<i>label</i>] TRIS f						
Operands:	$5 \le f \le 7$						
Operation:	$(W) \rightarrow TRIS$ register f;						
Status Affected:	None						
Encoding:	00 0000 0110 Offf						
Description.	registers are readable and writable, the user can directly address them.						
Words:	1						
Cycles:	1						
Example							
	To maintain upward compatibil- ity with future PICmicro [®] prod- ucts, do not use this instruction.						

XORLW	Exclusiv	ve OR L	iteral v	vith W				
Syntax:	[label]	XORL	Wk					
Operands:	$0 \le k \le 2$	$0 \le k \le 255$						
Operation:	(W) .XO	(W) .XOR. $k \rightarrow (W)$						
Status Affected:	Z	Z						
Encoding:	11	1010	kkkk	: kkkk				
Description:	The cont are XOR literal 'k'. the W re	The contents of the W register are XOR'ed with the eight bit literal 'k'. The result is placed in the W register.						
Words:	1							
Cycles:	1							
Example:	XORLW	0xAF						
	Before Ir	nstructio	n					
		W =	0xB	5				
	After Ins	truction						
		W =	0x1A	Ą				
XORWF	Exclusiv	e OR W	with f					
Syntax:	[label]	XORWF	f,d					
Operands:	$\begin{array}{l} 0 \leq f \leq 12 \\ d \in [0,1] \end{array}$	7						
Operation:	(W) .XOR	$R.(f) \to ($	dest)					
Status Affected:	Z							
Encoding:	00	0110	dfff	ffff				
Description:	Exclusive W registe 0, the res register. I stored ba	OR the r with re ult is sto f 'd' is 1, ck in reg	conten gister 'f red in t the res gister 'f'	ts of the r. If 'd' is the W sult is				
Words:	1							
Cycles:	1							
Example	XORWF	REG	1					
	Before In:	struction	I					
		REG W	= (0xAF 0xB5				
	After Inst	ruction						
		REG W	= (0x1A 0xB5				



FIGURE 12-8: PIC16CR62XA VOLTAGE-FREQUENCY GRAPH, -40°C \leq TA \leq 0°C, +70°C \leq TA \leq +125°C







12.1 DC Characteristics: PIC16C62X-04 (Commercial, Industrial, Extended) PIC16C62X-20 (Commercial, Industrial, Extended) PIC16LC62X-04 (Commercial, Industrial, Extended) (CONT.)

PIC16C62X				Standard Operating Conditions (unless otherwise stated)Operating temperature -40° C $\leq TA \leq +85^{\circ}$ C for industrial and 0° C $\leq TA \leq +70^{\circ}$ C for commercial and -40° CStandard Operating Conditions (unless otherwise stated)Operating temperature -40° C $\leq TA \leq +85^{\circ}$ C for industrial and 0° COperating temperature -40° C $\leq TA \leq +85^{\circ}$ C for industrial and 0° C					
	OULA		Opera	-40° C \leq TA \leq +70^{\circ}C for commercial a -40°C \leq TA \leq +125°C for extended Operating voltage VDD range is the PIC16C62X range.					
Param . No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions		
D022 D022A D023 D023A D022A D022A D022A D023	ΔIWDT ΔIBOR ΔICOM P ΔIVREF ΔIWDT ΔIBOR ΔICOM P	WDT Current ⁽⁵⁾ Brown-out Reset Current ⁽⁵⁾ Comparator Current for each Comparator ⁽⁵⁾ VREF Current ⁽⁵⁾ WDT Current ⁽⁵⁾ Brown-out Reset Current ⁽⁵⁾ Comparator Current for each Comparator ⁽⁵⁾	 	6.0 350 — 6.0 350 —	20 25 425 100 300 15 425 100	μΑ μΑ μΑ μΑ μΑ μΑ	$VDD=4.0V$ $(125^{\circ}C)$ $BOD \text{ enabled, } VDD = 5.0V$ $VDD = 4.0V$ $VDD = 4.0V$ $VDD=3.0V$ $BOD \text{ enabled, } VDD = 5.0V$ $VDD = 3.0V$		
D023A	Δ IVREF	VREF Current ⁽⁵⁾	—	_	300	μA	VDD = 3.0V		
1A	Fosc	LP Oscillator Operating Frequency RC Oscillator Operating Frequency XT Oscillator Operating Frequency HS Oscillator Operating Frequency	0 0 0 0		200 4 4 20	kHz MHz MHz MHz	All temperatures All temperatures All temperatures All temperatures		
1A	Fosc	LP Oscillator Operating Frequency RC Oscillator Operating Frequency XT Oscillator Operating Frequency HS Oscillator Operating Frequency	0 0 0 0		200 4 4 20	kHz MHz MHz MHz	All temperatures All temperatures All temperatures All temperatures		

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in Active Operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tri-stated, pulled to VDD,

MCLR = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or VSS.

4: For RC osc configuration, current through REXT is not included. The current through the resistor can be estimated by the formula: Ir = VDD/2REXT (mA) with REXT in kΩ.

5: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.













14.1 Package Marking Information



Legenc	I: XXX Y YY WW NNN	Customer specific information* Year code (last digit of calendar year) Year code (last 2 digits of calendar year) Week code (week of January 1 is week '01') Alphanumeric traceability code
Note:	In the even be carried for custom	nt the full Microchip part number cannot be marked on one line, it will over to the next line thus limiting the number of available characters her specific information.

* Standard PICmicro device marking consists of Microchip part number, year code, week code, and traceability code. For PICmicro device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

APPENDIX A: ENHANCEMENTS

The following are the list of enhancements over the PIC16C5X microcontroller family:

- Instruction word length is increased to 14 bits. This allows larger page sizes both in program memory (4K now as opposed to 512 before) and register file (up to 128 bytes now versus 32 bytes before).
- 2. A PC high latch register (PCLATH) is added to handle program memory paging. PA2, PA1, PA0 bits are removed from STATUS register.
- 3. Data memory paging is slightly redefined. STATUS register is modified.
- Four new instructions have been added: RETURN, RETFIE, ADDLW, and SUBLW.
 Two instructions TRIS and OPTION are being phased out, although they are kept for compatibility with PIC16C5X.
- 5. OPTION and TRIS registers are made addressable.
- 6. Interrupt capability is added. Interrupt vector is at 0004h.
- 7. Stack size is increased to 8 deep.
- 8. RESET vector is changed to 0000h.
- RESET of all registers is revisited. Five different RESET (and wake-up) types are recognized. Registers are reset differently.
- 10. Wake-up from SLEEP through interrupt is added.
- 11. Two separate timers, Oscillator Start-up Timer (OST) and Power-up Timer (PWRT) are included for more reliable power-up. These timers are invoked selectively to avoid unnecessary delays on power-up and wake-up.
- 12. PORTB has weak pull-ups and interrupt-onchange feature.
- 13. Timer0 clock input, T0CKI pin is also a port pin (RA4/T0CKI) and has a TRIS bit.
- 14. FSR is made a full 8-bit register.
- 15. "In-circuit programming" is made possible. The user can program PIC16CXX devices using only five pins: VDD, VSS, VPP, RB6 (clock) and RB7 (data in/out).
- PCON STATUS register is added with a Poweron-Reset (POR) STATUS bit and a Brown-out Reset STATUS bit (BOD).
- 17. Code protection scheme is enhanced such that portions of the program memory can be protected, while the remainder is unprotected.
- 18. PORTA inputs are now Schmitt Trigger inputs.
- 19. Brown-out Reset reset has been added.
- 20. Common RAM registers F0h-FFh implemented in bank1.

APPENDIX B: COMPATIBILITY

To convert code written for PIC16C5X to PIC16CXX, the user should take the following steps:

- 1. Remove any program memory page select operations (PA2, PA1, PA0 bits) for CALL, GOTO.
- 2. Revisit any computed jump operations (write to PC or add to PC, etc.) to make sure page bits are set properly under the new scheme.
- 3. Eliminate any data memory page switching. Redefine data variables to reallocate them.
- 4. Verify all writes to STATUS, OPTION, and FSR registers since these have changed.
- 5. Change RESET vector to 0000h.

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