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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	13
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	18-DIP (0.300", 7.62mm)
Supplier Device Package	18-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c622a-04i-p

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

## 2.0 PIC16C62X DEVICE VARIETIES

A variety of frequency ranges and packaging options are available. Depending on application and production requirements, the proper device option can be selected using the information in the PIC16C62X Product Identification System section at the end of this data sheet. When placing orders, please use this page of the data sheet to specify the correct part number.

### 2.1 UV Erasable Devices

The UV erasable version, offered in CERDIP package, is optimal for prototype development and pilot programs. This version can be erased and reprogrammed to any of the Oscillator modes.

Microchip's PICSTART<sup>®</sup> and PRO MATE<sup>®</sup> programmers both support programming of the PIC16C62X.

Note: Microchip does not recommend code protecting windowed devices.

#### 2.2 One-Time-Programmable (OTP) Devices

The availability of OTP devices is especially useful for customers who need the flexibility for frequent code updates and small volume applications. In addition to the program memory, the configuration bits must also be programmed.

#### 2.3 Quick-Turnaround-Production (QTP) Devices

Microchip offers a QTP programming service for factory production orders. This service is made available for users who chose not to program a medium to high quantity of units and whose code patterns have stabilized. The devices are identical to the OTP devices, but with all EPROM locations and configuration options already programmed by the factory. Certain code and prototype verification procedures apply before production shipments are available. Please contact your Microchip Technology sales office for more details.

#### 2.4 Serialized Quick-Turnaround-Production<sup>sm</sup> (SQTP<sup>sm</sup>) Devices

Microchip offers a unique programming service where a few user-defined locations in each device are programmed with different serial numbers. The serial numbers may be random, pseudo-random or sequential.

Serial programming allows each device to have a unique number, which can serve as an entry-code, password or ID number.

Name	DIP/SOIC Pin #	SSOP Pin #	I/O/P Type	Buffer Type	Description
OSC1/CLKIN	16	18	I	ST/CMOS	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	15	17	0	_	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. In RC mode, OSC2 pin out- puts CLKOUT, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
MCLR/Vpp	4	4	I/P	ST	Master Clear (Reset) input/programming voltage input. This pin is an Active Low Reset to the device.
					PORTA is a bi-directional I/O port.
RA0/AN0	17	19	I/O	ST	Analog comparator input
RA1/AN1	18	20	I/O	ST	Analog comparator input
RA2/AN2/VREF	1	1	I/O	ST	Analog comparator input or VREF output
RA3/AN3	2	2	I/O	ST	Analog comparator input /output
RA4/T0CKI	3	3	I/O	ST	Can be selected to be the clock input to the Timer0 timer/counter or a comparator output. Output is open drain type.
					PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs.
RB0/INT	6	7	I/O	TTL/ST <sup>(1)</sup>	RB0/INT can also be selected as an external interrupt pin.
RB1	7	8	I/O	TTL	
RB2	8	9	I/O	TTL	
RB3	9	10	I/O	TTL	
RB4	10	11	I/O	TTL	Interrupt-on-change pin.
RB5	11	12	I/O	TTL	Interrupt-on-change pin.
RB6	12	13	I/O	TTL/ST <sup>(2)</sup>	Interrupt-on-change pin. Serial programming clock.
RB7	13	14	I/O	TTL/ST <sup>(2)</sup>	Interrupt-on-change pin. Serial programming data.
Vss	5	5,6	Р	_	Ground reference for logic and I/O pins.
VDD	14	15,16	Р	_	Positive supply for logic and I/O pins.
Legend:	O = out — = No	put t used	I/O = inp	ut/output	P = power ST = Schmitt Trigger input

TABLE 3-1:	PIC16C62X PINOUT DESCRIPTIC	)N

TTL = TTL input

**Note** 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.

2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.

#### FIGURE 4-4: DATA MEMORY MAP FOR THE PIC16C620/621

File Address	3		File Address
00h	INDF <sup>(1)</sup>	INDF <sup>(1)</sup>	80h
01h	TMR0	OPTION	81h
02h	PCL	PCL	82h
03h	STATUS	STATUS	83h
04h	FSR	FSR	84h
05h	PORTA	TRISA	85h
06h	PORTB	TRISB	86h
07h			87h
08h			88h
09h			89h
0Ah	PCLATH	PCLATH	8Ah
0Bh	INTCON	INTCON	8Bh
0Ch	PIR1	PIE1	8Ch
0Dh			8Dh
0Eh		PCON	8Eh
0Fh			8Fh
10h			90h
11h			91h
12h			92h
13h			93h
14h			94h
15h			95h
16h			96h
17h			97h
18h			98h
19h			99h
1Ah			9Ah
1Bh			9Bh
1Ch			9Ch
1Dh			9Dh
1Eh			9Eh
1Fh	CMCON	VRCON	9Fh
20h	Osmanal		A0h
	Purpose		
6Eb	Register		
70n			
Į			_
7Fh	Donk 0	Dorld 1	FFh
	Dank U	Bank T	
Unimp	plemented data me	mory locations, r	ead as '0'.
Note 1:	Not a physical re	egister.	

# FIGURE 4-5:

#### DATA MEMORY MAP FOR THE PIC16C622

File Address	3		File Address					
00h	INDF <sup>(1)</sup>	INDF <sup>(1)</sup>	80h					
01h	TMR0	OPTION	81h					
02h	PCL	PCL	82h					
03h	STATUS	STATUS	83h					
04h	FSR	FSR	84h					
05h	PORTA	TRISA	85h					
06h	PORTB	TRISB	86h					
07h			87h					
08h			88h					
09h			89h					
0Ah	PCLATH	PCLATH	8Ah					
0Bh	INTCON	INTCON	8Bh					
0Ch	PIR1	PIE1	8Ch					
0Dh			8Dh					
0Eh		PCON	8Eh					
0Fh			8Fh					
10h			90h					
11h			91h					
12h			92h					
13h			93h					
14h			94h					
15h			95h					
16h			96h					
17h			97h					
18h			98h					
19h			99h					
1Ah			9Ah					
1Bh			9Bh					
1Ch			9Ch					
1Dh			9Dh					
1Eh			9Eh					
1Fh	CMCON	VRCON	9Fh					
20h			A0h					
	General	General	7.011					
	Purpose Register	Purpose Register						
	rtogiotor	rtogiotor	BFh					
			C0h					
7Fh			FFh					
,,,,,	Bank 0	Bank 1						
Unimp	plemented data me	mory locations, re	ead as '0'.					
Note 1:	Not a physical m	aistor						
Note 1: Not a physical register.								

#### 4.2.2.1 STATUS Register

The STATUS register, shown in Register 4-1, contains the arithmetic status of the ALU, the RESET status and the bank select bits for data memory.

The STATUS register can be the destination for any instruction, like any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the TO and PD bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, CLRF STATUS will clear the upper-three bits and set the Z bit. This leaves the STATUS register as 000uuluu (where u = unchanged).

It is recommended, therefore, that only BCF, BSF, SWAPF and MOVWF instructions are used to alter the STATUS register, because these instructions do not affect any STATUS bit. For other instructions not affecting any STATUS bits, see the "Instruction Set Summary".

- Note 1: The IRP and RP1 bits (STATUS<7:6>) are not used by the PIC16C62X and should be programmed as '0'. Use of these bits as general purpose R/W bits is NOT recommended, since this may affect upward compatibility with future products.
  - 2: The <u>C and DC bits</u> operate as a Borrow and Digit Borrow out bit, respectively, in subtraction. See the SUBLW and SUBWF instructions for examples.

#### REGISTER 4-1: STATUS REGISTER (ADDRESS 03H OR 83H)

Reserved	Reserved	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x		
IRP	RP1	RP0	TO	PD	Z	DC	С		
bit 7	•						bit 0		
IRP: Regis	ster Bank Sele	ect bit (used	d for indirect	addressing	)				
1 = Bank 2	2, 3 (100h - 1F	FFh)							
0 = Bank ( The IRP hi	), 1 (UUN - FFI it is reserved	n) on the PIC:	16C62X alw	/avs maintai	in this hit cle	ar			
RP<1·0>	Register Banl	C Select hits	s (used for c	lirect addres	sina)				
01 = Bank	1 (80h - FFh	)			Joinig)				
00 = Bank	0 (00h - 7Fh)	)							
Each bank	is 128 bytes.	The RP1 b	oit is reserve	ed on the Pl	C16C62X; a	lways maint	ain this bit		
clear.									
IU: Time-o			tion of at t	I Dinatruati	<b>~</b> ~				
1 = Alter p 0 = A WD1	ower-up, сък Г time-out осо	curred		EP Instructi	on				
PD: Power	r-down bit								
1 = After p	ower-up or by	/ the CLRWI	DT instructio	n					
0 = By exe	ecution of the	SLEEP inst	ruction						
Z: Zero bit									
1 = The re	sult of an ariti	hmetic or lo	gic operatio	n is zero	<b>`</b>				
	suit of an and				) instructions	)(for borrow)	the polarity		
is reversed)									
1 = A carry-out from the 4th low order bit of the result occurred									
0 = No carry-out from the 4th low order bit of the result									
C: Carry/b	orrow bit (ADI	DWF, ADDI	W,SUBLW,S	SUBWF instr	uctions)				
1 = A carry-out from the Most Significant bit of the result occurred									
0 = No car	ry-out from th	ie Most Sig	nificant dit o		occurrea	مرامي مراما			
Note: For porrow the polarity is reversed. A subtraction is executed by adding the two's									
	loaded with e	ither the high	gh or low or	der bit of the	e source reg	ister.	o, and bit lo		
Legend:									
R = Reada	able bit	VV = VV	ritable bit	U = Unin	nplemented	bit, read as	'0'		
- n = Value	e at POR	'1' = Bi	t is set	'0' = Bit i	s cleared	x = Bit is u	nknown		
	Reserved           IRP           bit 7           IRP: Regis           1 = Bank 2           0 = Bank 0           The IRP bit           RP<1:0>:           01 = Bank 0           RP<1:0>:           01 = Bank 0           Bank 0           RP<1:0>:           01 = Bank 0           RP<1:0>:           01 = Bank 0           RP<1:0>:           0 = Bank 0           I = After p           0 = A WD1           PD: Power           1 = After p           0 = By exee           Z: Zero bit           1 = The re           0 = The re           DC: Digit c           is reversed           1 = A carry           0 = No car           C: Carry/b           1 = A carry           0 = No car           Note:           Legend:           R = Reada           - n = Value	ReservedReservedIRPRP1bit 7IRP: Register Bank Sele1 = Bank 2, 3 (100h - 1f0 = Bank 0, 1 (00h - FFIThe IRP bit is reservedRP<1:0>: Register Bank01 = Bank 1 (80h - FFh)00 = Bank 0 (00h - 7Fh)Each bank is 128 bytes.clear.TO: Time-out bit1 = After power-up, CLR0 = A WDT time-out occPD: Power-down bit1 = After power-up or by0 = By execution of theZ: Zero bit1 = The result of an arith0 = The result of an arith0 = The result of an arith0 = No carry-out from the0 = No carry-out from the1 = A carry-out from the0 = No carry-out from the0 = No carry-out from the1 = A carry-out from the0 = No carry-out from the0 = No carry-out from the0 = No carry-out from the1 = A carry out from the1 = A carry out from the<	ReservedRevolR/W-0IRPRP1RP0bit 7IRP: Register Bank Select bit (used1 = Bank 2, 3 (100h - 1FFh)0 = Bank 0, 1 (00h - FFh)The IRP bit is reserved on the PIC? <b>RP&lt;1:0&gt;</b> : Register Bank Select bits01 = Bank 1 (80h - FFh)00 = Bank 0 (00h - 7Fh)Each bank is 128 bytes. The RP1 bitclear. <b>TO</b> : Time-out bit1 = After power-up, CLRWDT instruct0 = A WDT time-out occurred <b>PD</b> : Power-down bit1 = After power-up or by the CLRWD0 = By execution of the SLEEP inst <b>Z</b> : Zero bit1 = The result of an arithmetic or lo0 = The result of an arithmetic or lo0 = The result of an arithmetic or lo0 = C: Digit carry/borrow bit (ADDWF, is reversed)1 = A carry-out from the 4th low or0 = No carry-out from the Most Signi0 = No carry-out from the Most Signi <td>ReservedR/W-0R-1IRPRP1RP0TObit 7IRP: Register Bank Select bit (used for indirect1 = Bank 2, 3 (100h - 1FFh)0 = Bank 0, 1 (00h - FFh)The IRP bit is reserved on the PIC16C62X; alwRP&lt;1:0&gt;: Register Bank Select bits (used for d)01 = Bank 1 (80h - FFh)00 = Bank 0 (00h - 7Fh)Each bank is 128 bytes. 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The RP1 bit is reserved on the PIC clear.         TO:       Time-out bit         1 = After power-up, CLRWDT instruction, or SLEEP instruction 0 = A WDT time-out occurred         PD:       Power-down bit         1 = After power-up or by the CLRWDT instruction 0 = By execution of the SLEEP instruction         2: Zero bit       1 = The result of an arithmetic or logic operation is zero 0 = The result of an arithmetic or logic operation is not zero         DC:       Digit carry/borrow bit (ADDWF, ADDLW, SUBLW, SUBWF is reversed)         1 = A carry-out from the 4th low order bit of the result occur 0 = No carry-out from the Most Significant bit of the result of 0 = No carry-out from the Most Significant bit of the result of 0 = No carry-out from the Most Significant bit of the result of 0 = No carry-out from the Most Significant bit of the result of 0 = No carry-out from the Most Significant bit of the result of 0 = No carry-out from the Most Significant bit of the result of 0 = No carry-out from the Most Significant bit of the result of 0 = No carry-out from the Most Significant bit of the result of 0 =</td> <td>Reserved         Reserved         R/W-0         R-1         R-1         R/W-x           IRP         RP1         RP0         TO         PD         Z           bit 7         IRP: Register Bank Select bit (used for indirect addressing)         1         = Bank 2, 3 (100h - 1FFh)         0         = Bank 0, 1 (00h - FFh)           The IRP bit is reserved on the PIC16C62X; always maintain this bit cle         RP&lt;1:0&gt;: Register Bank Select bits (used for direct addressing)           01 = Bank 1 (80h - FFh)         0         = Bank 0 (00h - 7Fh)         Each bank is 128 bytes. The RP1 bit is reserved on the PIC16C62X; a clear.           TO: Time-out bit         1         = After power-up, CLRWDT instruction, or SLEEP instruction         0           0 = A WDT time-out occurred         PD: Power-down bit         1         = After power-up or by the CLRWDT instruction           0 = By execution of the SLEEP instruction         2         Zero bit         1         = The result of an arithmetic or logic operation is zero           0 = The result of an arithmetic or logic operation is not zero         DC: Digit carry/borrow bit (ADDWF, ADDLW, SUBLW, SUBWF instructions)           1 = A carry-out from the 4th low order bit of the result         C: Carry/borrow bit (ADDWF, ADDLW, SUBLW, SUBWF instructions)           1 = A carry-out from the Most Significant bit of the result occurred         0 = No carry-out from the Most Significant bit of the result occurred</td> <td>Reserved       Reserved       R/W-0       R-1       R-1       R/W-x       R/W-x         IRP       RP1       RP0       TO       PD       Z       DC         bit 7         IRP: Register Bank Select bit (used for indirect addressing)       1       Bank 2, 3 (100h - 1FFh)         0       Bank 0, 1 (00h - FFh)       The IRP bit is reserved on the PIC16C62X; always maintain this bit clear.         RP&lt;1:0&gt;: Register Bank Select bits (used for direct addressing)       01       = Bank 1 (80h - FFh)         00       Bank 0 (00h - 7Fh)       Each bank is 128 bytes. The RP1 bit is reserved on the PIC16C62X; always maintain thicear.         TO: Time-out bit       1       After power-up, CLRWDT instruction, or SLEEP instruction       0         0       = A WDT time-out occurred       PD: Power-down bit       1         1 = After power-up or by the CLRWDT instruction       0       = By execution of the SLEEP instruction         2: Zero bit       1       The result of an arithmetic or logic operation is zero       0         1 = The result of an arithmetic or logic operation is not zero       DC       DC         D: Digit carry/borrow bit (ADDWF, ADDLW, SUBLW, SUBWF instructions)(for borrow is reversed)       1       A carry-out from the 4th low order bit of the result occurred         0 = No carry-out from the Most Significant bit of the result occurred</td>	ReservedR/W-0R-1IRPRP1RP0TObit 7IRP: Register Bank Select bit (used for indirect1 = Bank 2, 3 (100h - 1FFh)0 = Bank 0, 1 (00h - FFh)The IRP bit is reserved on the PIC16C62X; alwRP<1:0>: Register Bank Select bits (used for d)01 = Bank 1 (80h - FFh)00 = Bank 0 (00h - 7Fh)Each bank is 128 bytes. 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The RP1 bit is reserved on the PIC16C62X; a clear.           TO: Time-out bit         1         = After power-up, CLRWDT instruction, or SLEEP instruction         0           0 = A WDT time-out occurred         PD: Power-down bit         1         = After power-up or by the CLRWDT instruction           0 = By execution of the SLEEP instruction         2         Zero bit         1         = The result of an arithmetic or logic operation is zero           0 = The result of an arithmetic or logic operation is not zero         DC: Digit carry/borrow bit (ADDWF, ADDLW, SUBLW, SUBWF instructions)           1 = A carry-out from the 4th low order bit of the result         C: Carry/borrow bit (ADDWF, ADDLW, SUBLW, SUBWF instructions)           1 = A carry-out from the Most Significant bit of the result occurred         0 = No carry-out from the Most Significant bit of the result occurred	Reserved       Reserved       R/W-0       R-1       R-1       R/W-x       R/W-x         IRP       RP1       RP0       TO       PD       Z       DC         bit 7         IRP: Register Bank Select bit (used for indirect addressing)       1       Bank 2, 3 (100h - 1FFh)         0       Bank 0, 1 (00h - FFh)       The IRP bit is reserved on the PIC16C62X; always maintain this bit clear.         RP<1:0>: Register Bank Select bits (used for direct addressing)       01       = Bank 1 (80h - FFh)         00       Bank 0 (00h - 7Fh)       Each bank is 128 bytes. The RP1 bit is reserved on the PIC16C62X; always maintain thicear.         TO: Time-out bit       1       After power-up, CLRWDT instruction, or SLEEP instruction       0         0       = A WDT time-out occurred       PD: Power-down bit       1         1 = After power-up or by the CLRWDT instruction       0       = By execution of the SLEEP instruction         2: Zero bit       1       The result of an arithmetic or logic operation is zero       0         1 = The result of an arithmetic or logic operation is not zero       DC       DC         D: Digit carry/borrow bit (ADDWF, ADDLW, SUBLW, SUBWF instructions)(for borrow is reversed)       1       A carry-out from the 4th low order bit of the result occurred         0 = No carry-out from the Most Significant bit of the result occurred		

#### 5.2 PORTB and TRISB Registers

PORTB is an 8-bit wide, bi-directional port. The corresponding data direction register is TRISB. A '1' in the TRISB register puts the corresponding output driver in a High Impedance mode. A '0' in the TRISB register puts the contents of the output latch on the selected pin(s).

Reading PORTB register reads the status of the pins, whereas writing to it will write to the port latch. All write operations are read-modify-write operations. So a write to a port implies that the port pins are first read, then this value is modified and written to the port data latch.

Each of the PORTB pins has a weak internal pull-up ( $\approx 200 \ \mu A \ typical$ ). A single control bit can turn on all the pull-ups. This is done by clearing the RBPU (OPTION<7>) bit. The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on Power-on Reset.

Four of PORTB's pins, RB<7:4>, have an interrupt on change feature. Only pins configured as inputs can cause this interrupt to occur (e.g., any RB<7:4> pin configured as an output is excluded from the interrupt on change comparison). The input pins (of RB<7:4>) are compared with the old value latched on the last read of PORTB. The "mismatch" outputs of RB<7:4> are OR'ed together to generate the RBIF interrupt (flag latched in INTCON<0>).

#### FIGURE 5-5: BLOCK DIAGRAM OF RB<7:4> PINS



This interrupt can wake the device from SLEEP. The user, in the interrupt service routine, can clear the interrupt in the following manner:

- a) Any read or write of PORTB. This will end the mismatch condition.
- b) Clear flag bit RBIF.

A mismatch condition will continue to set flag bit RBIF. Reading PORTB will end the mismatch condition and allow flag bit RBIF to be cleared.

This interrupt on mismatch feature, together with software configurable pull-ups on these four pins allow easy interface to a key pad and make it possible for wake-up on key-depression. (See AN552, "Implementing Wake-Up on Key Strokes.)

Note:	If a change on the I/O pin should occur						
	when the read operation is being executed						
	(start of the Q2 cycle), then the RBIF inter-						
	rupt flag may not get set.						

The interrupt-on-change feature is recommended for wake-up on key depression operation and operations where PORTB is only used for the interrupt on change feature. Polling of PORTB is not recommended while using the interrupt-on-change feature.





#### 6.3.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control (i.e., it can be changed "on-the-fly" during program execution). To avoid an unintended device RESET, the following instruction sequence (Example 6-1) must be executed when changing the prescaler assignment from Timer0 to WDT.)

#### EXAMPLE 6-1: CHANGING PRESCALER (TIMER0→WDT)

	-	
1.BCF	STATUS, RPO	;Skip if already in ;Bank 0
2.CLRWDT		;Clear WDT
3.CLRF	TMR0	;Clear TMR0 & Prescaler
4.BSF	STATUS, RPO	;Bank 1
5.MOVLW	'00101111'b;	;These 3 lines (5, 6, 7)
6.MOVWF	OPTION	;are required only if ;desired PS<2:0> are
7.CLRWDT		;000 or 001
8.MOVLW	'00101xxx'b	;Set Postscaler to
9.MOVWF	OPTION	;desired WDT rate
10.BCF	STATUS, RPO	;Return to Bank 0

To change prescaler from the WDT to the TMR0 module, use the sequence shown in Example 6-2. This precaution must be taken even if the WDT is disabled.

### EXAMPLE 6-2:

#### CHANGING PRESCALER (WDT→TIMER0)

	•	
CLRWDT		;Clear WDT and
		;prescaler
BSF	STATUS, RPO	
MOVLW	b'xxxx0xxx'	;Select TMR0, new
		prescale value and
		, glock gourgo
		,CIOCK SOULCE
MOVWF	OPTION REG	
BCF	STATUS, RPO	

#### TABLE 6-1: REGISTERS ASSOCIATED WITH TIMER0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Value on All Other RESETS
01h	h TMR0 Timer0 module register									XXXX XXXX	uuuu uuuu
0Bh/8Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
81h	OPTION	RBPU	INTEDG	TOCS	TOSE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
85h	TRISA	_	_		TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	1 1111	1 1111

Legend: — = Unimplemented locations, read as '0', u = unchanged, x = unknown

**Note:** Shaded bits are not used by TMR0 module.

NOTES:

#### 7.4 Comparator Response Time

Response time is the minimum time, after selecting a new reference voltage or input source, before the comparator output has a valid level. If the internal reference is changed, the maximum delay of the internal voltage reference must be considered when using the comparator outputs. Otherwise the maximum delay of the comparators should be used (Table 12-2).

#### 7.5 Comparator Outputs

The comparator outputs are read through the CMCON register. These bits are read only. The comparator outputs may also be directly output to the RA3 and RA4 I/O pins. When the CM<2:0> = 110, multiplexors in the output path of the RA3 and RA4 pins will switch and the output of each pin will be the unsynchronized output of the comparator. The uncertainty of each of the comparators is related to the input offset voltage and the response time given in the specifications. Figure 7-3 shows the comparator output block diagram.

The TRISA bits will still function as an output enable/ disable for the RA3 and RA4 pins while in this mode.

- Note 1: When reading the PORT register, all pins configured as analog inputs will read as a '0'. Pins configured as digital inputs will convert an analog input according to the Schmitt Trigger input specification.
  - 2: Analog levels on any pin that is defined as a digital input may cause the input buffer to consume more current than is specified.

#### FIGURE 7-3: COMPARATOR OUTPUT BLOCK DIAGRAM



#### 9.1 Configuration Bits

The configuration bits can be programmed (read as '0') or left unprogrammed (read as '1') to select various device configurations. These bits are mapped in program memory location 2007h.

The user will note that address 2007h is beyond the user program memory space. In fact, it belongs to the special test/configuration memory space (2000h - 3FFFh), which can be accessed only during programming.

#### REGISTER 9-1: CONFIGURATION WORD (ADDRESS 2007h)

CP1	CP0 (2)	CP1	CP0 (2)	CP1	CP0 (2)		BODEN	CP1	CP0 <sup>(2)</sup>	PWRTE	WDTE	F0SC1	F0SC0
bit 13							Į		ļ		<u> </u>	ļ	bit 0
bit 13-8 5-4:	<ul> <li>3-8, CP&lt;1:0&gt;: Code protection bit pairs <sup>(2)</sup> Code protection for 2K program memory 11 = Program memory code protection off 10 = 0400h-07FFh code protected 01 = 0200h-07FFh code protected 00 = 0000h-07FFh code protected</li> <li>Code protection for 1K program memory 11 = Program memory code protection off 10 = Program memory code protection off 10 = Program memory code protection off 01 = 0200h-03FFh code protected 00 = 0000h 03FFh code protected</li> </ul>												
	Cod 11 = 10 = 01 = 00 =	e protec = Progra = Progra = Progra = 0000h-	ction for ( m memo m memo m memo -01FFh c	).5K prop ory code ory code ory code ode prot	gram me protectio protectio protectio	emory on off on off on off							
bit 7	Uniı	npleme	e <b>nted</b> : Re	ead as 'C	)'								
bit 6	BOI	DEN: Br	own-out	Reset E	nable bit	(1)							
	1 = 0 =	BOR en BOR dis	abled sabled										
bit 3	<b>PWI</b> 1 = 0 =	<b>RTE</b> : Po PWRT c PWRT e	ower-up T disabled enabled	īmer En	able bit	(1, 3)							
bit 2	<b>WD</b> 1 = ' 0 = '	TE: Wat WDT en WDT dis	chdog Ti nabled sabled	mer Ena	ble bit								
bit 1-0	FOS	C1:FO	SCO: Oso	cillator S	election	bits							
	11 - 10 = 01 = 00 =	11 = RC oscillator 10 = HS oscillator 01 = XT oscillator 00 = LP oscillator											
	Note	e <b>1:</b> Er va er 2: או	nabling B alue of bit nabled.	PWRTE	it Reset E. Ensur	automa e the Po we to be	itically ena ower-up Ti	bles Pov mer is e	wer-up T nabled a	imer (PWF nytime Bro	RT) rega own-out l	rdless of Detect R	the eset is
		lis 3: Ui	ited. nprogram	nmed pa	rts defai	ult the F	Power-up T	imer dis	abled.				
Logond	1.												
R = Re	ı. adable b	it		W = 1	Writable	bit	U =	Unimple	emented	bit, read a	s '0'		

#### 9.2 Oscillator Configurations

#### 9.2.1 OSCILLATOR TYPES

The PIC16C62X devices can be operated in four different oscillator options. The user can program two configuration bits (FOSC1 and FOSC0) to select one of these four modes:

- LP Low Power Crystal
- XT Crystal/Resonator
- HS High Speed Crystal/Resonator
- RC Resistor/Capacitor

# 9.2.2 CRYSTAL OSCILLATOR / CERAMIC RESONATORS

In XT, LP or HS modes, a crystal or ceramic resonator is connected to the OSC1 and OSC2 pins to establish oscillation (Figure 9-1). The PIC16C62X oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in XT, LP or HS modes, the device can have an external clock source to drive the OSC1 pin (Figure 9-2).

#### FIGURE 9-1: CRYSTAL OPERATION (OR CERAMIC RESONATOR) (HS, XT OR LP OSC CONFIGURATION)



See Table 9-1 and Table 9-2 for recommended values of C1 and C2.

**Note:** A series resistor may be required for AT strip cut crystals.

#### FIGURE 9-2: EXTERNAL CLOCK INPUT OPERATION (HS, XT OR LP OSC



# TABLE 9-1:CAPACITOR SELECTION FOR<br/>CERAMIC RESONATORS

R	anges Chara	~[]						
Mode	Freq	<b>OSC2(C2)</b>						
ХТ	455 kHz 2.0 MHz 4.0 MHz	22 - 100 pF 15 - 68 pF 15 - 68 pF	82 - 100 pF 15 - 68 pF 15 - 68 pF					
HS	8.0 MHz 16.0 MHz 🔨	10-68 bF 10-22 pF	10 - 68 pF 10 - 22 pF					
Higher capacitance increases the stability of the oscil- lator but also increases the start-up time. These walkes are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components								

#### TABLE 9-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR

Mode	Freq	OSC1(C1)	OSC2(C2)	
LP	32 kHz	68 - 100 pF	68 - 100 pF	
	200 kHz	15 - 30 pF	15 - 30 pF	
хт	100 kHz	68 - 150 pF	150 - 300 pF	
	2 MHz	15 - 30 pF	15 - 30 pF	
	4 MHz	15 - 30 pF	15 - 30 pF	
HS	8 MHz	15-30 pF	<sup>V</sup> 15 - 30 pF	
	10 MHz	15-30 pF	15 - 30 pF	
	20 MHz 🔨	15-30 pF	15 - 30 pF	
Higher capacitance increases the stability of the oscillator but also increases the start-up time. These values are for design guidance only. Rs may be required in HS mode as well as XT mode to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.				

### 9.3 RESET

The PIC16C62X differentiates between various kinds of RESET:

- a) Power-on Reset (POR)
- b) MCLR Reset during normal operation
- c) MCLR Reset during SLEEP
- d) WDT Reset (normal operation)
- e) WDT wake-up (SLEEP)
- f) Brown-out Reset (BOR)

Some registers are not affected in any RESET condition Their status is unknown on POR and unchanged in any other RESET. Most other registers are reset to a "RESET state" on Power-on Reset,

MCLR Reset, WDT Reset and MCLR Reset during SLEEP. They are not affected by a WDT wake-up, since this is viewed as the resumption of normal operation. TO and PD bits are set or cleared differently in different RESET situations as indicated in Table 9-2. These bits are used in software to determine the nature of the RESET. See Table 9-5 for a full description of RESET states of all registers.

A simplified block diagram of the on-chip RESET circuit is shown in Figure 9-6.

The  $\overline{\text{MCLR}}$  Reset path has a noise filter to detect and ignore small pulses. See Table 12-5 for pulse width specification.





#### 9.4 Power-on Reset (POR), Power-up Timer (PWRT), Oscillator Start-up Timer (OST) and Brown-out Reset (BOR)

#### 9.4.1 POWER-ON RESET (POR)

The on-chip POR circuit holds the chip in RESET until VDD has reached a high enough level for proper operation. To take advantage of the POR, just tie the MCLR pin through a resistor to VDD. This will eliminate external RC components usually needed to create Power-on Reset. A maximum rise time for VDD is required. See Electrical Specifications for details.

The POR circuit does not produce an internal RESET when VDD declines.

When the device starts normal operation (exits the RESET condition), device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in RESET until the operating conditions are met.

For additional information, refer to Application Note AN607, "Power-up Trouble Shooting".

#### 9.4.2 POWER-UP TIMER (PWRT)

The Power-up Timer provides a fixed 72 ms (nominal) time-out on power-up only, from POR or Brown-out Reset. The Power-up Timer operates on an internal RC oscillator. The chip is kept in RESET as long as PWRT is active. The PWRT delay allows the VDD to rise to an acceptable level. A configuration bit, PWRTE can disable (if set) or enable (if cleared or programmed) the Power-up Timer. The Power-up Timer should always be enabled when Brown-out Reset is enabled.

The Power-up Time delay will vary from chip-to-chip and due to VDD, temperature and process variation. See DC parameters for details.

#### 9.4.3 OSCILLATOR START-UP TIMER (OST)

The Oscillator Start-Up Timer (OST) provides a 1024 oscillator cycle (from OSC1 input) delay after the PWRT delay is over. This ensures that the crystal oscillator or resonator has started and stabilized.

The OST time-out is invoked only for XT, LP and HS modes and only on Power-on Reset or wake-up from SLEEP.

#### 9.4.4 BROWN-OUT RESET (BOR)

The PIC16C62X members have on-chip Brown-out Reset circuitry. A configuration bit, BODEN, can disable (if clear/programmed) or enable (if set) the Brown-out Reset circuitry. If VDD falls below 4.0V refer to VBOR parameter D005 (VBOR) for greater than parameter (TBOR) in Table 12-5. The brown-out situation will RESET the chip. A RESET won't occur if VDD falls below 4.0V for less than parameter (TBOR).

On any RESET (Power-on, Brown-out, Watchdog, etc.) the chip will remain in RESET until VDD rises above BVDD. The Power-up Timer will now be invoked and will keep the chip in RESET an additional 72 ms.

If VDD drops below BVDD while the Power-up Timer is running, the chip will go back into a Brown-out Reset and the Power-up Timer will be re-initialized. Once VDD rises above BVDD, the Power-Up Timer will execute a 72 ms RESET. The Power-up Timer should always be enabled when Brown-out Reset is enabled. Figure 9-7 shows typical Brown-out situations.



#### FIGURE 9-7: BROWN-OUT SITUATIONS

#### 9.4.5 TIME-OUT SEQUENCE

On power-up the time-out sequence is as follows: First PWRT time-out is invoked after POR has expired. Then OST is activated. The total time-out will vary based on oscillator configuration and <u>PWRTE</u> bit status. For example, in RC mode with <u>PWRTE</u> bit erased (<u>PWRT</u> disabled), there will be no time-out at all. Figure 9-8, Figure 9-9 and Figure 9-10 depict time-out sequences.

Since the time-outs occur from the POR pulse, if  $\overline{\text{MCLR}}$  is kept low long enough, the time-outs will expire. Then bringing  $\overline{\text{MCLR}}$  high will begin execution immediately (see Figure 9-9). This is useful for testing purposes or to synchronize more than one PIC16C62X device operating in parallel.

Table 9-4 shows the RESET conditions for some special registers, while Table 9-5 shows the RESET conditions for all the registers.

#### 9.4.6 POWER CONTROL (PCON)/ STATUS REGISTER

The power control/STATUS register, PCON (address 8Eh), has two bits.

Bit0 is  $\overline{\text{BOR}}$  (Brown-out).  $\overline{\text{BOR}}$  is unknown on Poweron Reset. It must then be set by the user and checked on subsequent RESETS to see if  $\overline{\text{BOR}} = 0$ , indicating that a brown-out has occurred. The  $\overline{\text{BOR}}$  STATUS bit is a don't care and is not necessarily predictable if the brown-out circuit is disabled (by setting BODEN bit = 0 in the Configuration word).

Bit1 is POR (Power-on Reset). It is a '0' on Power-on Reset and unaffected otherwise. The user must write a '1' to this bit following a Power-on Reset. On a subsequent RESET, if POR is '0', it will indicate that a Power-on Reset must have occurred (VDD may have gone too low).

Oscillator Configuration	Powe	er-up	Brown-out Reset	Wake-up
	PWRTE = 0	PWRTE = 1	Brown-out Reset	from SLEEP
XT, HS, LP	72 ms + 1024 Tosc	1024 Tosc	72 ms + 1024 Tosc	1024 Tosc
RC	72 ms	_	72 ms	_

#### TABLE 9-1: TIME-OUT IN VARIOUS SITUATIONS

TABLE 9-2:	STATUS/PCON BITS AND THEIR SIGNIFICANCE

POR	BOR	то	PD	
0	Х	1	1	Power-on Reset
0	Х	0	Х	Illegal, TO is set on POR
0	Х	Х	0	Illegal, PD is set on POR
1	0	Х	Х	Brown-out Reset
1	1	0	u	WDT Reset
1	1	0	0	WDT Wake-up
1	1	u	u	MCLR Reset during normal operation
1	1	1	0	MCLR Reset during SLEEP

Legend: u = unchanged, x = unknown

#### TABLE 9-3: SUMMARY OF REGISTERS ASSOCIATED WITH BROWN-OUT

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR Reset	Value on all other RESETS <sup>(1)</sup>
83h	STATUS				TO	PD				0001 1xxx	000q quuu
8Eh	PCON							POR	BOR	0x	uq

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0', q = value depends on condition.

**Note 1:** Other (non Power-up) Resets include MCLR Reset, Brown-out Reset and Watchdog Timer Reset during normal operation.

# PIC16C62X

#### **FIGURE 9-11: EXTERNAL POWER-ON RESET CIRCUIT (FOR** SLOW VDD POWER-UP) Vdd Vdd D R R1 MCLR PIC16C62X С Note 1: External Power-on Reset circuit is required only if VDD power-up slope is too slow. The diode D helps discharge the capacitor quickly when VDD powers down. **2:** < 40 k $\Omega$ is recommended to make sure that voltage drop across R does not violate the device's electrical specification. **3:** R1 = $100\Omega$ to 1 k $\Omega$ will limit any current flowing into MCLR from external capacitor C in the event of MCLR/VPP pin

breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).

#### FIGURE 9-12: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 1



- Note 1: This circuit will activate RESET when VDD goes below (Vz + 0.7V) where Vz = Zener voltage.
  - **2:** Internal Brown-out Reset circuitry should be disabled when using this circuit.

#### FIGURE 9-13: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 2



**3:** Resistors should be adjusted for the characteristics of the transistor.

#### FIGURE 9-14: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 3



This brown-out protection circuit employs Microchip Technology's MCP809 microcontroller supervisor. The MCP8XX and MCP1XX families of supervisors provide push-pull and open collector outputs with both high and low active RESET pins. There are 7 different trip point selections to accommodate 5V and 3V systems.

TABLE 10-2:	PIC16C62X INSTRUCTION SET
-------------	---------------------------

Mnemonic,		Description	Cycles		14-Bit Opcode		Status	Notes	
Operands				MSb			LSb	Affected	
BYTE-ORIE	NTED I	FILE REGISTER OPERATIONS							
ADDWF	f, d	Add W and f	1	00	0111	dfff	ffff	C,DC,Z	1,2
ANDWF	f, d	AND W with f	1	00	0101	dfff	ffff	Z	1,2
CLRF	f	Clear f	1	00	0001	lfff	ffff	Z	2
CLRW	-	Clear W	1	00	0001	0000	0011	Z	
COMF	f, d	Complement f	1	00	1001	dfff	ffff	Z	1,2
DECF	f, d	Decrement f	1	00	0011	dfff	ffff	Z	1,2
DECFSZ	f, d	Decrement f, Skip if 0	1(2)	00	1011	dfff	ffff		1,2,3
INCF	f, d	Increment f	1	00	1010	dfff	ffff	Z	1,2
INCFSZ	f, d	Increment f, Skip if 0	1(2)	00	1111	dfff	ffff		1,2,3
IORWF	f, d	Inclusive OR W with f	1	00	0100	dfff	ffff	Z	1,2
MOVF	f, d	Move f	1	00	1000	dfff	ffff	Z	1,2
MOVWF	f	Move W to f	1	00	0000	lfff	ffff		
NOP	-	No Operation	1	00	0000	0xx0	0000		
RLF	f, d	Rotate Left f through Carry	1	00	1101	dfff	ffff	С	1,2
RRF	f, d	Rotate Right f through Carry	1	00	1100	dfff	ffff	С	1,2
SUBWF	f, d	Subtract W from f	1	00	0010	dfff	ffff	C,DC,Z	1,2
SWAPF	f, d	Swap nibbles in f	1	00	1110	dfff	ffff		1,2
XORWF	f, d	Exclusive OR W with f	1	00	0110	dfff	ffff	Z	1,2
BIT-ORIENT	ED FIL	E REGISTER OPERATIONS							
BCF	f, b	Bit Clear f	1	01	00bb	bfff	ffff		1,2
BSF	f, b	Bit Set f	1	01	01bb	bfff	ffff		1,2
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	01	10bb	bfff	ffff		3
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	01	11bb	bfff	ffff		3
LITERAL A	ND COI	NTROL OPERATIONS	-					-	
ADDLW	k	Add literal and W	1	11	111x	kkkk	kkkk	C,DC,Z	
ANDLW	k	AND literal with W	1	11	1001	kkkk	kkkk	Z	
CALL	k	Call subroutine	2	10	0kkk	kkkk	kkkk		
CLRWDT	-	Clear Watchdog Timer	1	00	0000	0110	0100	TO,PD	
GOTO	k	Go to address	2	10	1kkk	kkkk	kkkk		
IORLW	k	Inclusive OR literal with W	1	11	1000	kkkk	kkkk	Z	
MOVLW	k	Move literal to W	1	11	00xx	kkkk	kkkk		
RETFIE	-	Return from interrupt	2	00	0000	0000	1001		
RETLW	k	Return with literal in W	2	11	01xx	kkkk	kkkk		
RETURN	-	Return from Subroutine	2	00	0000	0000	1000		
SLEEP	-	Go into Standby mode	1	00	0000	0110	0011	TO,PD	
SUBLW	k	Subtract W from literal	1	11	110x	kkkk	kkkk	C,DC,Z	
XORLW	k	Exclusive OR literal with W	1	11	1010	kkkk	kkkk	Z	

**Note 1:** When an I/O register is modified as a function of itself (e.g., MOVF PORTB, 1), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

**2:** If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 Module.

**3:** If Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

# **10.1** Instruction Descriptions

ADDLW	Add Literal and W
Syntax:	[ <i>label</i> ] ADDLW k
Operands:	$0 \leq k \leq 255$
Operation:	$(W) + k \to (W)$
Status Affected:	C, DC, Z
Encoding:	11 111x kkkk kkkk
Description:	added to the eight bit literal 'k' and the result is placed in the W register.
Cycles:	1
Example	ADDLW 0x15
	Before Instruction W = 0x10 After Instruction W = 0x25

ANDLW	AND Literal with W
Syntax:	[ <i>label</i> ] ANDLW k
Operands:	$0 \le k \le 255$
Operation:	(W) .AND. (k) $\rightarrow$ (W)
Status Affected:	Z
Encoding:	11 1001 kkkk kkkk
Description:	The contents of W register are AND'ed with the eight bit literal 'k'. The result is placed in the W register.
Words:	1
Cycles:	1
Example	ANDLW 0x5F
	Before Instruction W = 0xA3 After Instruction W = 0x03
ANDWF	AND W with f

Add W and f
[ <i>label</i> ] ADDWF f,d
$\begin{array}{l} 0 \leq f \leq 127 \\ d  \in  [0,1] \end{array}$
(W) + (f) $\rightarrow$ (dest)
C, DC, Z
00 0111 dfff ffff
Add the contents of the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.
1
1
ADDWF FSR, <b>O</b>
Before Instruction W = 0x17 FSR = 0xC2 After Instruction W = 0xD9 FSR = 0xC2

ANDWF	AND W with f
Syntax:	[ <i>label</i> ] ANDWF f,d
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d  \in  [0,1] \end{array}$
Operation:	(W) .AND. (f) $\rightarrow$ (dest)
Status Affected:	Z
Encoding:	00 0101 dfff ffff
Description:	AND the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.
Words:	1
Cycles:	1
Example	ANDWF FSR, 1
	Before Instruction W = 0x17 FSR = 0xC2 After Instruction W = 0x17 FSR = 0x02

# PIC16C62X

CLRW	Clear W	COMF	Complement f
Syntax:	[label] CLRW	Syntax:	[ <i>label</i> ] COMF f,d
Operands:	None	Operands:	$0 \leq f \leq 127$
Operation:	$00h \rightarrow (W)$		d ∈ [0,1]
	$1 \rightarrow Z$	Operation:	$(f) \rightarrow (dest)$
Status Affected:	Z	Status Affected:	Z
Encoding:	00 0001 0000 0011	Encoding:	00 1001 dfff ffff
Description:	W register is cleared. Zero bit (Z) is set.	Description:	The contents of register 'f' are complemented. If 'd' is 0, the
Words:	1		result is stored in W. If 'd' is 1, the
Cycles:	1	Words:	1
Example	CLRW	Cycles:	1
	Before Instruction	Evernle	COME DECI 0
	W = 0x5A	Example	COMF REGI,0
	W = 0x00		REG1 = $0x13$
	Z = 1		After Instruction
			$\begin{array}{rcl} REG1 &= & 0x13 \\ W &= & 0xEC \end{array}$
CLRWDT	Clear Watchdog Timer		
Svntax:	[label] CLRWDT	DEAE	
<b>,</b>		DECF	Decrement f
Operands:	None	DECF Syntax:	Decrement f
Operands: Operation:	None $00h \rightarrow WDT$	DECF Syntax: Operands:	<b>Decrement f</b> [ <i>label</i> ] DECF f,d 0 < f < 127
Operands: Operation:	None $00h \rightarrow WDT$ $0 \rightarrow WDT$ prescaler, $1 \rightarrow TO$	Syntax: Operands:	Decrement f[ label ] DECF f,d $0 \le f \le 127$ $d \in [0,1]$
Operands: Operation:	None $00h \rightarrow WDT$ $0 \rightarrow WDT$ prescaler, $1 \rightarrow \overline{TO}$ $1 \rightarrow PD$	Syntax: Operands: Operation:	Decrement f [ <i>label</i> ] DECF f,d $0 \le f \le 127$ $d \in [0,1]$ (f) - 1 $\rightarrow$ (dest)
Operands: Operation: Status Affected:	None $00h \rightarrow WDT$ $0 \rightarrow WDT \text{ prescaler,}$ $1 \rightarrow \overline{TO}$ $1 \rightarrow PD$ $\overline{TO}, PD$	DECF Syntax: Operands: Operation: Status Affected:	Decrement f [ <i>label</i> ] DECF f,d $0 \le f \le 127$ $d \in [0,1]$ (f) - 1 $\rightarrow$ (dest) Z
Operands: Operation: Status Affected: Encoding:	None $00h \rightarrow WDT$ $0 \rightarrow WDT \text{ prescaler,}$ $1 \rightarrow \overline{TO}$ $1 \rightarrow PD$ $\overline{TO, PD}$ $00  0000  0110  0100$	DECF Syntax: Operands: Operation: Status Affected: Encoding:	Decrement f $[ label ]$ DECF f,d $0 \le f \le 127$ $d \in [0,1]$ $(f) - 1 \rightarrow (dest)$ Z $00$ $0011$ dfff
Operands: Operation: Status Affected: Encoding: Description:	None $00h \rightarrow WDT$ $0 \rightarrow WDT \text{ prescaler,}$ $1 \rightarrow \overline{TO}$ $1 \rightarrow PD$ $\overline{TO, PD}$ $00  0000  0110  0100$ CLRWDT instruction resets the	DECF Syntax: Operands: Operation: Status Affected: Encoding: Description:	Decrement f $[label]$ DECF f,d $0 \le f \le 127$ $d \in [0,1]$ (f) - 1 $\rightarrow$ (dest)Z000011dfffDecrement register 'f'. If 'd' is 0,
Operands: Operation: Status Affected: Encoding: Description:	None $00h \rightarrow WDT$ $0 \rightarrow WDT$ prescaler, $1 \rightarrow \overline{TO}$ $1 \rightarrow PD$ $\overline{TO}, \overline{PD}$ 00  0000  0110  0100 CLRWDT instruction resets the Watchdog Timer. It also resets the	DECF Syntax: Operands: Operation: Status Affected: Encoding: Description:	Decrement f[ /abe/ ] DECF f,d $0 \le f \le 127$ $d \in [0,1]$ (f) - 1 $\rightarrow$ (dest)Z000011dffffffDecrement register 'f'. If 'd' is 0,the result is stored in the W
Operands: Operation: Status Affected: Encoding: Description:	None $00h \rightarrow WDT$ $0 \rightarrow WDT$ prescaler, $1 \rightarrow \overline{TO}$ $1 \rightarrow PD$ $\overline{TO}, PD$ O CLRWDT instruction resets the Watchdog Timer. It also resets the prescaler of the WDT. STATUS http://open.com/	DECF Syntax: Operands: Operation: Status Affected: Encoding: Description:	Decrement f $[label]$ DECF f,d $0 \le f \le 127$ $d \in [0,1]$ $(f) - 1 \rightarrow (dest)$ Z $00$ 0011dffffffDecrement register 'f'. If 'd' is 0,the result is stored in the Wregister. If 'd' is 1, the result isctored back in register 'f'
Operands: Operation: Status Affected: Encoding: Description:	None $00h \rightarrow WDT$ $0 \rightarrow WDT prescaler,$ $1 \rightarrow TO$ $1 \rightarrow PD$ TO, PD 00  0000  0110  0100 CLRWDT instruction resets the Watchdog Timer. It also resets the pres <u>cal</u> er of the WDT. STATUS bits TO and PD are set.	DECF Syntax: Operands: Operation: Status Affected: Encoding: Description:	Decrement f[ label ] DECF f,d $0 \le f \le 127$ $d \in [0,1]$ (f) - 1 $\rightarrow$ (dest)Z000011dffffffDecrement register 'f'. If 'd' is 0,the result is stored in the Wregister. If 'd' is 1, the result isstored back in register 'f'.1
Operands: Operation: Status Affected: Encoding: Description: Words:	None $00h \rightarrow WDT$ $0 \rightarrow WDT$ prescaler, $1 \rightarrow \overline{TO}$ $1 \rightarrow PD$ $\overline{TO}, \overline{PD}$ OO 0000 0110 0100 CLRWDT instruction resets the Watchdog Timer. It also resets the prescaler of the WDT. STATUS bits TO and PD are set. 1	DECF Syntax: Operands: Operation: Status Affected: Encoding: Description: Words:	Decrement f $[ label ]$ DECF f,d $0 \le f \le 127$ $d \in [0,1]$ $(f) - 1 \rightarrow (dest)$ Z $00$ $0011$ dfffffffDecrement register 'f'. If 'd' is 0,the result is stored in the Wregister. If 'd' is 1, the result isstored back in register 'f'.1
Operands: Operation: Status Affected: Encoding: Description: Words: Cycles:	None $\begin{array}{l} 00h \rightarrow WDT \\ 0 \rightarrow WDT \text{ prescaler,} \\ 1 \rightarrow \overline{TO} \\ 1 \rightarrow PD \\ \hline \overline{TO}, \overline{PD} \\ \hline \hline 00 & 0000 & 0110 & 0100 \\ \hline \end{array}$ CLRWDT instruction resets the Watchdog Timer. It also resets the prescaler of the WDT. STATUS bits TO and PD are set. 1 1	DECF Syntax: Operands: Operation: Status Affected: Encoding: Description: Words: Cycles:	Decrement f $[label]$ DECF f,d $0 \le f \le 127$ $d \in [0,1]$ $(f) - 1 \rightarrow (dest)$ Z $00$ $0011$ dffffffDecrement register 'f'. If 'd' is 0,the result is stored in the Wregister. If 'd' is 1, the result isstored back in register 'f'.111
Operands: Operation: Status Affected: Encoding: Description: Words: Cycles: Example	None $00h \rightarrow WDT$ $0 \rightarrow WDT prescaler,$ $1 \rightarrow TO$ $1 \rightarrow PD$ TO, PD 00  0000  0110  0100 CLRWDT instruction resets the Watchdog Timer. It also resets the pres <u>caler of the</u> WDT. STATUS bits TO and PD are set. 1 1 CLRWDT Defense landmention	DECF Syntax: Operands: Operation: Status Affected: Encoding: Description: Words: Cycles: Example	Decrement f $[ label ]$ DECF f,d $0 \le f \le 127$ $d \in [0,1]$ $(f) - 1 \rightarrow (dest)$ Z000011dfffffffDecrement register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.11DECFCNT, 1Decrement register
Operands: Operation: Status Affected: Encoding: Description: Words: Cycles: Example	None $00h \rightarrow WDT$ $0 \rightarrow WDT$ prescaler, $1 \rightarrow TO$ $1 \rightarrow PD$ TO, PD 00  0000  0110  0100 CLRWDT instruction resets the Watchdog Timer. It also resets the prescaler of the WDT. STATUS bits TO and PD are set. 1 1 CLRWDT Before Instruction WDT counter = 2	DECF Syntax: Operands: Operation: Status Affected: Encoding: Description: Words: Cycles: Example	Decrement f [ <i>label</i> ] DECF f,d $0 \le f \le 127$ $d \in [0,1]$ (f) - 1 → (dest) Z 00 0011 dfff fff Decrement register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'. 1 1 DECF CNT, 1 Before Instruction CNT = 0x01
Operands: Operation: Status Affected: Encoding: Description: Words: Cycles: Example	None $\begin{array}{l} 00h \rightarrow WDT \\ 0 \rightarrow WDT \ prescaler, \\ 1 \rightarrow \overline{TO} \\ 1 \rightarrow PD \\ \hline TO, PD \\ \hline 00 & 0000 & 0110 & 0100 \\ \hline \end{array}$ CLRWDT instruction resets the Watchdog Timer. It also resets the Watchdog Timer. It also resets the prescaler of the WDT. STATUS bits TO and PD are set. 1 1 CLRWDT Before Instruction WDT counter = ? After Instruction	DECF Syntax: Operands: Operation: Status Affected: Encoding: Description: Words: Cycles: Example	Decrement f[ label ] DECF f,d $0 \le f \le 127$ $d \in [0,1]$ (f) - 1 $\rightarrow$ (dest)Z $00$ $0011$ dffffffDecrement register 'f'. If 'd' is 0,the result is stored in the Wregister. If 'd' is 1, the result isstored back in register 'f'.11DECFCNT, 1Before InstructionCNT $Z$ $=$ $0$
Operands: Operation: Status Affected: Encoding: Description: Words: Cycles: Example	None $00h \rightarrow WDT$ $0 \rightarrow WDT prescaler,$ $1 \rightarrow TO$ $1 \rightarrow PD$ TO, PD 00  0000  0110  0100 CLRWDT instruction resets the Watchdog Timer. It also resets the prescaler of the WDT. STATUS bits TO and PD are set. 1 1 CLRWDT Before Instruction WDT counter = ? After Instruction WDT counter = 0x00 WDT counter = 0x00	DECF Syntax: Operands: Operation: Status Affected: Encoding: Description: Words: Cycles: Example	Decrement f         [/abel]       DECF f,d $0 \le f \le 127$ $d \in [0,1]$ $(f) - 1 \rightarrow (dest)$ Z $00$ $0011$ dfff         fff       Decrement register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.         1       DECF       CNT, 1         Before Instruction       CNT       = 0x01         Z       = 0       After Instruction
Operands: Operation: Status Affected: Encoding: Description: Words: Cycles: Example	None $\begin{array}{c} 00h \rightarrow WDT \\ 0 \rightarrow WDT \ prescaler, \\ 1 \rightarrow TO \\ 1 \rightarrow PD \\ \hline TO, PD \\ \hline 00 & 0000 & 0110 & 0100 \\ \hline \end{array}$ CLRWDT instruction resets the Watchdog Timer. It also resets the Watchdog Timer. It also resets the prescaler of the WDT. STATUS bits TO and PD are set. 1 1 CLRWDT Before Instruction WDT counter = ? After Instruction WDT counter = 0 TO = 1	DECF Syntax: Operands: Operation: Status Affected: Encoding: Description: Words: Cycles: Example	Decrement f $[label]$ DECF f,d $0 \le f \le 127$ $d \in [0,1]$ $(f) - 1 \rightarrow (dest)$ Z $00$ $0011$ dfffffDecrement register 'f'. If 'd' is 0,the result is stored in the Wregister. If 'd' is 1, the result isstored back in register 'f'.11DECFCNTCNT $Z$ $=$ 0After InstructionCNTCNT $Z$ $=$ 0After InstructionCNT $CNT$ $=$ $0x00$ $Z$ $=$ $1$

SWAPF	Swap Nibbles in f					
Syntax:	[label]	SWAPF	f,d			
Operands:	$0 \le f \le 127$ $d \in [0,1]$					
Operation:	(f<3:0>) → (dest<7:4>), (f<7:4>) → (dest<3:0>)					
Status Affected:	None					
Encoding:	00	1110	dfff	Ē	ffff	
Description:	register 'f' are exchanged. If 'd' is 0, the result is placed in W register. If 'd' is 1, the result is placed in register 'f'.					
Words:	1					
Cycles:	1					
Example	SWAPF	REG,	0			
	Before Instruction					
		REG1	=	0xA5		
	After Instruction					
		REG1 W	= =	0xA5 0x5A		

TRIS	Load TRIS Register					
Syntax:	[ <i>label</i> ] TRIS f					
Operands:	$5 \leq f \leq 7$					
Operation:	$(W) \rightarrow TRIS$ register f;					
Status Affected:	None					
Encoding:	00 0000 0110 Offf					
Description.	code compatibility with the PIC16C5X products. Since TRIS registers are readable and writable, the user can directly address them.					
Words:	1					
Cycles:	1					
Example						
	To maintain upward compatibil- ity with future PICmicro <sup>®</sup> prod- ucts, do not use this instruction.					

XORLW	Exclusiv	Exclusive OR Literal with W					
Syntax:	[ label ]	XORL	Wk				
Operands:	$0 \le k \le 2$	$0 \le k \le 255$					
Operation:	(W) .XOR. $k \rightarrow (W)$						
Status Affected:	Z						
Encoding:	11	1010	kkkk	: kkkk			
Description:	The contents of the W register are XOR'ed with the eight bit literal 'k'. The result is placed in the W register.						
Words:	1						
Cycles:	1						
Example:	XORLW	0xAF					
	Before Instruction						
		W =	0xB8	5			
	After Ins	After Instruction					
		W =	0x1A	4			
YOBWE	Exclusiv		with f				
Suntax:			fd				
Operands:	0 ≤ f ≤ 12 d ∈ [0,1]	7	ı,u				
Operation:	(W) .XOR. (f) $\rightarrow$ (dest)						
Status Affected:	Z						
Encoding:	00	0110	dfff	ffff			
Description:	Exclusive OR the contents of the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.						
Words:	1						
Cycles:	1						
Example	XORWF	REG	1				
	Before Instruction						
		REG W	= ( = (	)xAF )xB5			
	After Instruction						
		REG W	= ( = (	)x1A )xB5			

# PIC16C62X









## 13.0 DEVICE CHARACTERIZATION INFORMATION

The graphs and tables provided in this section are for design guidance and are not tested. In some graphs or tables, the data presented is outside specified operating range (e.g., outside specified VDD range). This is for information only and devices will operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. "Typical" represents the mean of the distribution, while "max" or "min" represents (mean +  $3\sigma$ ) and (mean -  $3\sigma$ ) respectively, where  $\sigma$  is standard deviation.



FIGURE 13-1: IDD VS. FREQUENCY (XT MODE, VDD = 5.5V)

FIGURE 13-2: PIC16C622A IPD VS. VDD (WDT DISABLE)



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