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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	13
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	18-DIP (0.300", 7.62mm)
Supplier Device Package	18-PDIP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic16c622a-20-p">https://www.e-xfl.com/product-detail/microchip-technology/pic16c622a-20-p</a>

# PIC16C62X

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NOTES:

# PIC16C62X

**FIGURE 4-6: DATA MEMORY MAP FOR THE PIC16C620A/CR620A/621A**

File Address			File Address
00h	INDF <sup>(1)</sup>	INDF <sup>(1)</sup>	80h
01h	TMR0	OPTION	81h
02h	PCL	PCL	82h
03h	STATUS	STATUS	83h
04h	FSR	FSR	84h
05h	PORTA	TRISA	85h
06h	PORTB	TRISB	86h
07h			87h
08h			88h
09h			89h
0Ah	PCLATH	PCLATH	8Ah
0Bh	INTCON	INTCON	8Bh
0Ch	PIR1	PIE1	8Ch
0Dh			8Dh
0Eh		PCON	8Eh
0Fh			8Fh
10h			90h
11h			91h
12h			92h
13h			93h
14h			94h
15h			95h
16h			96h
17h			97h
18h			98h
19h			99h
1Ah			9Ah
1Bh			9Bh
1Ch			9Ch
1Dh			9Dh
1Eh			9Eh
1Fh	CMCON	VRCON	9Fh
20h	General Purpose Register		A0h
6Fh			F0h
70h	General Purpose Register	Accesses 70h-7Fh	F0h
7Fh			FFh
Bank 0		Bank 1	

☐ Unimplemented data memory locations, read as '0'.

**Note 1:** Not a physical register.

**FIGURE 4-7: DATA MEMORY MAP FOR THE PIC16C622A**

File Address			File Address
00h	INDF <sup>(1)</sup>	INDF <sup>(1)</sup>	80h
01h	TMR0	OPTION	81h
02h	PCL	PCL	82h
03h	STATUS	STATUS	83h
04h	FSR	FSR	84h
05h	PORTA	TRISA	85h
06h	PORTB	TRISB	86h
07h			87h
08h			88h
09h			89h
0Ah	PCLATH	PCLATH	8Ah
0Bh	INTCON	INTCON	8Bh
0Ch	PIR1	PIE1	8Ch
0Dh			8Dh
0Eh		PCON	8Eh
0Fh			8Fh
10h			90h
11h			91h
12h			92h
13h			93h
14h			94h
15h			95h
16h			96h
17h			97h
18h			98h
19h			99h
1Ah			9Ah
1Bh			9Bh
1Ch			9Ch
1Dh			9Dh
1Eh			9Eh
1Fh	CMCON	VRCON	9Fh
20h	General Purpose Register	General Purpose Register	A0h
			BFh
			C0h
6Fh	General Purpose Register		F0h
70h			F0h
7Fh	General Purpose Register	Accesses 70h-7Fh	FFh
Bank 0		Bank 1	

☐ Unimplemented data memory locations, read as '0'.

**Note 1:** Not a physical register.

# PIC16C62X

## 4.2.2.1 STATUS Register

The STATUS register, shown in Register 4-1, contains the arithmetic status of the ALU, the RESET status and the bank select bits for data memory.

The STATUS register can be the destination for any instruction, like any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the  $\overline{\text{TO}}$  and  $\overline{\text{PD}}$  bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper-three bits and set the Z bit. This leaves the STATUS register as 000uu1uu (where u = unchanged).

It is recommended, therefore, that only `BCF`, `BSF`, `SWAPF` and `MOVWF` instructions are used to alter the STATUS register, because these instructions do not affect any STATUS bit. For other instructions not affecting any STATUS bits, see the "Instruction Set Summary".

**Note 1:** The IRP and RP1 bits (STATUS<7:6>) are not used by the PIC16C62X and should be programmed as '0'. Use of these bits as general purpose R/W bits is NOT recommended, since this may affect upward compatibility with future products.

**2:** The C and DC bits operate as a Borrow and Digit Borrow out bit, respectively, in subtraction. See the `SUBLW` and `SUBWF` instructions for examples.

## REGISTER 4-1: STATUS REGISTER (ADDRESS 03H OR 83H)

Reserved	Reserved	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
IRP	RP1	RP0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C
bit 7							bit 0

- bit 7 **IRP:** Register Bank Select bit (used for indirect addressing)  
 1 = Bank 2, 3 (100h - 1FFh)  
 0 = Bank 0, 1 (00h - FFh)  
 The IRP bit is reserved on the PIC16C62X; always maintain this bit clear.
- bit 6-5 **RP<1:0>:** Register Bank Select bits (used for direct addressing)  
 01 = Bank 1 (80h - FFh)  
 00 = Bank 0 (00h - 7Fh)  
 Each bank is 128 bytes. The RP1 bit is reserved on the PIC16C62X; always maintain this bit clear.
- bit 4  **$\overline{\text{TO}}$ :** Time-out bit  
 1 = After power-up, `CLRWDT` instruction, or `SLEEP` instruction  
 0 = A WDT time-out occurred
- bit 3  **$\overline{\text{PD}}$ :** Power-down bit  
 1 = After power-up or by the `CLRWDT` instruction  
 0 = By execution of the `SLEEP` instruction
- bit 2 **Z:** Zero bit  
 1 = The result of an arithmetic or logic operation is zero  
 0 = The result of an arithmetic or logic operation is not zero
- bit 1 **DC:** Digit carry/borrow bit (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions)(for borrow the polarity is reversed)  
 1 = A carry-out from the 4th low order bit of the result occurred  
 0 = No carry-out from the 4th low order bit of the result
- bit 0 **C:** Carry/borrow bit (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions)  
 1 = A carry-out from the Most Significant bit of the result occurred  
 0 = No carry-out from the Most Significant bit of the result occurred
- Note:** For borrow the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (`RRF`, `RLF`) instructions, this bit is loaded with either the high or low order bit of the source register.

### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared    x = Bit is unknown

# PIC16C62X

## 4.2.2.3 INTCON Register

The INTCON register is a readable and writable register, which contains the various enable and flag bits for all interrupt sources except the comparator module. See Section 4.2.2.4 and Section 4.2.2.5 for a description of the comparator enable and flag bits.

**Note:** Interrupt flag bits get set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>).

### REGISTER 4-3: INTCON REGISTER (ADDRESS 0BH OR 8BH)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF
bit 7							bit 0

- bit 7 **GIE:** Global Interrupt Enable bit  
1 = Enables all un-masked interrupts  
0 = Disables all interrupts
- bit 6 **PEIE:** Peripheral Interrupt Enable bit  
1 = Enables all un-masked peripheral interrupts  
0 = Disables all peripheral interrupts
- bit 5 **TOIE:** TMR0 Overflow Interrupt Enable bit  
1 = Enables the TMR0 interrupt  
0 = Disables the TMR0 interrupt
- bit 4 **INTE:** RB0/INT External Interrupt Enable bit  
1 = Enables the RB0/INT external interrupt  
0 = Disables the RB0/INT external interrupt
- bit 3 **RBIE:** RB Port Change Interrupt Enable bit  
1 = Enables the RB port change interrupt  
0 = Disables the RB port change interrupt
- bit 2 **TOIF:** TMR0 Overflow Interrupt Flag bit  
1 = TMR0 register has overflowed (must be cleared in software)  
0 = TMR0 register did not overflow
- bit 1 **INTF:** RB0/INT External Interrupt Flag bit  
1 = The RB0/INT external interrupt occurred (must be cleared in software)  
0 = The RB0/INT external interrupt did not occur
- bit 0 **RBIF:** RB Port Change Interrupt Flag bit  
1 = When at least one of the RB<7:4> pins changed state (must be cleared in software)  
0 = None of the RB<7:4> pins have changed state

#### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared    x = Bit is unknown

## 4.2.2.4 PIE1 Register

This register contains the individual enable bit for the comparator interrupt.

### REGISTER 4-4: PIE1 REGISTER (ADDRESS 8CH)

U-0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0
—	CMIE	—	—	—	—	—	—
bit 7							bit 0

- bit 7 **Unimplemented:** Read as '0'
- bit 6 **CMIE:** Comparator Interrupt Enable bit  
1 = Enables the Comparator interrupt  
0 = Disables the Comparator interrupt
- bit 5-0 **Unimplemented:** Read as '0'

#### Legend:

R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '0'  
- n = Value at POR      '1' = Bit is set      '0' = Bit is cleared      x = Bit is unknown

## 4.2.2.5 PIR1 Register

This register contains the individual flag bit for the comparator interrupt.

**Note:** Interrupt flag bits get set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

### REGISTER 4-5: PIR1 REGISTER (ADDRESS 0CH)

U-0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0
—	CMIF	—	—	—	—	—	—
bit 7							bit 0

- bit 7 **Unimplemented:** Read as '0'
- bit 6 **CMIF:** Comparator Interrupt Flag bit  
1 = Comparator input has changed  
0 = Comparator input has not changed
- bit 5-0 **Unimplemented:** Read as '0'

#### Legend:

R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '0'  
- n = Value at POR      '1' = Bit is set      '0' = Bit is cleared      x = Bit is unknown

**TABLE 5-1: PORTA FUNCTIONS**

Name	Bit #	Buffer Type	Function
RA0/AN0	bit0	ST	Input/output or comparator input
RA1/AN1	bit1	ST	Input/output or comparator input
RA2/AN2/VREF	bit2	ST	Input/output or comparator input or VREF output
RA3/AN3	bit3	ST	Input/output or comparator input/output
RA4/T0CKI	bit4	ST	Input/output or external clock input for TMR0 or comparator output. Output is open drain type.

Legend: ST = Schmitt Trigger input

**TABLE 5-2: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Value on All Other RESETS
05h	PORTA	—	—	—	RA4	RA3	RA2	RA1	RA0	---x 0000	---u 0000
85h	TRISA	—	—	—	TRISA 4	TRISA 3	TRISA 2	TRISA 1	TRISA 0	---1 1111	---1 1111
1Fh	CMCON	C2OUT	C1OUT	—	—	CIS	CM2	CM1	CM0	00-- 0000	00-- 0000
9Fh	VRCON	VREN	VROE	VRR	—	VR3	VR2	VR1	VR0	000- 0000	000- 0000

Legend: — = Unimplemented locations, read as '0', u = unchanged, x = unknown

**Note:** Shaded bits are not used by PORTA.

## 6.0 TIMER0 MODULE

The Timer0 module timer/counter has the following features:

- 8-bit timer/counter
- Readable and writable
- 8-bit software programmable prescaler
- Internal or external clock select
- Interrupt on overflow from FFh to 00h
- Edge select for external clock

Figure 6-1 is a simplified block diagram of the Timer0 module.

Timer mode is selected by clearing the T0CS bit (OPTION<5>). In Timer mode, the TMR0 will increment every instruction cycle (without prescaler). If Timer0 is written, the increment is inhibited for the following two cycles (Figure 6-2 and Figure 6-3). The user can work around this by writing an adjusted value to TMR0.

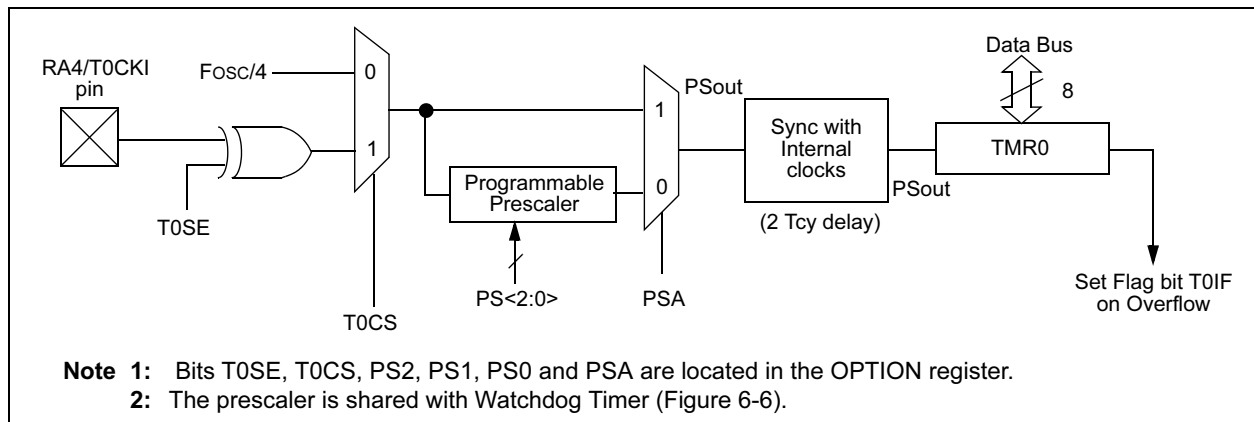
Counter mode is selected by setting the T0CS bit. In this mode, Timer0 will increment either on every rising or falling edge of pin RA4/T0CKI. The incrementing edge is determined by the source edge (T0SE) control bit (OPTION<4>). Clearing the T0SE bit selects the rising edge. Restrictions on the external clock input are discussed in detail in Section 6.2.

The prescaler is shared between the Timer0 module and the Watchdog Timer. The prescaler assignment is controlled in software by the control bit PSA (OPTION<3>). Clearing the PSA bit will assign the prescaler to Timer0. The prescaler is not readable or writable. When the prescaler is assigned to the Timer0 module, prescale value of 1:2, 1:4, ..., 1:256 are selectable. Section 6.3 details the operation of the prescaler.

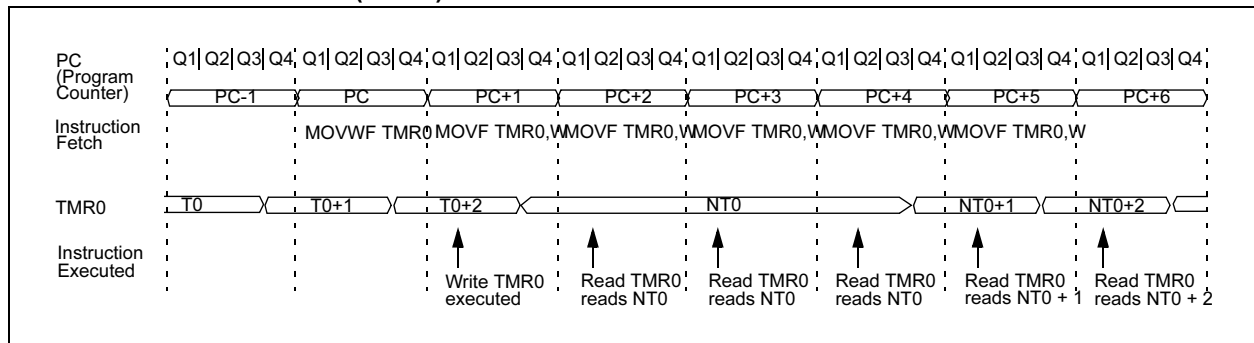
### 6.1 TIMER0 Interrupt

Timer0 interrupt is generated when the TMR0 register timer/counter overflows from FFh to 00h. This overflow sets the T0IF bit. The interrupt can be masked by clearing the T0IE bit (INTCON<5>). The T0IF bit (INTCON<2>) must be cleared in software by the Timer0 module interrupt service routine before re-enabling this interrupt. The Timer0 interrupt cannot wake the processor from SLEEP, since the timer is shut off during SLEEP. See Figure 6-4 for Timer0 interrupt timing.

**FIGURE 6-1: TIMER0 BLOCK DIAGRAM**



**FIGURE 6-2: TIMER0 (TMR0) TIMING: INTERNAL CLOCK/NO PRESCALER**





## 9.3 RESET

The PIC16C62X differentiates between various kinds of RESET:

- Power-on Reset (POR)
- $\overline{\text{MCLR}}$  Reset during normal operation
- $\overline{\text{MCLR}}$  Reset during SLEEP
- WDT Reset (normal operation)
- WDT wake-up (SLEEP)
- Brown-out Reset (BOR)

Some registers are not affected in any RESET condition. Their status is unknown on POR and unchanged in any other RESET. Most other registers are reset to a "RESET state" on Power-on Reset,

$\overline{\text{MCLR}}$  Reset, WDT Reset and  $\overline{\text{MCLR}}$  Reset during SLEEP. They are not affected by a WDT wake-up, since this is viewed as the resumption of normal operation.  $\overline{\text{TO}}$  and  $\overline{\text{PD}}$  bits are set or cleared differently in different RESET situations as indicated in Table 9-2. These bits are used in software to determine the nature of the RESET. See Table 9-5 for a full description of RESET states of all registers.

A simplified block diagram of the on-chip RESET circuit is shown in Figure 9-6.

The  $\overline{\text{MCLR}}$  Reset path has a noise filter to detect and ignore small pulses. See Table 12-5 for pulse width specification.

**FIGURE 9-6: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT**

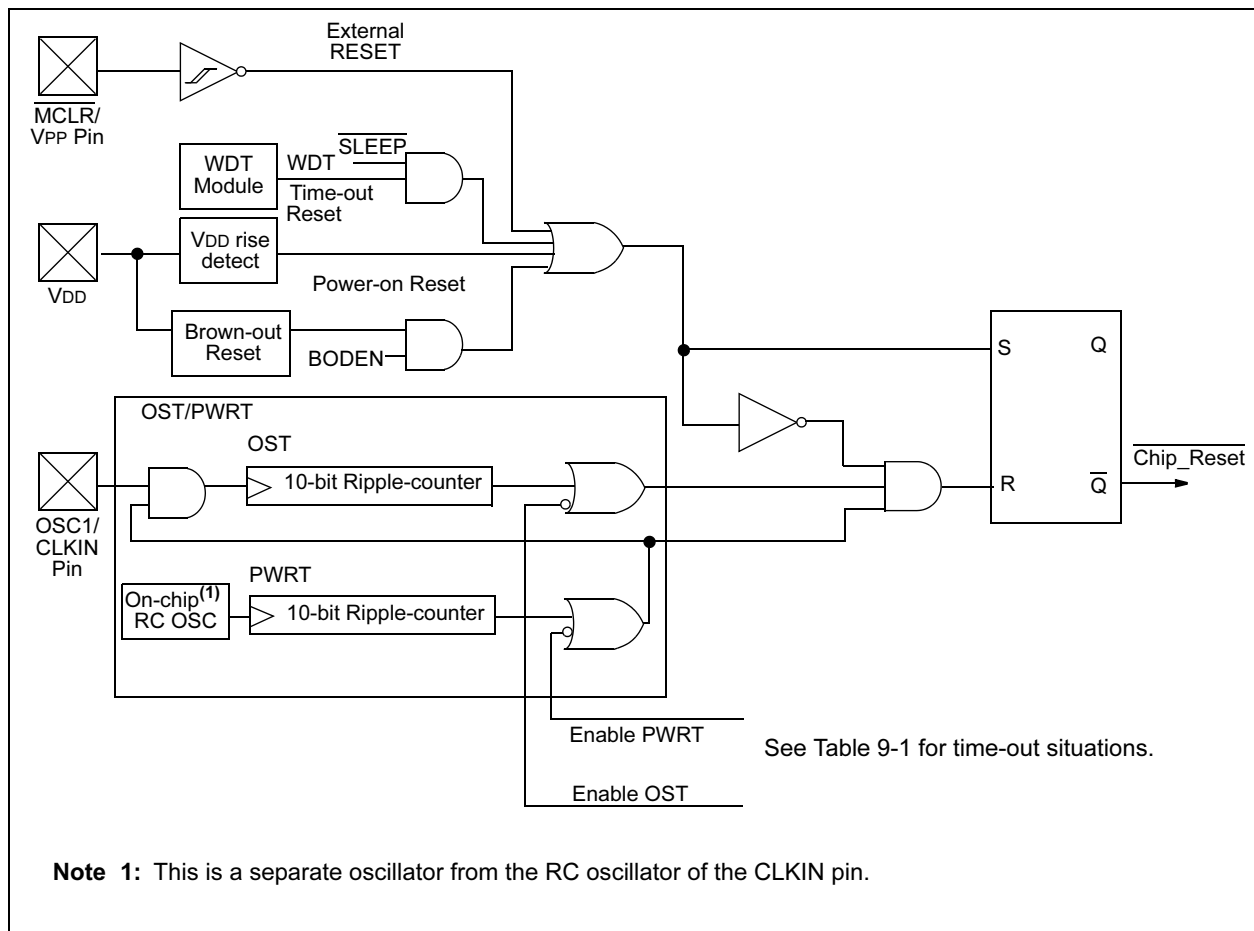


FIGURE 9-8: TIME-OUT SEQUENCE ON POWER-UP ( $\overline{\text{MCLR}}$  NOT TIED TO  $V_{\text{DD}}$ ): CASE 1

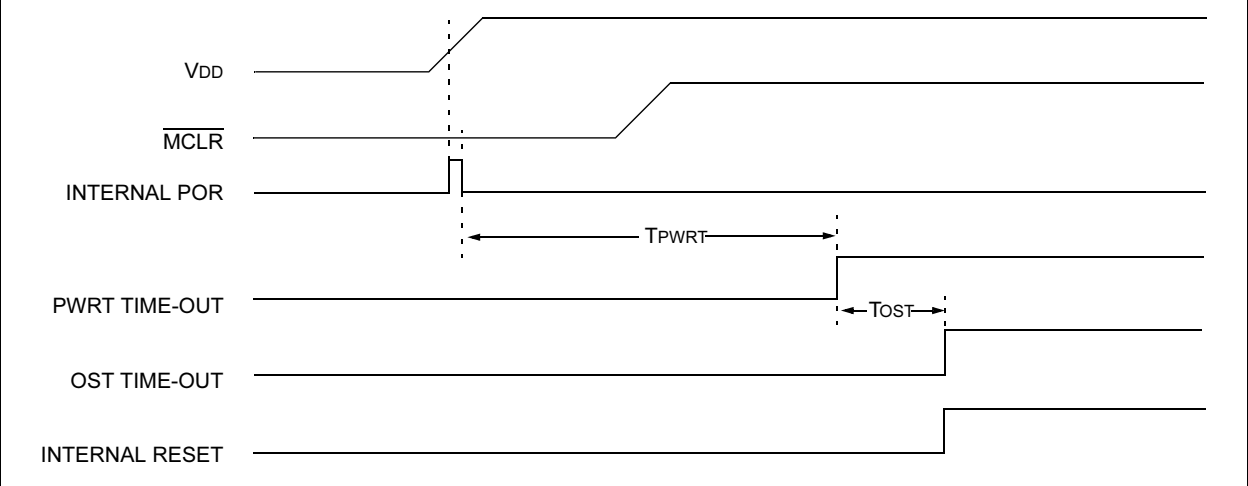


FIGURE 9-9: TIME-OUT SEQUENCE ON POWER-UP ( $\overline{\text{MCLR}}$  NOT TIED TO  $V_{\text{DD}}$ ): CASE 2

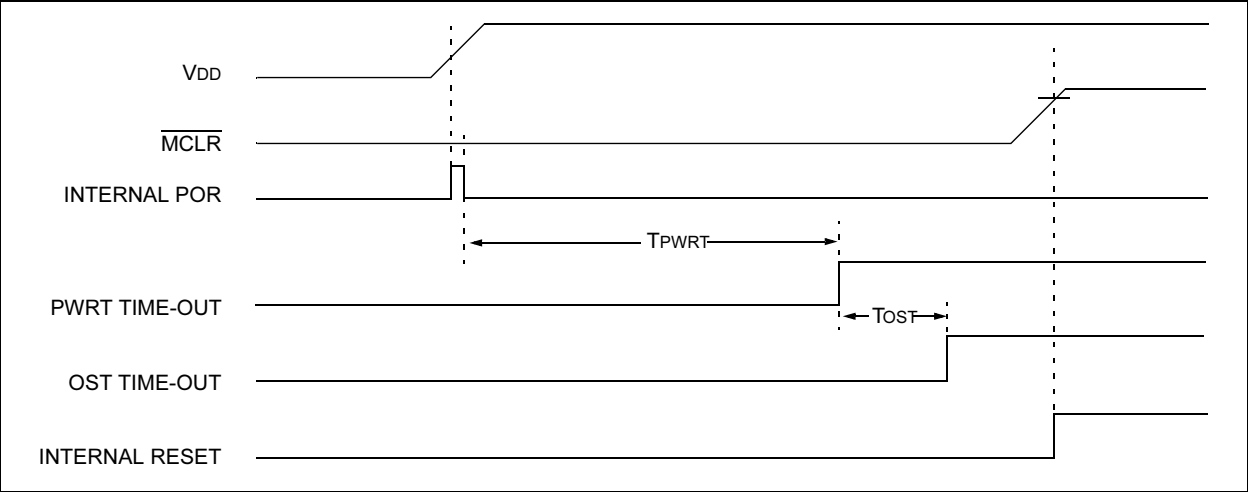
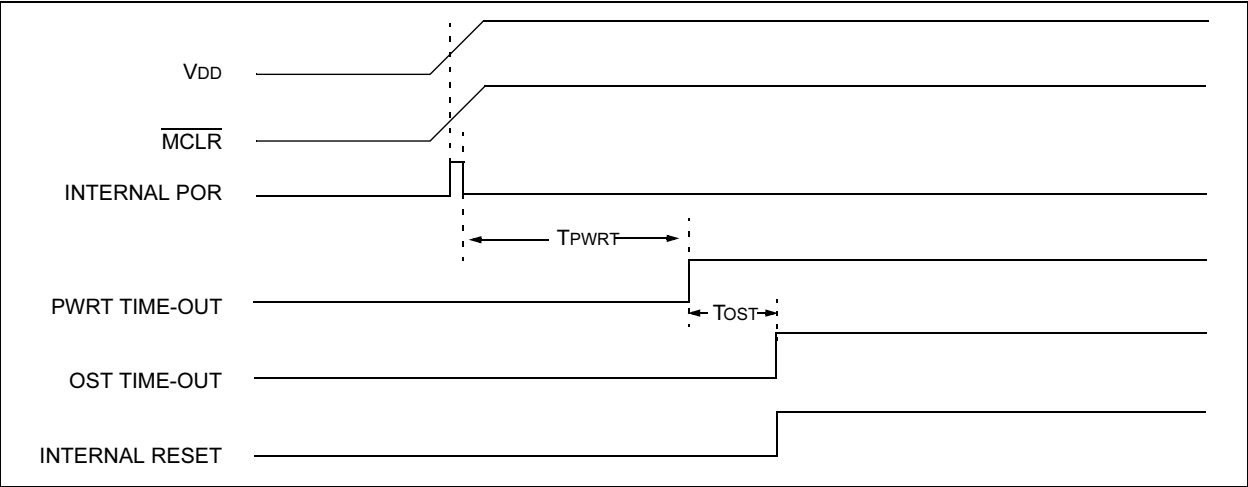


FIGURE 9-10: TIME-OUT SEQUENCE ON POWER-UP ( $\overline{\text{MCLR}}$  TIED TO  $V_{\text{DD}}$ )



## 9.8 Power-Down Mode (SLEEP)

The Power-down mode is entered by executing a SLEEP instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the PD bit in the STATUS register is cleared, the TO bit is set, and the oscillator driver is turned off. The I/O ports maintain the status they had, before SLEEP was executed (driving high, low, or hi-impedance).

For lowest current consumption in this mode, all I/O pins should be either at VDD or VSS with no external circuitry drawing current from the I/O pin and the comparators and VREF should be disabled. I/O pins that are hi-impedance inputs should be pulled high or low externally to avoid switching currents caused by floating inputs. The T0CKI input should also be at VDD or VSS for lowest current consumption. The contribution from on chip pull-ups on PORTB should be considered.

The MCLR pin must be at a logic high level (VIHMC).

**Note:** It should be noted that a RESET generated by a WDT time-out does not drive MCLR pin low.

The first event will cause a device RESET. The two latter events are considered a continuation of program execution. The  $\overline{TO}$  and  $\overline{PD}$  bits in the STATUS register can be used to determine the cause of device RESET. PD bit, which is set on power-up, is cleared when SLEEP is invoked.  $\overline{TO}$  bit is cleared if WDT wake-up occurred.

When the SLEEP instruction is being executed, the next instruction (PC + 1) is pre-fetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set (enabled). Wake-up is regardless of the state of the GIE bit. If the GIE bit is clear (disabled), the device continues execution at the instruction after the SLEEP instruction. If the GIE bit is set (enabled), the device executes the instruction after the SLEEP instruction and then branches to the interrupt address (0004h). In cases where the execution of the instruction following SLEEP is not desirable, the user should have an NOP after the SLEEP instruction.

**Note:** If the global interrupts are disabled (GIE is cleared), but any interrupt source has both its interrupt enable bit and the corresponding interrupt flag bits set, the device will immediately wake-up from SLEEP. The SLEEP instruction is completely executed.

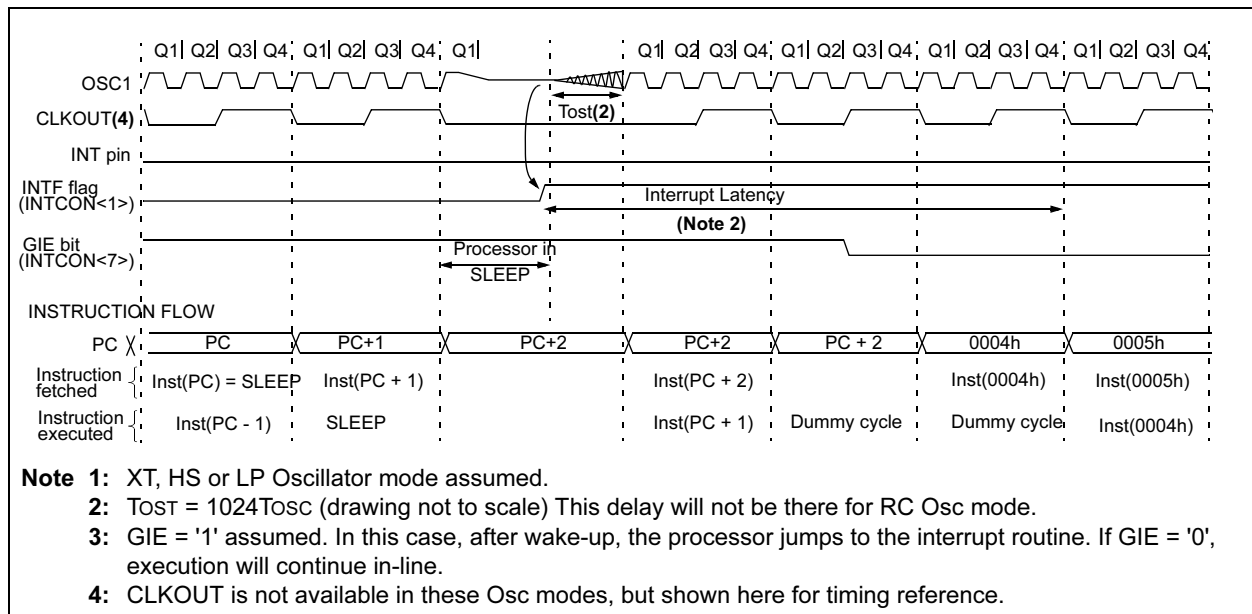
### 9.8.1 WAKE-UP FROM SLEEP

The device can wake-up from SLEEP through one of the following events:

1. External RESET input on MCLR pin
2. Watchdog Timer Wake-up (if WDT was enabled)
3. Interrupt from RB0/INT pin, RB Port change, or the Peripheral Interrupt (Comparator).

The WDT is cleared when the device wakes up from SLEEP, regardless of the source of wake-up.

**FIGURE 9-18: WAKE-UP FROM SLEEP THROUGH INTERRUPT**



## 10.1 Instruction Descriptions

ADDLW		Add Literal and W							
Syntax:	[ <i>label</i> ] ADDLW    k								
Operands:	$0 \leq k \leq 255$								
Operation:	$(W) + k \rightarrow (W)$								
Status Affected:	C, DC, Z								
Encoding:	<table border="1"><tr><td>11</td><td>111x</td><td>kkkk</td><td>kkkk</td></tr></table>					11	111x	kkkk	kkkk
11	111x	kkkk	kkkk						
Description:	The contents of the W register are added to the eight bit literal 'k' and the result is placed in the W register.								
Words:	1								
Cycles:	1								
Example	ADDLW    0x15								
	Before Instruction								
	W        =    0x10								
	After Instruction								
	W        =    0x25								

ADDWF		Add W and f							
Syntax:	[ <i>label</i> ] ADDWF    f,d								
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$								
Operation:	$(W) + (f) \rightarrow (\text{dest})$								
Status Affected:	C, DC, Z								
Encoding:	<table border="1"><tr><td>00</td><td>0111</td><td>dfff</td><td>ffff</td></tr></table>					00	0111	dfff	ffff
00	0111	dfff	ffff						
Description:	Add the contents of the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.								
Words:	1								
Cycles:	1								
Example	ADDWF    FSR,    0								
	Before Instruction								
	W    =    0x17								
	FSR =    0xC2								
	After Instruction								
	W    =    0xD9								
	FSR =    0xC2								

ANDLW		AND Literal with W							
Syntax:	[ <i>label</i> ] ANDLW    k								
Operands:	$0 \leq k \leq 255$								
Operation:	$(W) .\text{AND}. (k) \rightarrow (W)$								
Status Affected:	Z								
Encoding:	<table border="1"><tr><td>11</td><td>1001</td><td>kkkk</td><td>kkkk</td></tr></table>					11	1001	kkkk	kkkk
11	1001	kkkk	kkkk						
Description:	The contents of W register are AND'ed with the eight bit literal 'k'. The result is placed in the W register.								
Words:	1								
Cycles:	1								
Example	ANDLW    0x5F								
	Before Instruction								
	W        =    0xA3								
	After Instruction								
	W        =    0x03								

ANDWF		AND W with f						
Syntax:	[ <i>label</i> ] ANDWF    f,d							
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$							
Operation:	(W) .AND. (f) $\rightarrow$ (dest)							
Status Affected:	Z							
Encoding:	<table border="1"><tr><td>00</td><td>0101</td><td>dfff</td><td>ffff</td></tr></table>				00	0101	dfff	ffff
00	0101	dfff	ffff					
Description:	AND the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.							
Words:	1							
Cycles:	1							
Example	ANDWF    FSR,    1							
	Before Instruction							
	W    =    0x17							
	FSR =    0xC2							
	After Instruction							
	W    =    0x17							
	FSR =    0x02							

## RLF Rotate Left f through Carry

**Syntax:** [ *label* ] RLF f,d

**Operands:**  $0 \leq f \leq 127$   
 $d \in [0,1]$

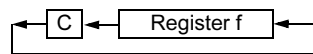
**Operation:** See description below

**Status Affected:** C

**Encoding:**

00	1101	dfff	ffff
----	------	------	------

**Description:** The contents of register 'f' are rotated one bit to the left through the Carry Flag. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is stored back in register 'f'.



**Words:** 1

**Cycles:** 1

**Example** RLF REG1,0

**Before Instruction**

REG1 = 1110 0110  
 C = 0

**After Instruction**

REG1 = 1110 0110  
 W = 1100 1100  
 C = 1

## RRF Rotate Right f through Carry

**Syntax:** [ *label* ] RRF f,d

**Operands:**  $0 \leq f \leq 127$   
 $d \in [0,1]$

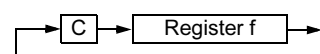
**Operation:** See description below

**Status Affected:** C

**Encoding:**

00	1100	dfff	ffff
----	------	------	------

**Description:** The contents of register 'f' are rotated one bit to the right through the Carry Flag. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'.



**Words:** 1

**Cycles:** 1

**Example** RRF REG1,0

**Before Instruction**

REG1 = 1110 0110  
 C = 0

**After Instruction**

REG1 = 1110 0110  
 W = 0111 0011  
 C = 0

## SLEEP

**Syntax:** [ *label* ] SLEEP ]

**Operands:** None

**Operation:** 00h → WDT,  
 0 → WDT prescaler,  
 1 →  $\overline{TO}$ ,  
 0 → PD

**Status Affected:**  $\overline{TO}$ , PD

**Encoding:**

00	0000	0110	0011
----	------	------	------

**Description:** The power-down STATUS bit, PD is cleared. Time-out STATUS bit,  $\overline{TO}$  is set. Watch-dog Timer and its prescaler are cleared.

The processor is put into SLEEP mode with the oscillator stopped. See Section 9.8 for more details.

**Words:** 1

**Cycles:** 1

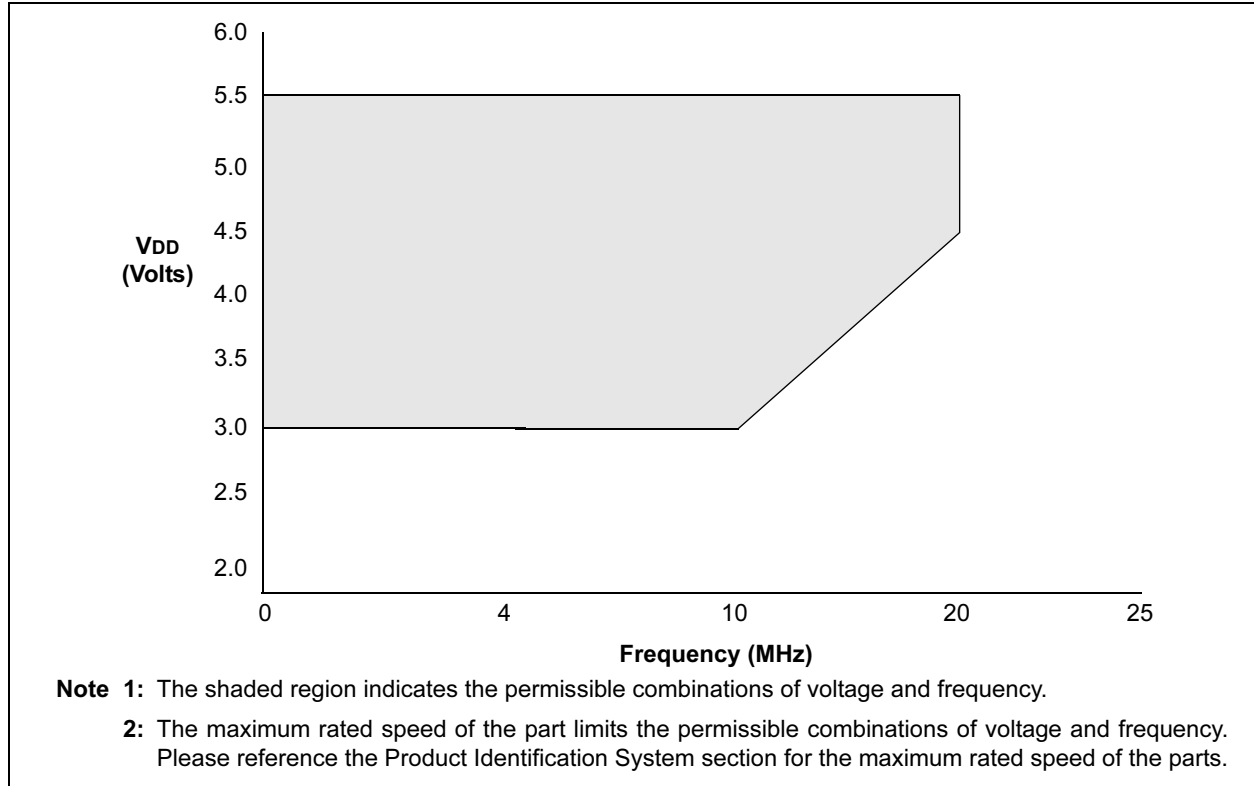
**Example:** SLEEP

# PIC16C62X

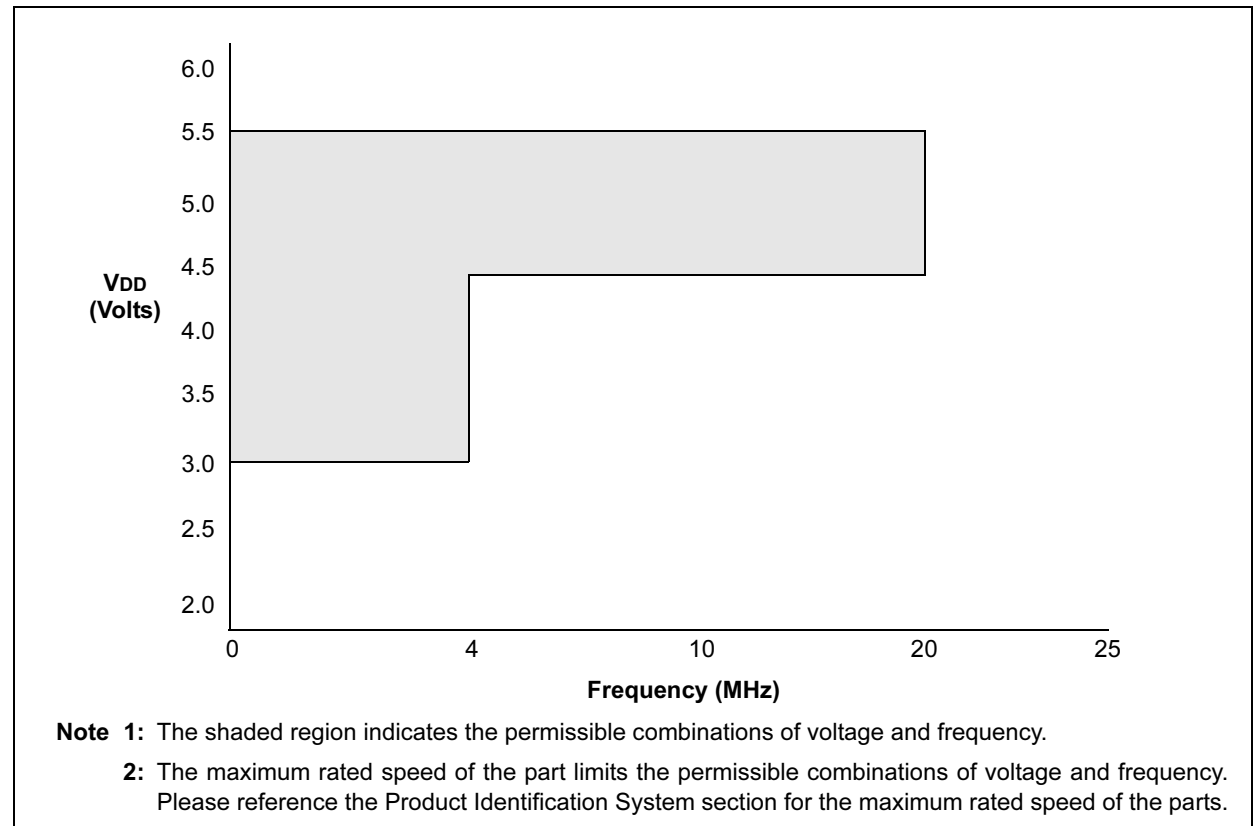
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NOTES:

**FIGURE 12-7: PIC16CR62XA VOLTAGE-FREQUENCY GRAPH,  $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$**



**FIGURE 12-8: PIC16CR62XA VOLTAGE-FREQUENCY GRAPH,  $-40^{\circ}\text{C} \leq T_A \leq 0^{\circ}\text{C}$ ,  $+70^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$**



# PIC16C62X

## 12.2 DC Characteristics: PIC16C62XA-04 (Commercial, Industrial, Extended) PIC16C62XA-20 (Commercial, Industrial, Extended) PIC16LC62XA-04 (Commercial, Industrial, Extended (CONT.))

PIC16C62XA			Standard Operating Conditions (unless otherwise stated)				
			Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial and -40°C ≤ TA ≤ +125°C for extended				
PIC16LC62XA			Standard Operating Conditions (unless otherwise stated)				
			Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial and -40°C ≤ TA ≤ +125°C for extended				
Param. No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D022	ΔI <sub>WDT</sub>	WDT Current <sup>(5)</sup>	—	6.0	10	μA	V <sub>DD</sub> = 4.0V (125°C)
D022A	ΔI <sub>BOR</sub>	Brown-out Reset Current <sup>(5)</sup>	—	75	125	μA	BOD enabled, V <sub>DD</sub> = 5.0V
D023	ΔI <sub>COMP</sub>	Comparator Current for each Comparator <sup>(5)</sup>	—	30	60	μA	V <sub>DD</sub> = 4.0V
D023A	ΔI <sub>VREF</sub>	VREF Current <sup>(5)</sup>	—	80	135	μA	V <sub>DD</sub> = 4.0V
D022	ΔI <sub>WDT</sub>	WDT Current <sup>(5)</sup>	—	6.0	10	μA	V <sub>DD</sub> =4.0V (125°C)
D022A	ΔI <sub>BOR</sub>	Brown-out Reset Current <sup>(5)</sup>	—	75	125	μA	BOD enabled, V <sub>DD</sub> = 5.0V
D023	ΔI <sub>COMP</sub>	Comparator Current for each Comparator <sup>(5)</sup>	—	30	60	μA	V <sub>DD</sub> = 4.0V
D023A	ΔI <sub>VREF</sub>	VREF Current <sup>(5)</sup>	—	80	135	μA	V <sub>DD</sub> = 4.0V
1A	FOSC	LP Oscillator Operating Frequency	0	—	200	kHz	All temperatures
		RC Oscillator Operating Frequency	0	—	4	MHz	All temperatures
		XT Oscillator Operating Frequency	0	—	4	MHz	All temperatures
		HS Oscillator Operating Frequency	0	—	20	MHz	All temperatures
1A	FOSC	LP Oscillator Operating Frequency	0	—	200	kHz	All temperatures
		RC Oscillator Operating Frequency	0	—	4	MHz	All temperatures
		XT Oscillator Operating Frequency	0	—	4	MHz	All temperatures
		HS Oscillator Operating Frequency	0	—	20	MHz	All temperatures

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** This is the limit to which V<sub>DD</sub> can be lowered without losing RAM data.

**2:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all I<sub>DD</sub> measurements in Active Operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tri-stated, pulled to V<sub>DD</sub>,

MCLR = V<sub>DD</sub>; WDT enabled/disabled as specified.

**3:** The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to V<sub>DD</sub> or V<sub>SS</sub>.

**4:** For RC osc configuration, current through R<sub>EXT</sub> is not included. The current through the resistor can be estimated by the formula: I<sub>r</sub> = V<sub>DD</sub>/2R<sub>EXT</sub> (mA) with R<sub>EXT</sub> in kΩ.

**5:** The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base I<sub>DD</sub> or I<sub>PD</sub> measurement.

**6:** Commercial temperature range only.



## 12.3 DC CHARACTERISTICS: PIC16CR62XA-04 (Commercial, Industrial, Extended) PIC16CR62XA-20 (Commercial, Industrial, Extended) PIC16LCR62XA-04 (Commercial, Industrial, Extended)

<b>PIC16CR62XA-04 PIC16CR62XA-20</b>			<b>Standard Operating Conditions (unless otherwise stated)</b> Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial and $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial and $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended				
<b>PIC16LCR62XA-04</b>			<b>Standard Operating Conditions (unless otherwise stated)</b> Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial and $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial and $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended				
Param. No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D001	VDD	Supply Voltage	3.0	—	5.5	V	See Figures 12-7, 12-8, 12-9
D001	VDD	Supply Voltage	2.5	—	5.5	V	See Figures 12-7, 12-8, 12-9
D002	VDR	RAM Data Retention Voltage <sup>(1)</sup>	—	1.5*	—	V	Device in SLEEP mode
D002	VDR	RAM Data Retention Voltage <sup>(1)</sup>	—	1.5*	—	V	Device in SLEEP mode
D003	VPOR	VDD start voltage to ensure Power-on Reset	—	VSS	—	V	See section on Power-on Reset for details
D003	VPOR	VDD start voltage to ensure Power-on Reset	—	VSS	—	V	See section on Power-on Reset for details
D004	SVDD	VDD rise rate to ensure Power-on Reset	0.05*	—	—	V/ms	See section on Power-on Reset for details
D004	SVDD	VDD rise rate to ensure Power-on Reset	0.05*	—	—	V/ms	See section on Power-on Reset for details
D005	VBOR	Brown-out Detect Voltage	3.7	4.0	4.35	V	BOREN configuration bit is cleared
D005	VBOR	Brown-out Detect Voltage	3.7	4.0	4.35	V	BOREN configuration bit is cleared
D010	IDD	Supply Current <sup>(2)</sup>	—	1.2	1.7	mA	FOSC = 4 MHz, VDD = 5.5V, WDT disabled, XT mode, (Note 4)*
			—	500	900	μA	FOSC = 4 MHz, VDD = 3.0V, WDT disabled, XT mode, (Note 4)
			—	1.0	2.0	mA	FOSC = 10 MHz, VDD = 3.0V, WDT disabled, HS mode, (Note 6)
			—	4.0	7.0	mA	FOSC = 20 MHz, VDD = 5.5V, WDT disabled*, HS mode
			—	3.0	6.0	mA	FOSC = 20 MHz, VDD = 4.5V, WDT disabled, HS mode
			—	35	70	μA	FOSC = 32 kHz, VDD = 3.0V, WDT disabled, LP mode
D010	IDD	Supply Current <sup>(2)</sup>	—	1.2	1.7	mA	FOSC = 4.0 MHz, VDD = 5.5V, WDT disabled, XT mode, (Note 4)*
			—	400	800	μA	FOSC = 4.0 MHz, VDD = 2.5V, WDT disabled, XT mode (Note 4)
			—	35	70	μA	FOSC = 32 kHz, VDD = 2.5V, WDT disabled, LP mode

# PIC16C62X

## 12.5 DC CHARACTERISTICS: PIC16C620A/C621A/C622A-40<sup>(7)</sup> (Commercial) PIC16CR620A-40<sup>(7)</sup> (Commercial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated)				
			Operating temperature 0°C ≤ TA ≤ +70°C for commercial				
Param No.	Sym	Characteristic	Min	Typ†	Max	Unit	Conditions
D030	V <sub>IL</sub>	<b>Input Low Voltage</b> I/O ports with TTL buffer	V <sub>SS</sub>	—	0.8V 0.15V <sub>DD</sub>	V	V <sub>DD</sub> = 4.5V to 5.5V, otherwise
D031		with Schmitt Trigger input	V <sub>SS</sub>	—	0.2V <sub>DD</sub>	V	(Note 1)
D032		MCLR, RA4/T0CKI, OSC1 (in RC mode)	V <sub>SS</sub>	—	0.2V <sub>DD</sub>	V	
D033		OSC1 (in XT and HS) OSC1 (in LP)	V <sub>SS</sub> V <sub>SS</sub>	— —	0.3V <sub>DD</sub> 0.6V <sub>DD</sub> - 1.0	V V	
D040	V <sub>IH</sub>	<b>Input High Voltage</b> I/O ports with TTL buffer	2.0V 0.25 V <sub>DD</sub> + 0.8	—	V <sub>DD</sub> V <sub>DD</sub>	V	V <sub>DD</sub> = 4.5V to 5.5V, otherwise
D041		with Schmitt Trigger input	0.8 V <sub>DD</sub>	—	V <sub>DD</sub>	V	(Note 1)
D042		MCLR RA4/T0CKI	0.8 V <sub>DD</sub>	—	V <sub>DD</sub>	V	
D043		OSC1 (XT, HS and LP)	0.7 V <sub>DD</sub>	—	V <sub>DD</sub>	V	
D043A		OSC1 (in RC mode)	0.9 V <sub>DD</sub>	—			(Note 1)
D070	IPURB	<b>PORTB Weak Pull-up Current</b>	50	200	400	μA	V <sub>DD</sub> = 5.0V, V <sub>PIN</sub> = V <sub>SS</sub>
D060	I <sub>IL</sub>	<b>Input Leakage Current</b> <sup>(2, 3)</sup> I/O ports (except PORTA)	—	—	±1.0	μA	V <sub>SS</sub> ≤ V <sub>PIN</sub> ≤ V <sub>DD</sub> , pin at hi-impedance
D061		PORTA	—	—	±0.5	μA	V <sub>SS</sub> ≤ V <sub>PIN</sub> ≤ V <sub>DD</sub> , pin at hi-impedance
D063		RA4/T0CKI	—	—	±1.0	μA	V <sub>SS</sub> ≤ V <sub>PIN</sub> ≤ V <sub>DD</sub>
		OSC1, MCLR	—	—	±5.0	μA	V <sub>SS</sub> ≤ V <sub>PIN</sub> ≤ V <sub>DD</sub> , XT, HS and LP osc configuration
D080	V <sub>OL</sub>	<b>Output Low Voltage</b> I/O ports	—	—	0.6	V	I <sub>OL</sub> = 8.5 mA, V <sub>DD</sub> = 4.5V, -40° to +85°C
			—	—	0.6	V	I <sub>OL</sub> = 7.0 mA, V <sub>DD</sub> = 4.5V, +125°C
D083		OSC2/CLKOUT (RC only)	—	—	0.6	V	I <sub>OL</sub> = 1.6 mA, V <sub>DD</sub> = 4.5V, -40° to +85°C
			—	—	0.6	V	I <sub>OL</sub> = 1.2 mA, V <sub>DD</sub> = 4.5V, +125°C
D090	V <sub>OH</sub>	<b>Output High Voltage</b> <sup>(3)</sup> I/O ports (except RA4)	V <sub>DD</sub> -0.7 V <sub>DD</sub> -0.7	— —	— —	V V	I <sub>OH</sub> = -3.0 mA, V <sub>DD</sub> = 4.5V, -40° to +85°C I <sub>OH</sub> = -2.5 mA, V <sub>DD</sub> = 4.5V, +125°C
D092		OSC2/CLKOUT (RC only)	V <sub>DD</sub> -0.7 V <sub>DD</sub> -0.7	— —	— —	V V	I <sub>OH</sub> = -1.3 mA, V <sub>DD</sub> = 4.5V, -40° to +85°C I <sub>OH</sub> = -1.0 mA, V <sub>DD</sub> = 4.5V, +125°C
*D150	V <sub>OD</sub>	<b>Open Drain High Voltage</b>			8.5	V	RA4 pin
D100	C <sub>osc2</sub>	<b>Capacitive Loading Specs on Output Pins</b> OSC2 pin			15	pF	In XT, HS and LP modes when external clock used to drive OSC1.
D101	C <sub>io</sub>	All I/O pins/OSC2 (in RC mode)			50	pF	

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** This is the limit to which V<sub>DD</sub> can be lowered in SLEEP mode without losing RAM data.

**Note 2:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all I<sub>DD</sub> measurements in Active Operation mode are:

OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to V<sub>DD</sub>, MCLR = V<sub>DD</sub>; WDT enabled/disabled as specified.

**Note 3:** The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to V<sub>DD</sub> or V<sub>SS</sub>.

**Note 4:** For RC osc configuration, current through R<sub>EXT</sub> is not included. The current through the resistor can be estimated by the formula  $I_r = V_{DD} / 2R_{EXT}$  (mA) with R<sub>EXT</sub> in kΩ.

**Note 5:** The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base I<sub>DD</sub> or I<sub>PD</sub> measurement.

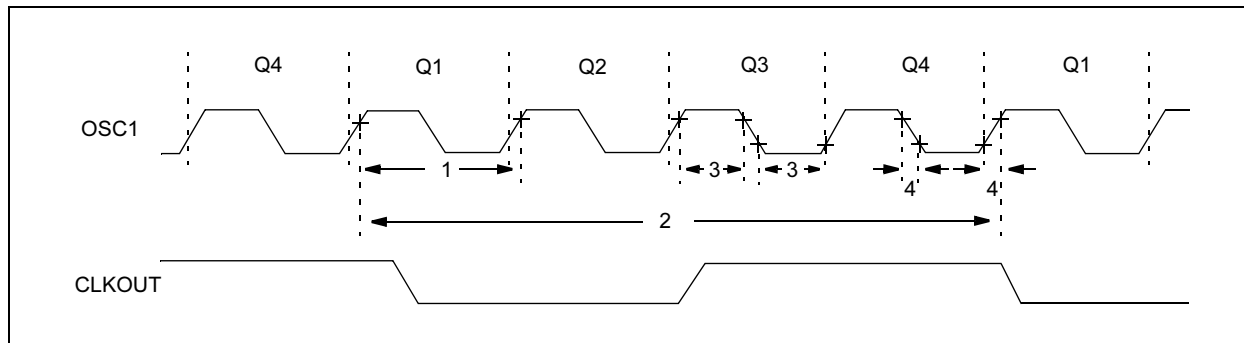
**Note 6:** Commercial temperature range only.

**Note 7:** See Section 12.1 and Section 12.3 for 16C62X and 16CR62X devices for operation between 20 MHz and 40 MHz for valid modified characteristics.

# PIC16C62X

## 12.9 Timing Diagrams and Specifications

**FIGURE 12-12: EXTERNAL CLOCK TIMING**



**TABLE 12-3: EXTERNAL CLOCK TIMING REQUIREMENTS**

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
1A	Fosc	External CLKIN Frequency <sup>(1)</sup>	DC	—	4	MHz	XT and RC Osc mode, VDD=5.0V
			DC	—	20	MHz	HS Osc mode
			DC	—	200	kHz	LP Osc mode
		Oscillator Frequency <sup>(1)</sup>	DC	—	4	MHz	RC Osc mode, VDD=5.0V
1	Tosc	External CLKIN Period <sup>(1)</sup>	0.1	—	4	MHz	XT Osc mode
			1	—	20	MHz	HS Osc mode
			DC	—	200	kHz	LP Osc mode
		Oscillator Period <sup>(1)</sup>	250	—	—	ns	RC Osc mode
			250	—	10,000	ns	XT Osc mode
			50	—	1,000	ns	HS Osc mode
2	Tcy	Instruction Cycle Time <sup>(1)</sup>	5	—	—	μs	LP Osc mode
			1.0	Fosc/4	DC	μs	Tcys=Fosc/4
			250	—	—	ns	XT oscillator, Tosc L/H duty cycle
3*	TosL, TosH	External Clock in (OSC1) High or Low Time	2*	—	—	μs	LP oscillator, Tosc L/H duty cycle
			20*	—	—	ns	HS oscillator, Tosc L/H duty cycle
			25*	—	—	ns	XT oscillator
4*	TosR, TosF	External Clock in (OSC1) Rise or Fall Time	50*	—	—	ns	LP oscillator
			15*	—	—	ns	HS oscillator
			25*	—	—	ns	XT oscillator

2: \* These parameters are characterized but not tested.

3: † Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** Instruction cycle period (Tcy) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1 pin. When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

FIGURE 13-5:  $I_{OH}$  vs.  $V_{OH}$ ,  $V_{DD} = 3.0V$

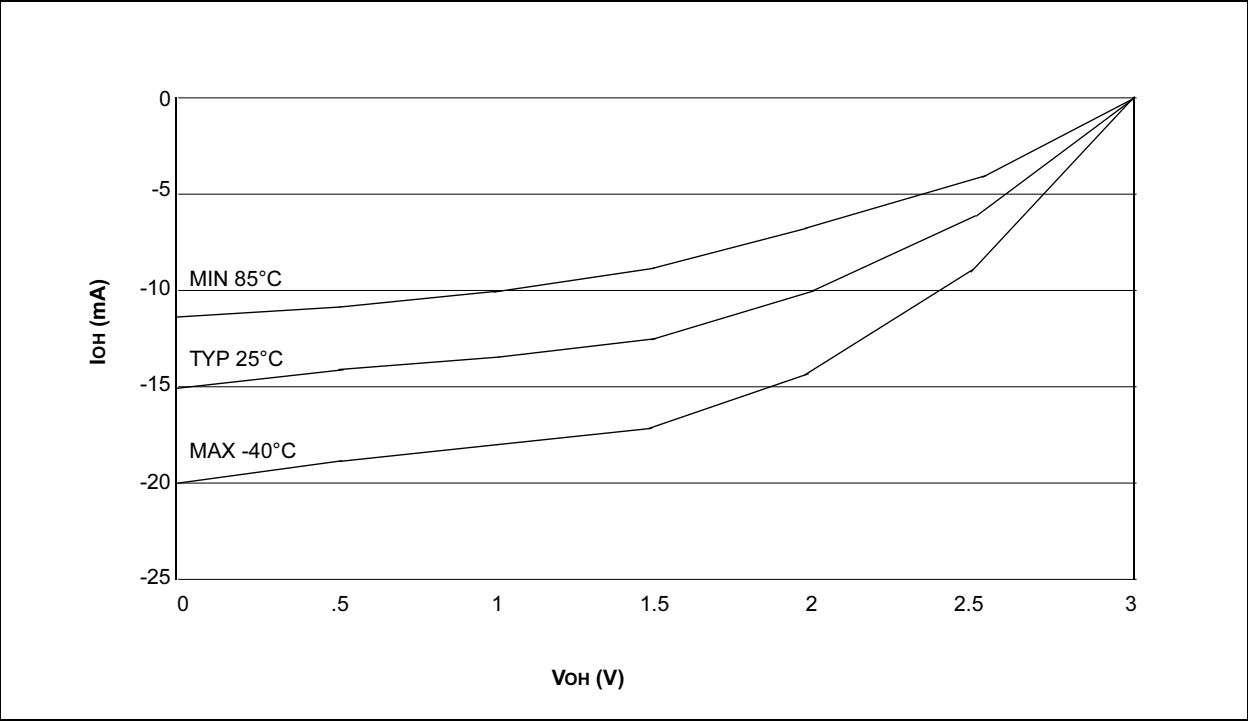
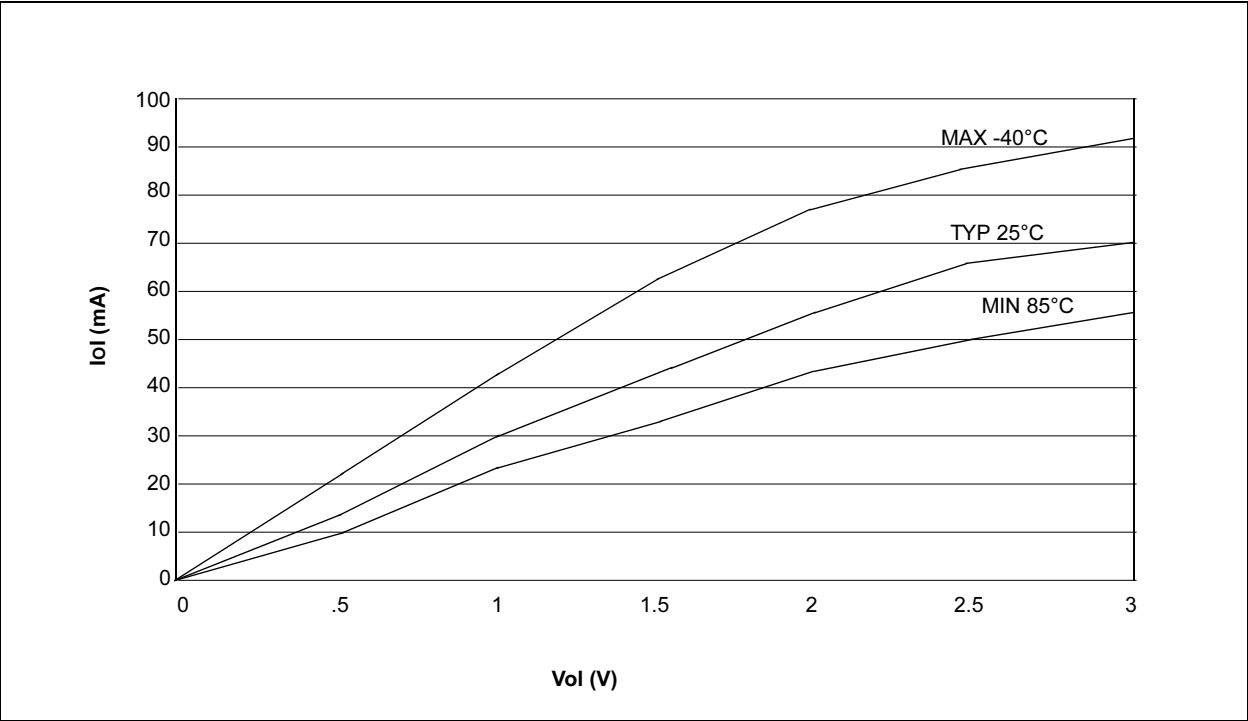


FIGURE 13-6:  $I_{OL}$  vs.  $V_{OL}$ ,  $V_{DD} = 5.5V$



## APPENDIX A: ENHANCEMENTS

The following are the list of enhancements over the PIC16C5X microcontroller family:

1. Instruction word length is increased to 14 bits. This allows larger page sizes both in program memory (4K now as opposed to 512 before) and register file (up to 128 bytes now versus 32 bytes before).
2. A PC high latch register (PCLATH) is added to handle program memory paging. PA2, PA1, PA0 bits are removed from STATUS register.
3. Data memory paging is slightly redefined. STATUS register is modified.
4. Four new instructions have been added: RETURN, RETFIE, ADDLW, and SUBLW. Two instructions TRIS and OPTION are being phased out, although they are kept for compatibility with PIC16C5X.
5. OPTION and TRIS registers are made addressable.
6. Interrupt capability is added. Interrupt vector is at 0004h.
7. Stack size is increased to 8 deep.
8. RESET vector is changed to 0000h.
9. RESET of all registers is revisited. Five different RESET (and wake-up) types are recognized. Registers are reset differently.
10. Wake-up from SLEEP through interrupt is added.
11. Two separate timers, Oscillator Start-up Timer (OST) and Power-up Timer (PWRT) are included for more reliable power-up. These timers are invoked selectively to avoid unnecessary delays on power-up and wake-up.
12. PORTB has weak pull-ups and interrupt-on-change feature.
13. Timer0 clock input, T0CKI pin is also a port pin (RA4/T0CKI) and has a TRIS bit.
14. FSR is made a full 8-bit register.
15. "In-circuit programming" is made possible. The user can program PIC16CXX devices using only five pins: VDD, VSS, VPP, RB6 (clock) and RB7 (data in/out).
16. PCON STATUS register is added with a Power-on-Reset (POR) STATUS bit and a Brown-out Reset STATUS bit (BOD).
17. Code protection scheme is enhanced such that portions of the program memory can be protected, while the remainder is unprotected.
18. PORTA inputs are now Schmitt Trigger inputs.
19. Brown-out Reset reset has been added.
20. Common RAM registers F0h-FFh implemented in bank1.

## APPENDIX B: COMPATIBILITY

To convert code written for PIC16C5X to PIC16CXX, the user should take the following steps:

1. Remove any program memory page select operations (PA2, PA1, PA0 bits) for CALL, GOTO.
2. Revisit any computed jump operations (write to PC or add to PC, etc.) to make sure page bits are set properly under the new scheme.
3. Eliminate any data memory page switching. Redefine data variables to reallocate them.
4. Verify all writes to STATUS, OPTION, and FSR registers since these have changed.
5. Change RESET vector to 0000h.