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#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	13
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c622t-20i-ss

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

NOTES:

		PIC16C620 <sup>(3)</sup>	PIC16C620A <sup>(1)(4)</sup>	PIC16CR620A <sup>(2)</sup>	PIC16C621 <sup>(3)</sup>	PIC16C621A <sup>(1)(4)</sup>	PIC16C622 <sup>(3)</sup>	PIC16C622A <sup>(1)(4)</sup>
Clock	Maximum Frequency of Operation (MHz)	20	40	20	20	40	20	40
Memory	EPROM Program Memory (x14 words)	512	512	512	1K	1K	2K	2K
	Data Memory (bytes)	80	96	96	80	96	128	128
Peripherals	Timer Module(s)	TMR0	TMR0	TMRO	TMR0	TMR0	TMR0	TMR0
	Comparators(s)	2	2	2	2	2	2	2
	Internal Reference Voltage	Yes						
Features	Interrupt Sources	4	4	4	4	4	4	4
	I/O Pins	13	13	13	13	13	13	13
	Voltage Range (Volts)	2.5-6.0	2.7-5.5	2.5-5.5	2.5-6.0	2.7-5.5	2.5-6.0	2.7-5.5
	Brown-out Reset	Yes						
	Packages	18-pin DIP, SOIC; 20-pin SSOP						

#### TABLE 1-1: PIC16C62X FAMILY OF DEVICES

All PICmicro<sup>®</sup> Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability. All PIC16C62X Family devices use serial programming with clock pin RB6 and data pin RB7.

**Note 1:** If you change from this device to another device, please verify oscillator characteristics in your application.

2: For ROM parts, operation from 2.0V - 2.5V will require the PIC16LCR62XA parts.

**3:** For OTP parts, operation from 2.5V - 3.0V will require the PIC16LC62X part.

4: For OTP parts, operation from 2.7V - 3.0V will require the PIC16LC62XA part.

NOTES:

# 3.1 Clocking Scheme/Instruction Cycle

The clock input (OSC1/CLKIN pin) is internally divided by four to generate four non-overlapping quadrature clocks namely Q1, Q2, Q3 and Q4. Internally, the program counter (PC) is incremented every Q1, the instruction is fetched from the program memory and latched into the instruction register in Q4. The instruction is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow is shown in Figure 3-2.

#### 3.2 Instruction Flow/Pipelining

An "Instruction Cycle" consists of four Q cycles (Q1, Q2, Q3 and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle while decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g., GOTO) then two cycles are required to complete the instruction (Example 3-1).

A fetch cycle begins with the program counter (PC) incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the "Instruction Register (IR)" in cycle Q1. This instruction is then decoded and executed during the Q2, Q3 and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).



#### FIGURE 3-2: CLOCK/INSTRUCTION CYCLE

#### EXAMPLE 3-1: INSTRUCTION PIPELINE FLOW



#### FIGURE 4-4: DATA MEMORY MAP FOR THE PIC16C620/621

File Address	3		File Address			
00h	INDF <sup>(1)</sup>	INDF <sup>(1)</sup>	80h			
01h	TMR0	OPTION	81h			
02h	PCL	PCL	82h			
03h	STATUS	STATUS	83h			
04h	FSR	FSR	84h			
05h	PORTA	TRISA	85h			
06h	PORTB	TRISB	86h			
07h			87h			
08h			88h			
09h			89h			
0Ah	PCLATH	PCLATH	8Ah			
0Bh	INTCON	INTCON	8Bh			
0Ch	PIR1	PIE1	8Ch			
0Dh			8Dh			
0Eh		PCON	8Eh			
0Fh			8Fh			
10h			90h			
11h			91h			
12h			92h			
13h			93h			
14h			94h			
15h			95h			
16h			96h			
17h			97h			
18h			98h			
19h			99h			
1Ah			9Ah			
1Bh			9Bh			
1Ch			9Ch			
1Dh			9Dh			
1Eh			9Eh			
1Fh	CMCON	VRCON	9Fh			
20h	Osmanal		A0h			
	Purpose					
6Eb	Register					
70n						
Į			_			
7Fh	Donk 0	Dorld 1	FFh			
	Dank U	Bank T				
Unimplemented data memory locations, read as '0'.						
Note 1:	Not a physical re	egister.				

## FIGURE 4-5:

#### DATA MEMORY MAP FOR THE PIC16C622

File Address	3		File Address		
00h	INDF <sup>(1)</sup>	INDF <sup>(1)</sup>	80h		
01h	TMR0	OPTION	81h		
02h	PCL	PCL	82h		
03h	STATUS	STATUS	83h		
04h	FSR	FSR	84h		
05h	PORTA	TRISA	85h		
06h	PORTB	TRISB	86h		
07h			87h		
08h			88h		
09h			89h		
0Ah	PCLATH	PCLATH	8Ah		
0Bh	INTCON	INTCON	8Bh		
0Ch	PIR1	PIE1	8Ch		
0Dh			8Dh		
0Eh		PCON	8Eh		
0Fh			8Fh		
10h			90h		
11h			91h		
12h			92h		
13h			93h		
14h			94h		
15h			95h		
16h			96h		
17h			97h		
18h			98h		
19h			99h		
1Ah			9Ah		
1Bh			9Bh		
1Ch			9Ch		
1Dh			9Dh		
1Eh			9Eh		
1Fh	CMCON	VRCON	9Fh		
20h			A0h		
	General	General	7.011		
	Purpose Register	Purpose Register			
	rtogiotor	rtogiotor	BFh		
			C0h		
7Fh			FFh		
,,,,,	Bank 0	Bank 1			
Unimp	plemented data me	mory locations, re	ead as '0'.		
Note 1:	Not a physical m	aistor			
Note 1: Not a physical register.					

#### 4.2.2.6 PCON Register

The PCON register contains flag bits to differentiate between a Power-on Reset, an external MCLR Reset, WDT Reset or a Brown-out Reset.

Note:	BOR is unknown on Power-on Reset. It						
	must then be set by the user and checked						
	on subsequent RESETS to see if BOR is						
	cleared, indicating a brown-out has						
	occurred. The $\overline{\text{BOR}}$ STATUS bit is a "don't						
	care" and is not necessarily predictable if						
	the brown-out circuit is disabled (by						
	programming BODEN bit in the						
	Configuration word).						

#### REGISTER 4-6: PCON REGISTER (ADDRESS 8Eh)

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	POR	BOR
bit 7							bit 0

bit 7-2 Unimplemented: Read as '0'

bit 1 **POR**: Power-on Reset STATUS bit

- 1 = No Power-on Reset occurred
- 0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)

bit 0 **BOR**: Brown-out Reset STATUS bit

1 = No Brown-out Reset occurred

0 = A Brown-out Reset occurred (must be set in software after a Brown-out Reset occurs)

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented	bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

## 4.3 PCL and PCLATH

The program counter (PC) is 13-bits wide. The low byte comes from the PCL register, which is a readable and writable register. The high byte (PC<12:8>) is not directly readable or writable and comes from PCLATH. On any RESET, the PC is cleared. Figure 4-8 shows the two situations for the loading of the PC. The upper example in the figure shows how the PC is loaded on a write to PCL (PCLATH<4:0>  $\rightarrow$  PCH). The lower example in the figure shows how the PC is loaded during a CALL or GOTO instruction (PCLATH<4:3>  $\rightarrow$  PCH).

#### FIGURE 4-8: LOADING OF PC IN DIFFERENT SITUATIONS



## 4.3.1 COMPUTED GOTO

A computed GOTO is accomplished by adding an offset to the program counter (ADDWF PCL). When doing a table read using a computed GOTO method, care should be exercised if the table location crosses a PCL memory boundary (each 256 byte block). Refer to the application note, *"Implementing a Table Read"* (AN556).

### 4.3.2 STACK

The PIC16C62X family has an 8-level deep x 13-bit wide hardware stack (Figure 4-2 and Figure 4-3). The stack space is not part of either program or data space and the stack pointer is not readable or writable. The PC is PUSHed onto the stack when a CALL instruction is executed or an interrupt causes a branch. The stack is POPed in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not affected by a PUSH or POP operation.

The stack operates as a circular buffer. This means that after the stack has been PUSHed eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on).

- Note 1: There are no STATUS bits to indicate stack overflow or stack underflow conditions.
  - 2: There are no instructions/mnemonics called PUSH or POP. These are actions that occur from the execution of the CALL, RETURN, RETLW and RETFIE instructions, or the vectoring to an interrupt address.

## 5.0 I/O PORTS

The PIC16C62X have two ports, PORTA and PORTB. Some pins for these I/O ports are multiplexed with an alternate function for the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

#### 5.1 PORTA and TRISA Registers

PORTA is a 5-bit wide latch. RA4 is a Schmitt Trigger input and an open drain output. Port RA4 is multiplexed with the T0CKI clock input. All other RA port pins have Schmitt Trigger input levels and full CMOS output drivers. All pins have data direction bits (TRIS registers), which can configure these pins as input or output.

A '1' in the TRISA register puts the corresponding output driver in a Hi-impedance mode. A '0' in the TRISA register puts the contents of the output latch on the selected pin(s).

Reading the PORTA register reads the status of the pins, whereas writing to it will write to the port latch. All write operations are read-modify-write operations. So a write to a port implies that the port pins are first read, then this value is modified and written to the port data latch.

The PORTA pins are multiplexed with comparator and voltage reference functions. The operation of these pins are selected by control bits in the CMCON (comparator control register) register and the VRCON (voltage reference control register) register. When selected as a comparator input, these pins will read as '0's.

#### FIGURE 5-1: BLOCK DIAGRAM OF RA1:RA0 PINS



Note:	On RESET, the TRISA register is set to all
	inputs. The digital inputs are disabled and
	the comparator inputs are forced to ground
	to reduce excess current consumption.

TRISA controls the direction of the RA pins, even when they are being used as comparator inputs. The user must make sure to keep the pins configured as inputs when using them as comparator inputs.

The RA2 pin will also function as the output for the voltage reference. When in this mode, the VREF pin is a very high impedance output and must be buffered prior to any external load. The user must configure TRISA<2> bit as an input and use high impedance loads.

In one of the Comparator modes defined by the CMCON register, pins RA3 and RA4 become outputs of the comparators. The TRISA<4:3> bits must be cleared to enable outputs to use this function.

#### EXAMPLE 5-1: INITIALIZING PORTA

CLRF	PORTA	;Initialize PORTA by setting ;output data latches
MOVLW	0X07	;Turn comparators off and
MOVWF	CMCON	;enable pins for I/O ;functions
BSF	STATUS, RPO	;Select Bank1
MOVLW	0x1F	;Value used to initialize
		;data direction
MOVWF	TRISA	;Set RA<4:0> as inputs
		;TRISA<7:5> are always
		;read as '0'.

#### FIGURE 5-2: BLOCK DIAGRAM OF RA2 PIN



# PIC16C62X









#### 8.0 **VOLTAGE REFERENCE** MODULE

The Voltage Reference is a 16-tap resistor ladder network that provides a selectable voltage reference. The resistor ladder is segmented to provide two ranges of VREF values and has a power-down function to conserve power when the reference is not being used. The VRCON register controls the operation of the reference as shown in Register 8-1. The block diagram is given in Figure 8-1.

#### 8.1 **Configuring the Voltage Reference**

The Voltage Reference can output 16 distinct voltage levels for each range. The equations used to calculate the output of the Voltage Reference are as follows:

if VRR = 0: VREF = (VDD x 1/4) + (VR<3:0>/32) x VDD

The setting time of the Voltage Reference must be considered when changing the VREF output (Table 12-1). Example 8-1 shows an example of how to configure the Voltage Reference for an output voltage of 1.25V with VDD = 5.0V.

	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	
	VREN	VROE	Vrr	_	VR3	VR2	VR1	Vr0	
	bit 7							bit 0	
bit 7	VREN: VREI 1 = VREF C	F Enable ircuit power	ed on						
	0 = VREF C	ircuit powere	ed down, no	IDD drain					
bit 6	VROE: VREF Output Enable								
	1 = VREF IS 0 = VREF IS	s output on F s disconnect	cA2 pin ed from RA2	2 pin					
bit 5 VRR: VREF Range selection									
	1 = Low Ra	ange							
hit 1		ange	d aa '0'						
DIC 4	Unimplem	ented: Rea	das U						
bit 3-0	VR<3:0>: \	/REF value s	election $0 \leq$	VR [3:0] ≤ 1	5				
	when VRR	= 1: VREF =	(VR<3:0>/ 2	4) * VDD	0) + ) /				
	when VRR	= 0: VREF =	1/4 ^ VDD +	(VR<3:0>/ 3	2) ^ VDD				
	Legend:								
	R = Reada	ıble bit	W = W	/ritable bit	U = Unin	nplemented	bit, read as	'0'	
	- n = Value	at POR	'1' = B	it is set	'0' = Bit i	s cleared	x = Bit is u	Inknown	
8-1:	VOLTAGE			K DIAGR	۸M				
			16 \$	Stages					
$\sim$	T			∕		_			
$\rightarrow$	-여드 <sub>8R</sub>	R	R	R	R				
				۸ ۸ ۸	A A A				

#### **REGISTER 8-1:** VRCON REGISTER(ADDRESS 9Fh)

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented I	bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

#### **FIGURE 8-**



#### EXAMPLE 8-1: VOLTAGE REFERENCE CONFIGURATION

MOVLW	0x02	; 4 Inputs Muxed
MOVWF	CMCON	; to 2 comps.
BSF	STATUS, RPO	; go to Bank 1
MOVLW	0x0F	; RA3-RA0 are
MOVWF	TRISA	; inputs
MOVLW	0xA6	; enable VREF
MOVWF	VRCON	; low range
		; set VR<3:0>=6
BCF	STATUS, RPO	; go to Bank O
CALL	DELAY10	; 10µs delay

#### 8.2 Voltage Reference Accuracy/Error

The full range of VSS to VDD cannot be realized due to the construction of the module. The transistors on the top and bottom of the resistor ladder network (Figure 8-1) keep VREF from approaching VSS or VDD. The voltage reference is VDD derived and therefore, the VREF output changes with fluctuations in VDD. The tested absolute accuracy of the voltage reference can be found in Table 12-2.

## 8.3 Operation During SLEEP

When the device wakes up from SLEEP through an interrupt or a Watchdog Timer time-out, the contents of the VRCON register are not affected. To minimize current consumption in SLEEP mode, the voltage reference should be disabled.

## 8.4 Effects of a RESET

A device RESET disables the voltage reference by clearing bit VREN (VRCON<7>). This reset also disconnects the reference from the RA2 pin by clearing bit VROE (VRCON<6>) and selects the high voltage range by clearing bit VRR (VRCON<5>). The VREF value select bits, VRCON<3:0>, are also cleared.

#### 8.5 Connection Considerations

The voltage reference module operates independently of the comparator module. The output of the reference generator may be connected to the RA2 pin if the TRISA<2> bit is set and the VROE bit, VRCON<6>, is set. Enabling the voltage reference output onto the RA2 pin with an input signal present will increase current consumption. Connecting RA2 as a digital output with VREF enabled will also increase current consumption.

The RA2 pin can be used as a simple D/A output with limited drive capability. Due to the limited drive capability, a buffer must be used in conjunction with the voltage reference output for external connections to VREF. Figure 8-2 shows an example buffering technique.

# FIGURE 8-2: VOLTAGE REFERENCE OUTPUT BUFFER EXAMPLE

#### TABLE 8-1: REGISTERS ASSOCIATED WITH VOLTAGE REFERENCE

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value On POR	Value On All Other RESETS
9Fh	VRCON	VREN	VROE	VRR		VR3	VR2	VR1	VR0	000- 0000	000- 0000
1Fh	CMCON	C2OUT	C10UT	_	-	CIS	CM2	CM1	CM0	00 0000	00 0000
85h	TRISA	_	_	_	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	1 1111	1 1111

**Note:** - = Unimplemented, read as "0"

#### 9.4.5 TIME-OUT SEQUENCE

On power-up the time-out sequence is as follows: First PWRT time-out is invoked after POR has expired. Then OST is activated. The total time-out will vary based on oscillator configuration and <u>PWRTE</u> bit status. For example, in RC mode with <u>PWRTE</u> bit erased (<u>PWRT</u> disabled), there will be no time-out at all. Figure 9-8, Figure 9-9 and Figure 9-10 depict time-out sequences.

Since the time-outs occur from the POR pulse, if  $\overline{\text{MCLR}}$  is kept low long enough, the time-outs will expire. Then bringing  $\overline{\text{MCLR}}$  high will begin execution immediately (see Figure 9-9). This is useful for testing purposes or to synchronize more than one PIC16C62X device operating in parallel.

Table 9-4 shows the RESET conditions for some special registers, while Table 9-5 shows the RESET conditions for all the registers.

#### 9.4.6 POWER CONTROL (PCON)/ STATUS REGISTER

The power control/STATUS register, PCON (address 8Eh), has two bits.

Bit0 is  $\overline{\text{BOR}}$  (Brown-out).  $\overline{\text{BOR}}$  is unknown on Poweron Reset. It must then be set by the user and checked on subsequent RESETS to see if  $\overline{\text{BOR}} = 0$ , indicating that a brown-out has occurred. The  $\overline{\text{BOR}}$  STATUS bit is a don't care and is not necessarily predictable if the brown-out circuit is disabled (by setting BODEN bit = 0 in the Configuration word).

Bit1 is POR (Power-on Reset). It is a '0' on Power-on Reset and unaffected otherwise. The user must write a '1' to this bit following a Power-on Reset. On a subsequent RESET, if POR is '0', it will indicate that a Power-on Reset must have occurred (VDD may have gone too low).

Oscillator Configuration	Powe	er-up	Brown-out Reset	Wake-up	
	PWRTE = 0	PWRTE = 1	Brown-out Reset	from SLEEP	
XT, HS, LP	72 ms + 1024 Tosc	1024 Tosc	72 ms + 1024 Tosc	1024 Tosc	
RC	72 ms	_	72 ms	_	

#### TABLE 9-1: TIME-OUT IN VARIOUS SITUATIONS

TABLE 9-2:	STATUS/PCON BITS AND THEIR SIGNIFICANCE

POR	BOR	то	PD	
0	Х	1	1	Power-on Reset
0	Х	0	Х	Illegal, TO is set on POR
0	Х	Х	0	Illegal, PD is set on POR
1	0	Х	Х	Brown-out Reset
1	1	0	u	WDT Reset
1	1	0	0	WDT Wake-up
1	1	u	u	MCLR Reset during normal operation
1	1	1	0	MCLR Reset during SLEEP

Legend: u = unchanged, x = unknown

#### TABLE 9-3: SUMMARY OF REGISTERS ASSOCIATED WITH BROWN-OUT

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR Reset	Value on all other RESETS <sup>(1)</sup>
83h	STATUS				TO	PD				0001 1xxx	000q quuu
8Eh	PCON							POR	BOR	0x	uq

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0', q = value depends on condition.

**Note 1:** Other (non Power-up) Resets include MCLR Reset, Brown-out Reset and Watchdog Timer Reset during normal operation.

### 9.7 Watchdog Timer (WDT)

The Watchdog Timer is a free running on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the RC oscillator of the CLKIN pin. That means that the WDT will run, even if the clock on the OSC1 and OSC2 pins of the device has been stopped, for example, by execution of a SLEEP instruction. During normal operation, a WDT time-out generates a device RESET. If the device is in SLEEP mode, a WDT time-out causes the device to wake-up and continue with normal operation. The WDT can be permanently disabled by programming the configuration bit WDTE as clear (Section 9.1).

#### 9.7.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms, (with no prescaler). The time-out periods vary with temperature, VDD and process variations from part to part (see

DC specs). If longer time-out periods are desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT under software control by writing to the OPTION register. Thus, time-out periods up to 2.3 seconds can be realized.

The CLRWDT and SLEEP instructions clear the WDT and the postscaler, if assigned to the WDT, and prevent it from timing out and generating a device RESET.

The  $\overline{\text{TO}}$  bit in the STATUS register will be cleared upon a Watchdog Timer time-out.

#### 9.7.2 WDT PROGRAMMING CONSIDERATIONS

It should also be taken in account that under worst case conditions (VDD = Min., Temperature = Max., max. WDT prescaler) it may take several seconds before a WDT time-out occurs.



#### FIGURE 9-17: WATCHDOG TIMER BLOCK DIAGRAM

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR Reset	Value on all other RESETS
2007h	Config. bits	—	BODEN	CP1	CP0	PWRTE	WDTE	FOSC1	FOSC0	—	—
81h	OPTION	RBPU	INTEDG	TOCS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111

Legend: Shaded cells are not used by the Watchdog Timer.

**Note:** – = Unimplemented location, read as "0"

+ = Reserved for future use

#### 9.8 Power-Down Mode (SLEEP)

The Power-down mode is entered by executing a SLEEP instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the PD bit in the STATUS register is cleared, the TO bit is set, and the oscillator driver is turned off. The I/O ports maintain the status they had, before SLEEP was executed (driving high, low, or hi-impedance).

For lowest current consumption in this mode, all I/O pins should be either at VDD or VSs with no external circuitry drawing current from the I/O pin and the comparators and VREF should be disabled. I/O pins that are hi-impedance inputs should be pulled high or low externally to avoid switching currents caused by floating inputs. The TOCKI input should also be at VDD or VSs for lowest current consumption. The contribution from on chip pull-ups on PORTB should be considered.

The MCLR pin must be at a logic high level (VIHMC).

Note:	It should be noted that a RESET generated
	by a WDT time-out does not drive MCLR
	pin low.

#### 9.8.1 WAKE-UP FROM SLEEP

The device can wake-up from SLEEP through one of the following events:

- 1. External RESET input on MCLR pin
- 2. Watchdog Timer Wake-up (if WDT was enabled)
- 3. Interrupt from RB0/INT pin, RB Port change, or the Peripheral Interrupt (Comparator).

The first event will cause a device RESET. The two latter events are considered a continuation of program execution. The TO and PD bits in the STATUS register can be used to determine the cause of device RESET. PD bit, which is set on power-up, is cleared when SLEEP is invoked. TO bit is cleared if WDT wake-up occurred.

When the SLEEP instruction is being executed, the next instruction (PC + 1) is pre-fetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set (enabled). Wake-up is regardless of the state of the GIE bit. If the GIE bit is clear (disabled), the device continues execution at the instruction after the SLEEP instruction. If the GIE bit is set (enabled), the device executes the instruction after the SLEEP instruction after the SLEEP instruction after the instruction and then branches to the interrupt address (0004h). In cases where the execution of the instruction following SLEEP is not desirable, the user should have an NOP after the SLEEP instruction.

**Note:** If the global interrupts are disabled (GIE is cleared), but any interrupt source has both its interrupt enable bit and the corresponding interrupt flag bits set, the device will immediately wake-up from SLEEP. The SLEEP instruction is completely executed.

The WDT is cleared when the device wakes up from SLEEP, regardless of the source of wake-up.

Q1 Q2 Q3 Q4 Q1 Q2 Q3 Q4	4 Q1	Q1 Q2 Q3 Q4	Q1 Q2 Q3 Q4	Q1 Q2 Q3 Q4	Q1 Q2 Q3 Q4
CLKOUT(4)	Tost(2	)/	\/	\/'\	'
INT pin		1	ı ı ı ı	1	I
INTE flag	\		I I		
(INTCON<1>)	∕_	Interrupt Latend	şy		
	<u>i</u>	(Note 2)	i		
(INTCON<7>)	Processor in	1		<u> </u>	<u> </u>
	SLEEP	1	I I	i	i i
INSTRUCTION FLOW		1	і і і і	1	1
PC X PC+1	X PC+2	X PC+2	X PC + 2	<u>x 0004h x</u>	0005h
$\begin{array}{c} \mbox{Instruction} \\ \mbox{fetched} \end{array} \Big\{ \begin{array}{c} \mbox{Inst}(\mbox{PC}) = \mbox{SLEEP} & \mbox{Inst}(\mbox{PC} + 1) \end{array} \right.$		Inst(PC + 2)	       	Inst(0004h)	Inst(0005h)
Instruction { Inst(PC - 1) SLEEP	1 1 1	Inst(PC + 1)	Dummy cycle	Dummy cycle	Inst(0004h)
Note 1: XT, HS or LP Oscillator mode 2: Tos⊤ = 1024Tosc (drawing n	e assumed. ot to scale) This	delay will not be	e there for RC	Osc mode.	

#### FIGURE 9-18: WAKE-UP FROM SLEEP THROUGH INTERRUPT

**3:** GIE = '1' assumed. In this case, after wake-up, the processor jumps to the interrupt routine. If GIE = '0', execution will continue in-line.

4: CLKOUT is not available in these Osc modes, but shown here for timing reference.

# PIC16C62X

INCFSZ	Increment f, Skip if 0	IORWF	Inclusive OR W with f
Syntax:	[label] INCFSZ f,d	Syntax:	[ <i>label</i> ] IORWF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$	Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d  \in  [0,1] \end{array}$
Operation:	(f) + 1 $\rightarrow$ (dest), skip if result = 0	Operation:	(W) .OR. (f) $\rightarrow$ (dest)
Status Affected:	None	Status Affected:	Z
Encoding:	00 1111 dfff ffff	Encoding:	00 0100 dfff ffff
Description:	The contents of register 'f' are incremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'.	Description:	Inclusive OR the W register with register 'f'. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.
	If the result is 0, the next instruc-	Words:	1
	discarded. A NOP is executed	Cycles:	1
	instead making it a two-cycle	Example	IORWF RESULT, 0
	Instruction.		Before Instruction
vvoras:	1		$\begin{array}{rcl} RESULI &= & 0x13 \\ W &= & 0x91 \end{array}$
Cycles: Example	1(2) HERE INCFSZ CNT, 1 GOTO LOOP CONTINUE • •		After Instruction $\begin{array}{rcl} RESULT &= & 0x13 \\ W &  = & 0x93 \\ Z &  = & 1 \end{array}$
	Before Instruction	MOVLW	Move Literal to W
	PC = address HERE After Instruction	Syntax:	[ <i>label</i> ] MOVLW k
	CNT = CNT + 1	Operands:	$0 \le k \le 255$
	if $CNT = 0$ , PC = address CONTINUE	Operation:	$k \rightarrow (W)$
	if $CNT \neq 0$ ,	Status Affected:	None
	PC = address HERE +1	Encoding:	11 00xx kkkk kkkk
IORLW	Inclusive OR Literal with W	Description:	The eight bit literal 'k' is loaded into W register. The don't cares will assemble as 0's.
Syntax:	[ <i>label</i> ] IORLW k	Words:	1
Operands:	$0 \le k \le 255$	Cycles:	1
Operation:	(W) .OR. $k \rightarrow$ (W)	Example	MOVLW 0x5A
Status Affected:	Z	·	After Instruction
Encoding:	11 1000 kkkk kkkk		W = 0x5A
Description:	The contents of the W register is OR'ed with the eight bit literal 'k'. The result is placed in the W register.		
Words:	1		
Cycles:	1		
Example	IORLW 0x35		
	Before Instruction W = 0x9A		
	After Instruction		

W = Z =

0xBF 1 NOTES:

# PIC16C62X





**2**: The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.





#### 12.2 DC Characteristics: PIC16C62XA-04 (Commercial, Industrial, Extended) PIC16C62XA-20 (Commercial, Industrial, Extended) PIC16LC62XA-04 (Commercial, Industrial, Extended) (CONT.)

PIC16C62XA			Standard Operating Conditions (unless otherwise stated)Operating temperature $-40^{\circ}$ C $\leq TA \leq +85^{\circ}$ C for industrial and $0^{\circ}$ C $\leq TA \leq +70^{\circ}$ C for commercial and $-40^{\circ}$ C $\leq TA \leq +125^{\circ}$ C for extended							
PIC16LC62XA				dard O ating te	<b>perati</b> empera	ng Con ature -4 -4	$\begin{array}{ll} \mbox{ditions (unless otherwise stated)} \\ 10^{\circ}C &\leq TA \leq +85^{\circ}C \mbox{ for industrial and} \\ 0^{\circ}C &\leq TA \leq +70^{\circ}C \mbox{ for commercial and} \\ 0^{\circ}C &\leq TA \leq +125^{\circ}C \mbox{ for extended} \end{array}$			
Param. No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions			
D010	IDD	Supply Current <sup>(2, 4)</sup>	-	1.2 0.4	2.0 1.2	mA mA	Fosc = 4 MHz, VDD = 5.5V, WDT disabled, XT mode, (Note 4)* Fosc = 4 MHz, VDD = 3.0V, WDT disabled, XT mode (Note 4)*			
				1.0 4.0	2.0 6.0	mA mA	Fosc = 10 MHz, VDD = 3.0V, WDT dis- abled, HS mode, (Note 6) Fosc = 20 MHz, VDD = 4.5V, WDT dis-			
			-	4.0 35	7.0 70	mA μA	abled, HS mode Fosc = 20 MHz, VDD = 5.5V, WDT dis- abled*, HS mode Fosc = 32 kHz, VDD = 3.0V, WDT dis- abled. LP mode			
D010	IDD	Supply Current <sup>(2)</sup>	_	1.2	2.0 1.1	mA mA	Fosc = 4 MHz, VDD = 5.5V, WDT disabled, XT mode, (Note 4)* Fosc = 4 MHz, VDD = 2.5V, WDT disabled, XT mode, (Note 4)			
			_	35	70	μA	Fosc = 32 kHz, VDD = 2.5V, WDT dis- abled, LP mode			
D020	IPD	Power-down Current <sup>(3)</sup>	   		2.2 5.0 9.0 15	μΑ μΑ μΑ μΑ	VDD = 3.0V VDD = 4.5V* VDD = 5.5V VDD = 5.5V Extended Temp.			
D020	IPD	Power-down Current <sup>(3)</sup>	     	 	2.0 2.2 9.0 15	μΑ μΑ μΑ μΑ	VDD = 2.5V VDD = 3.0V* VDD = 5.5V VDD = 5.5V Extended Temp.			

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in Active Operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tri-stated, pulled to VDD,

MCLR = VDD; WDT enabled/disabled as specified.

**3:** The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or Vss.

4: For RC osc configuration, current through REXT is not included. The current through the resistor can be estimated by the formula: Ir = VDD/2REXT (mA) with REXT in kΩ.

5: The ∆ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

6: Commercial temperature range only.

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## **PRODUCT IDENTIFICATION SYSTEM**

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	<u>-xx</u>	¥	<u>/xx</u>	xxx	Ex	camples:
Device	Frequency Range	Temperature Range	Package	Pattern	a)	PIC16C621A - 04/P 301 = Commercial temp PDIP package, 4 MHz, normal VDD limits, QT pattern #301.
Device Frequency Range	PIC16C6 PIC16C6 PIC16C6 PIC16LC PIC16LC PIC16LC PIC16LC PIC16LC PIC16CF PIC16CC PIC16LC 04 200 04 4 M 20 20 M	52X: VDD range 3.0 52XT: VDD range 3.0 52XA: VDD range 3.0 52XA: VDD range 2.5 52XX: VDD range 2.5 562X: VDD range 2.5 562X: VDD range 2.5 562XA: VDD range 2.5 572XA: V	/ to 6.0V IV to 6.0V (Tape DV to 5.5V .0V to 5.5V (Tap .5V to 6.0V .5V to 6.0V 2.5V to 5.5V 2.5V to 5.5V (Ta .5V to 5.5V 2.5V to 5.5V (Ta 2.5V to 5.5V (Ta 3.5V to 5.5V (Ta) 3.5V to	e and Reel) be and Reel) be and Reel) ape and Reel) ape and Reel) Tape and Reel)	) )	PIC16LC622- 04I/SO = Industrial temp., SOI package, 200 kHz, extended VDD limits.
emperature Range	e - = I = E =	0°C to +70°C -40°C to +85°C -40°C to +125°C				
Package	P = SO = SS = JW* =	PDIP SOIC (Gull Wing, SSOP (209 mil) Windowed CERD	300 mil body) NP			
Pattern	3-Digit Pa	attern Code for QTF	P (blank otherwi	se)		

\* JW Devices are UV erasable and can be programmed to any device configuration. JW Devices meet the electrical requirement of each oscillator type.

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