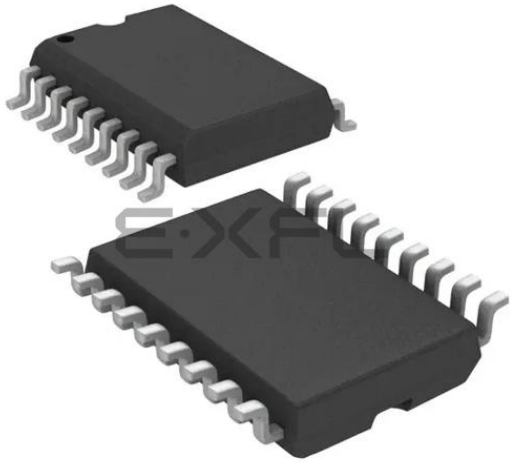

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	13
Program Memory Size	896B (512 x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	96 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	18-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lc620a-04i-so

Device Differences

Device	Voltage Range	Oscillator	Process Technology (Microns)
PIC16C620(3)	2.5 - 6.0	See **Note 1**	0.9
PIC16C621(3)	2.5 - 6.0	See **Note 1**	0.9
PIC16C622(3)	2.5 - 6.0	See **Note 1**	0.9
PIC16C620A(4)	2.7 - 5.5	See **Note 1**	0.7
PIC16CR620A(2)	2.5 - 5.5	See **Note 1**	0.7
PIC16C621A(4)	2.7 - 5.5	See **Note 1**	0.7
PIC16C622A(4)	2.7 - 5.5	See **Note 1**	0.7

Note 1: If you change from this device to another device, please verify oscillator characteristics in your application.

2: For ROM parts, operation from 2.5V - 3.0V will require the PIC16LCR62X parts.

3: For OTP parts, operation from 2.5V - 3.0V will require the PIC16LC62X parts.

4: For OTP parts, operations from 2.7V - 3.0V will require the PIC16LC62XA parts.

2.0 PIC16C62X DEVICE VARIETIES

A variety of frequency ranges and packaging options are available. Depending on application and production requirements, the proper device option can be selected using the information in the PIC16C62X Product Identification System section at the end of this data sheet. When placing orders, please use this page of the data sheet to specify the correct part number.

2.1 UV Erasable Devices

The UV erasable version, offered in CERDIP package, is optimal for prototype development and pilot programs. This version can be erased and reprogrammed to any of the Oscillator modes.

Microchip's PICSTART® and PRO MATE® programmers both support programming of the PIC16C62X.

Note:	Microchip does not recommend code protecting windowed devices.

2.2 One-Time-Programmable (OTP) Devices

The availability of OTP devices is especially useful for customers who need the flexibility for frequent code updates and small volume applications. In addition to the program memory, the configuration bits must also be programmed.

2.3 Quick-Turnaround-Production (QTP) Devices

Microchip offers a QTP programming service for factory production orders. This service is made available for users who chose not to program a medium to high quantity of units and whose code patterns have stabilized. The devices are identical to the OTP devices, but with all EPROM locations and configuration options already programmed by the factory. Certain code and prototype verification procedures apply before production shipments are available. Please contact your Microchip Technology sales office for more details.

2.4 Serialized Quick-Turnaround-Production℠ (SQTP℠) Devices

Microchip offers a unique programming service where a few user-defined locations in each device are programmed with different serial numbers. The serial numbers may be random, pseudo-random or sequential.

Serial programming allows each device to have a unique number, which can serve as an entry-code, password or ID number.

4.0 MEMORY ORGANIZATION

4.1 Program Memory Organization

The PIC16C62X has a 13-bit program counter capable of addressing an 8K x 14 program memory space. Only the first 512 x 14 (0000h - 01FFh) for the PIC16C620(A) and PIC16CR620, 1K x 14 (0000h - 03FFh) for the PIC16C621(A) and 2K x 14 (0000h - 07FFh) for the PIC16C622(A) are physically implemented. Accessing a location above these boundaries will cause a wrap-around within the first 512 x 14 space (PIC16C(R)620(A)) or 1K x 14 space (PIC16C621(A)) or 2K x 14 space (PIC16C622(A)). The RESET vector is at 0000h and the interrupt vector is at 0004h (Figure 4-1, Figure 4-2, Figure 4-3).

FIGURE 4-1: PROGRAM MEMORY MAP AND STACK FOR THE PIC16C620/PIC16C620A/ PIC16CR620A

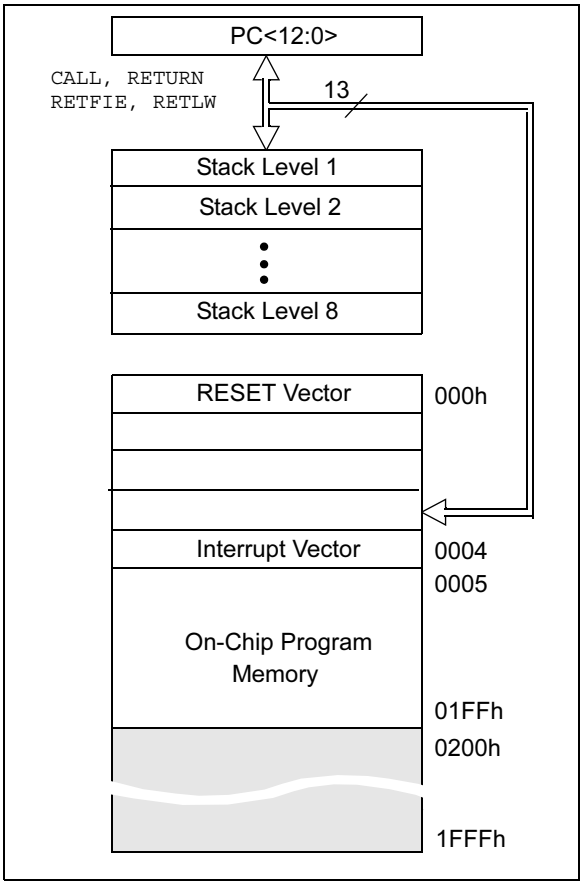


FIGURE 4-2: PROGRAM MEMORY MAP AND STACK FOR THE PIC16C621/PIC16C621A

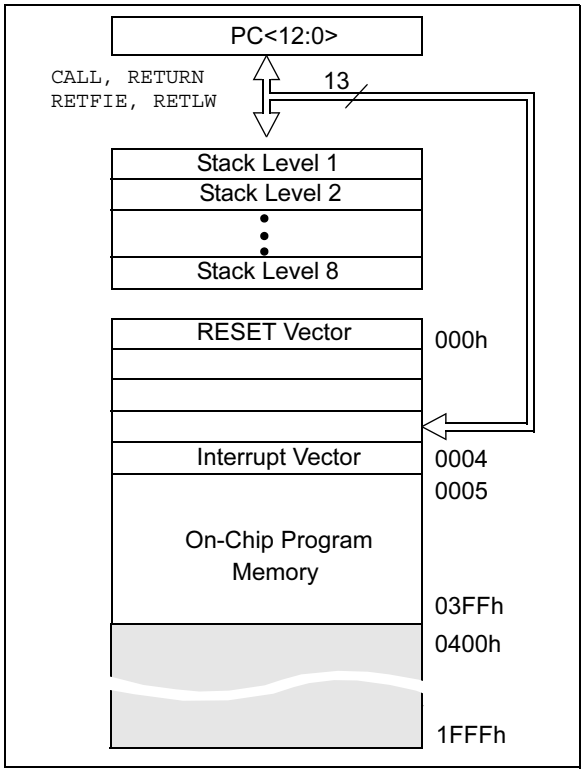
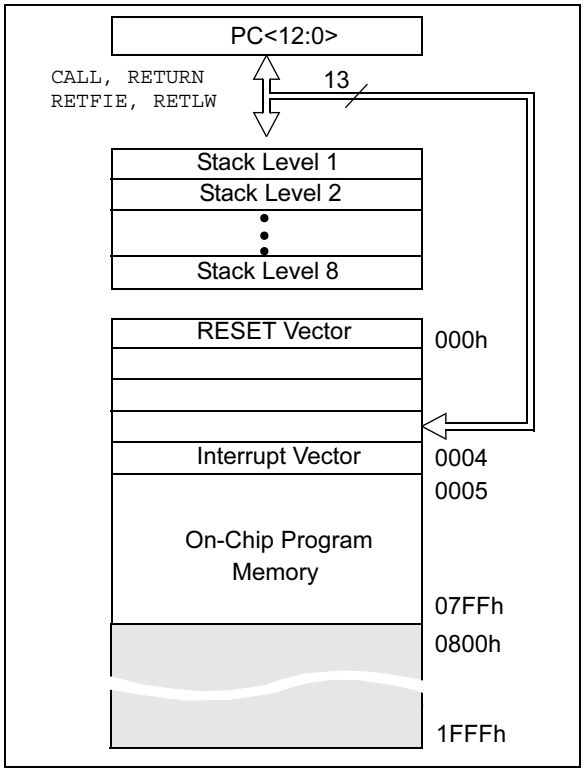


FIGURE 4-3: PROGRAM MEMORY MAP AND STACK FOR THE PIC16C622/PIC16C622A



The code example in Example 7-1 depicts the steps required to configure the comparator module. RA3 and RA4 are configured as digital output. RA0 and RA1 are configured as the V- inputs and RA2 as the V+ input to both comparators.

EXAMPLE 7-1: INITIALIZING COMPARATOR MODULE

```
MOVLW   0x03          ;Init comparator mode
MOVWF   CMCON         ;CM<2:0> = 011
CLRF    PORTA         ;Init PORTA
BSF     STATUS,RP0    ;Select Bank1
MOVLW   0x07          ;Initialize data direction
MOVWF   TRISA         ;Set RA<2:0> as inputs
                      ;RA<4:3> as outputs
                      ;TRISA<7:5> always read '0'
BCF     STATUS,RP0    ;Select Bank 0
CALL    DELAY 10      ;10µs delay
MOVF    CMCON,F       ;Read CMCON to end change condition
BCF     PIR1,CMIF     ;Clear pending interrupts
BSF     STATUS,RP0    ;Select Bank 1
BSF     PIE1,CMIE     ;Enable comparator interrupts
BCF     STATUS,RP0    ;Select Bank 0
BSF     INTCON,PEIE   ;Enable peripheral interrupts
BSF     INTCON,GIE    ;Global interrupt enable
```

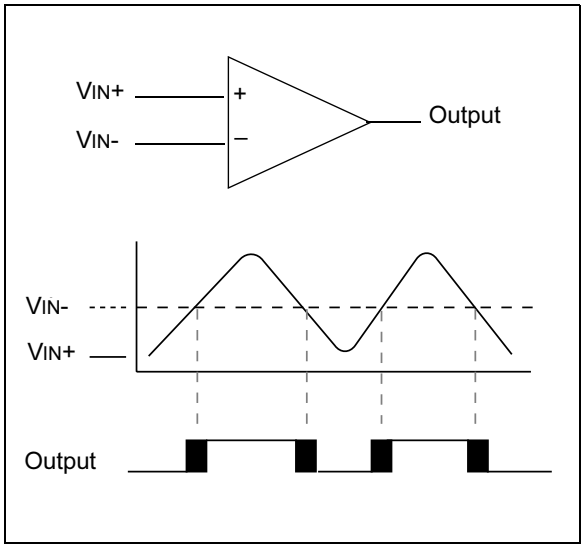
7.2 Comparator Operation

A single comparator is shown in Figure 7-2 along with the relationship between the analog input levels and the digital output. When the analog input at VIN+ is less than the analog input VIN-, the output of the comparator is a digital low level. When the analog input at VIN+ is greater than the analog input VIN-, the output of the comparator is a digital high level. The shaded areas of the output of the comparator in Figure 7-2 represent the uncertainty due to input offsets and response time.

7.3 Comparator Reference

An external or internal reference signal may be used depending on the comparator Operating mode. The analog signal that is present at VIN- is compared to the signal at VIN+, and the digital output of the comparator is adjusted accordingly (Figure 7-2).

FIGURE 7-2: SINGLE COMPARATOR



7.3.1 EXTERNAL REFERENCE SIGNAL

When external voltage references are used, the comparator module can be configured to have the comparators operate from the same or different reference sources. However, threshold detector applications may require the same reference. The reference signal must be between VSS and VDD, and can be applied to either pin of the comparator(s).

7.3.2 INTERNAL REFERENCE SIGNAL

The comparator module also allows the selection of an internally generated voltage reference for the comparators. Section 10, Instruction Sets, contains a detailed description of the Voltage Reference Module that provides this signal. The internal reference signal is used when the comparators are in mode CM<2:0>=010 (Figure 7-1). In this mode, the internal voltage reference is applied to the VIN+ pin of both comparators.

8.0 VOLTAGE REFERENCE MODULE

The Voltage Reference is a 16-tap resistor ladder network that provides a selectable voltage reference. The resistor ladder is segmented to provide two ranges of VREF values and has a power-down function to conserve power when the reference is not being used. The VRCON register controls the operation of the reference as shown in Register 8-1. The block diagram is given in Figure 8-1.

8.1 Configuring the Voltage Reference

The Voltage Reference can output 16 distinct voltage levels for each range. The equations used to calculate the output of the Voltage Reference are as follows:

if VRR = 1: VREF = (VR<3:0>/24) x VDD

if VRR = 0: VREF = (VDD x 1/4) + (VR<3:0>/32) x VDD

The setting time of the Voltage Reference must be considered when changing the VREF output (Table 12-1). Example 8-1 shows an example of how to configure the Voltage Reference for an output voltage of 1.25V with VDD = 5.0V.

REGISTER 8-1: VRCON REGISTER(ADDRESS 9Fh)

R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
VREN	VROE	VRR	—	VR3	VR2	VR1	VR0
bit 7							bit 0

bit 7 **VREN:** VREF Enable
1 = VREF circuit powered on
0 = VREF circuit powered down, no IDD drain

bit 6 **VROE:** VREF Output Enable
1 = VREF is output on RA2 pin
0 = VREF is disconnected from RA2 pin

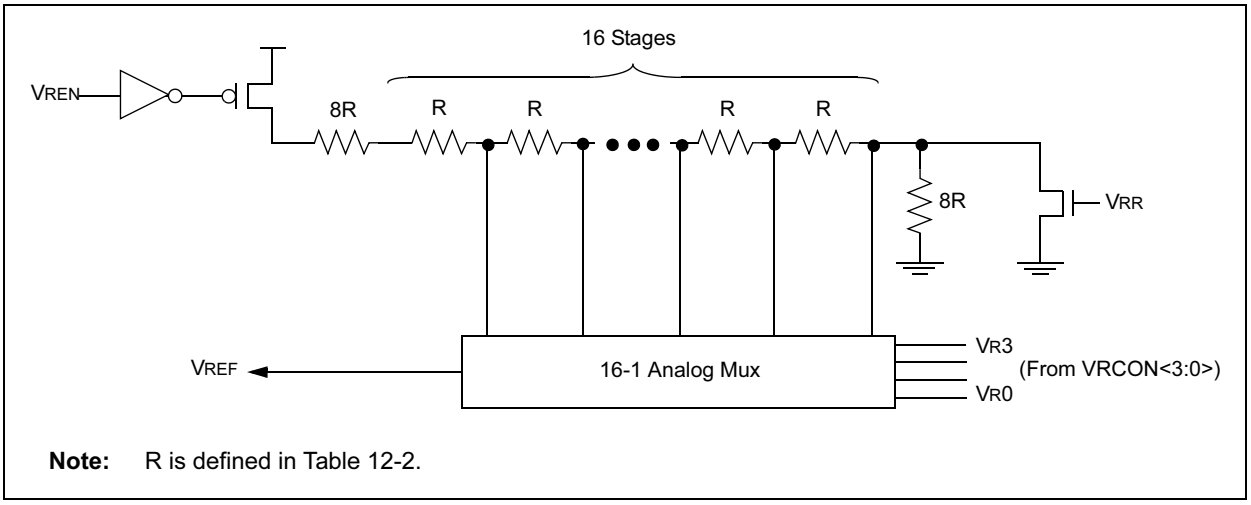
bit 5 **VRR:** VREF Range selection
1 = Low Range
0 = High Range

bit 4 **Unimplemented:** Read as '0'

bit 3-0 **VR<3:0>**: VREF value selection 0 ≤ VR [3:0] ≤ 15
when VRR = 1: VREF = (VR<3:0>/ 24) * VDD
when VRR = 0: VREF = 1/4 * VDD + (VR<3:0>/ 32) * VDD

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

FIGURE 8-1: VOLTAGE REFERENCE BLOCK DIAGRAM



Note: R is defined in Table 12-2.

9.0 SPECIAL FEATURES OF THE CPU

Special circuits to deal with the needs of real-time applications are what sets a microcontroller apart from other processors. The PIC16C62X family has a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection.

These are:

1. OSC selection
2. RESET
   Power-on Reset (POR)
   Power-up Timer (PWRT)
   Oscillator Start-up Timer (OST)
   Brown-out Reset (BOR)
3. Interrupts
4. Watchdog Timer (WDT)
5. SLEEP
6. Code protection
7. ID Locations
8. In-Circuit Serial Programming™

The PIC16C62X devices have a Watchdog Timer which is controlled by configuration bits. It runs off its own RC oscillator for added reliability. There are two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in RESET until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay of 72 ms (nominal) on power-up only, designed to keep the part in RESET while the power supply stabilizes. There is also circuitry to RESET the device if a brown-out occurs, which provides at least a 72 ms RESET. With these three functions on-chip, most applications need no external RESET circuitry.

The SLEEP mode is designed to offer a very low current Power-down mode. The user can wake-up from SLEEP through external RESET, Watchdog Timer wake-up or through an interrupt. Several oscillator options are also made available to allow the part to fit the application. The RC oscillator option saves system cost, while the LP crystal option saves power. A set of configuration bits are used to select various options.

9.1 Configuration Bits

The configuration bits can be programmed (read as '0') or left unprogrammed (read as '1') to select various device configurations. These bits are mapped in program memory location 2007h.

The user will note that address 2007h is beyond the user program memory space. In fact, it belongs to the special test/configuration memory space (2000h – 3FFFh), which can be accessed only during programming.

REGISTER 9-1: CONFIGURATION WORD (ADDRESS 2007h)

CP1	CP0 (2)	CP1	$\overline{CP0}$ (2)	$\overline{CP1}$	CP0 (2)		BODEN	CP1	CP0 (2)	$\overline{PWRTE}$	WDTE	F0SC1	F0SC0
bit 13													bit 0

bit 13-8, 5-4: **CP<1:0>:** Code protection bit pairs (2)

Code protection for 2K program memory
11 = Program memory code protection off
10 = 0400h-07FFh code protected
01 = 0200h-07FFh code protected
00 = 0000h-07FFh code protected

Code protection for 1K program memory
11 = Program memory code protection off
10 = Program memory code protection off
01 = 0200h-03FFh code protected
00 = 0000h-03FFh code protected

Code protection for 0.5K program memory
11 = Program memory code protection off
10 = Program memory code protection off
01 = Program memory code protection off
00 = 0000h-01FFh code protected

bit 7 **Unimplemented**: Read as '0'

bit 6 **BODEN**: Brown-out Reset Enable bit (1)
1 = BOR enabled
0 = BOR disabled

bit 3 **$\overline{PWRTE}$**: Power-up Timer Enable bit (1, 3)
1 = PWRT disabled
0 = PWRT enabled

bit 2 **WDTE**: Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled

bit 1-0 **FOSC1:FOSC0**: Oscillator Selection bits
11 = RC oscillator
10 = HS oscillator
01 = XT oscillator
00 = LP oscillator

Note 1: Enabling Brown-out Reset automatically enables Power-up Timer (PWRT) regardless of the value of bit $\overline{PWRTE}$. Ensure the Power-up Timer is enabled anytime Brown-out Detect Reset is enabled.
2: All of the CP<1:0> pairs have to be given the same value to enable the code protection scheme listed.
3: Unprogrammed parts default the Power-up Timer disabled.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	1 = bit is set	0 = bit is cleared	x = bit is unknown

9.2.3 EXTERNAL CRYSTAL OSCILLATOR CIRCUIT

Either a prepackaged oscillator can be used or a simple oscillator circuit with TTL gates can be built. Prepackaged oscillators provide a wide operating range and better stability. A well-designed crystal oscillator will provide good performance with TTL gates. Two types of crystal oscillator circuits can be used; one with series resonance or one with parallel resonance.

Figure 9-3 shows implementation of a parallel resonant oscillator circuit. The circuit is designed to use the fundamental frequency of the crystal. The 74AS04 inverter performs the 180° phase shift that a parallel oscillator requires. The 4.7 kΩ resistor provides the negative feedback for stability. The 10 kΩ potentiometers bias the 74AS04 in the linear region. This could be used for external oscillator designs.

FIGURE 9-3: EXTERNAL PARALLEL RESONANT CRYSTAL OSCILLATOR CIRCUIT

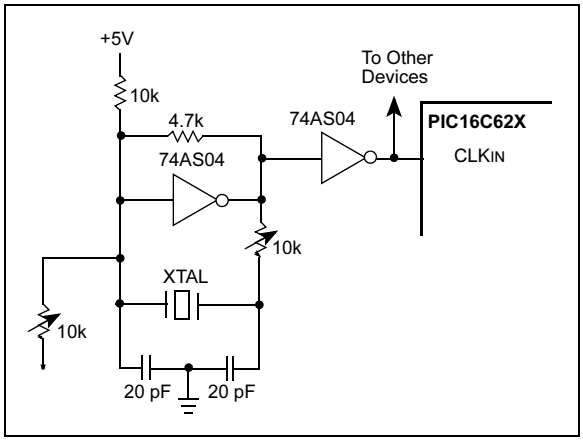
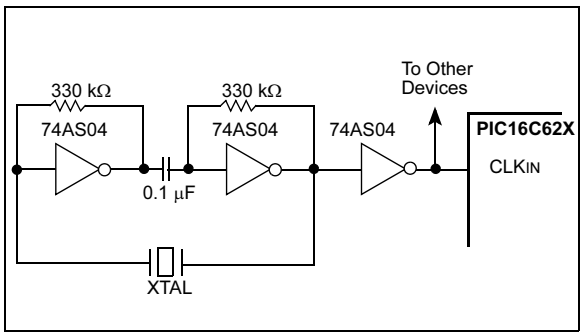


Figure 9-4 shows a series resonant oscillator circuit. This circuit is also designed to use the fundamental frequency of the crystal. The inverter performs a 180° phase shift in a series resonant oscillator circuit. The 330 kΩ resistors provide the negative feedback to bias the inverters in their linear region.

FIGURE 9-4: EXTERNAL SERIES RESONANT CRYSTAL OSCILLATOR CIRCUIT



9.2.4 RC OSCILLATOR

For timing insensitive applications the "RC" device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (REXT) and capacitor (CEXT) values, and the operating temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low CEXT values. The user also needs to take into account variation due to tolerance of external R and C components used. Figure 9-5 shows how the R/C combination is connected to the PIC16C62X. For REXT values below 2.2 kΩ, the oscillator operation may become unstable or stop completely. For very high REXT values (e.g., 1 MΩ), the oscillator becomes sensitive to noise, humidity and leakage. Thus, we recommend to keep REXT between 3 kΩ and 100 kΩ.

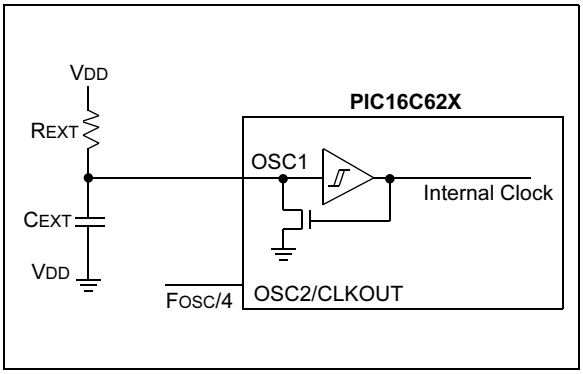
Although the oscillator will operate with no external capacitor (CEXT = 0 pF), we recommend using values above 20 pF for noise and stability reasons. With no or small external capacitance, the oscillation frequency can vary dramatically due to changes in external capacitances, such as PCB trace capacitance or package lead frame capacitance.

See Section 13.0 for RC frequency variation from part to part due to normal process variation. The variation is larger for larger R (since leakage current variation will affect RC frequency more for large R) and for smaller C (since variation of input capacitance will affect RC frequency more).

See Section 13.0 for variation of oscillator frequency due to VDD for given REXT/CEXT values, as well as frequency variation due to operating temperature for given R, C and VDD values.

The oscillator frequency, divided by 4, is available on the OSC2/CLKOUT pin, and can be used for test purposes or to synchronize other logic (Figure 3-2 for waveform).

FIGURE 9-5: RC OSCILLATOR MODE



9.4.5 TIME-OUT SEQUENCE

On power-up the time-out sequence is as follows: First PWRT time-out is invoked after POR has expired. Then OST is activated. The total time-out will vary based on oscillator configuration and PWRTE bit status. For example, in RC mode with PWRTE bit erased (PWRT disabled), there will be no time-out at all. Figure 9-8, Figure 9-9 and Figure 9-10 depict time-out sequences.

Since the time-outs occur from the POR pulse, if MCLR is kept low long enough, the time-outs will expire. Then bringing MCLR high will begin execution immediately (see Figure 9-9). This is useful for testing purposes or to synchronize more than one PIC16C62X device operating in parallel.

Table 9-4 shows the RESET conditions for some special registers, while Table 9-5 shows the RESET conditions for all the registers.

9.4.6 POWER CONTROL (PCON)/ STATUS REGISTER

The power control/STATUS register, PCON (address 8Eh), has two bits.

Bit0 is BOR (Brown-out). BOR is unknown on Power-on Reset. It must then be set by the user and checked on subsequent RESETS to see if BOR = 0, indicating that a brown-out has occurred. The BOR STATUS bit is a don't care and is not necessarily predictable if the brown-out circuit is disabled (by setting BODEN bit = 0 in the Configuration word).

Bit1 is POR (Power-on Reset). It is a '0' on Power-on Reset and unaffected otherwise. The user must write a '1' to this bit following a Power-on Reset. On a subsequent RESET, if POR is '0', it will indicate that a Power-on Reset must have occurred (V_{DD} may have gone too low).

TABLE 9-1: TIME-OUT IN VARIOUS SITUATIONS

Oscillator Configuration	Power-up		Brown-out Reset	Wake-up from SLEEP
	PWRTE = 0	PWRTE = 1		
XT, HS, LP	72 ms + 1024 TOSC	1024 TOSC	72 ms + 1024 TOSC	1024 TOSC
RC	72 ms	—	72 ms	—

TABLE 9-2: STATUS/PCON BITS AND THEIR SIGNIFICANCE

POR	BOR	TO	PD	
0	X	1	1	Power-on Reset
0	X	0	X	Illegal, TO is set on POR
0	X	X	0	Illegal, PD is set on POR
1	0	X	X	Brown-out Reset
1	1	0	u	WDT Reset
1	1	0	0	WDT Wake-up
1	1	u	u	MCLR Reset during normal operation
1	1	1	0	MCLR Reset during SLEEP

Legend: u = unchanged, x = unknown

TABLE 9-3: SUMMARY OF REGISTERS ASSOCIATED WITH BROWN-OUT

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR Reset	Value on all other RESETS(1)
83h	STATUS				TO	PD				0001 1xxx	000q quuu
8Eh	PCON	—	—	—	—	—	—	POR	BOR	---- --0x	---- --uq

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0', q = value depends on condition.

Note 1: Other (non Power-up) Resets include MCLR Reset, Brown-out Reset and Watchdog Timer Reset during normal operation.

MOVF **Move f**

Syntax: [*label*] MOVF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f) → (dest)

Status Affected: Z

Encoding:

00	1000	dfff	ffff

Description: The contents of register f is moved to a destination dependent upon the status of d. If d = 0, destination is W register. If d = 1, the destination is file register f itself. d = 1 is useful to test a file register since status flag Z is affected.

Words: 1

Cycles: 1

Example
```
MOVF    FSR, 0
```
After Instruction
W = value in FSR register
Z = 1

MOVWF **Move W to f**

Syntax: [*label*] MOVWF f

Operands: $0 \le f \le 127$

Operation: (W) → (f)

Status Affected: None

Encoding:

00	0000	1fff	ffff

Description: Move data from W register to register 'f'.

Words: 1

Cycles: 1

Example
```
MOVWF   OPTION
```
Before Instruction
OPTION = 0xFF
W = 0x4F
After Instruction
OPTION = 0x4F
W = 0x4F

NOP **No Operation**

Syntax: [*label*] NOP

Operands: None

Operation: No operation

Status Affected: None

Encoding:

00	0000	0xx0	0000

Description: No operation.

Words: 1

Cycles: 1

Example
```
NOP
```

OPTION **Load Option Register**

Syntax: [*label*] OPTION

Operands: None

Operation: (W) → OPTION

Status Affected: None

Encoding:

00	0000	0110	0010

Description: The contents of the W register are loaded in the OPTION register. This instruction is supported for code compatibility with PIC16C5X products. Since OPTION is a readable/writable register, the user can directly address it.

Words: 1

Cycles: 1

Example

To maintain upward compatibility with future PICmicro® products, do not use this instruction.

SWAPF **Swap Nibbles in f**

Syntax: [*label*] SWAPF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f<3:0>) → (dest<7:4>),
(f<7:4>) → (dest<3:0>)

Status Affected: None

Encoding:

00	1110	dfff	ffff

Description: The upper and lower nibbles of register 'f' are exchanged. If 'd' is 0, the result is placed in W register. If 'd' is 1, the result is placed in register 'f'.

Words: 1

Cycles: 1

Example
```
SWAPF REG, 0
```
Before Instruction
REG1 = 0xA5

After Instruction
REG1 = 0xA5
W = 0x5A

TRIS **Load TRIS Register**

Syntax: [*label*] TRIS f

Operands: $5 \le f \le 7$

Operation: (W) → TRIS register f;

Status Affected: None

Encoding:

00	0000	0110	0fff

Description: The instruction is supported for code compatibility with the PIC16C5X products. Since TRIS registers are readable and writable, the user can directly address them.

Words: 1

Cycles: 1

Example

To maintain upward compatibility with future PICmicro® products, do not use this instruction.

XORLW **Exclusive OR Literal with W**

Syntax: [*label*] XORLW k

Operands: $0 \le k \le 255$

Operation: (W) .XOR. k → (W)

Status Affected: Z

Encoding:

11	1010	kkkk	kkkk

Description: The contents of the W register are XOR'ed with the eight bit literal 'k'. The result is placed in the W register.

Words: 1

Cycles: 1

Example
```
XORLW 0xAF
```
Before Instruction
W = 0xB5

After Instruction
W = 0x1A

XORWF **Exclusive OR W with f**

Syntax: [*label*] XORWF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (W) .XOR. (f) → (dest)

Status Affected: Z

Encoding:

00	0110	dfff	ffff

Description: Exclusive OR the contents of the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example
```
XORWF REG 1
```
Before Instruction
REG = 0xAF
W = 0xB5

After Instruction
REG = 0x1A
W = 0xB5

11.3 MPLAB C17 and MPLAB C18 C Compilers

The MPLAB C17 and MPLAB C18 Code Development Systems are complete ANSI C compilers for Microchip's PIC17CXXX and PIC18CXXX family of microcontrollers. These compilers provide powerful integration capabilities, superior code optimization and ease of use not found with other compilers.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

11.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK object linker combines relocatable objects created by the MPASM assembler and the MPLAB C17 and MPLAB C18 C compilers. It can link relocatable objects from pre-compiled libraries, using directives from a linker script.

The MPLIB object librarian manages the creation and modification of library files of pre-compiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

11.5 MPLAB C30 C Compiler

The MPLAB C30 C compiler is a full-featured, ANSI compliant, optimizing compiler that translates standard ANSI C programs into dsPIC30F assembly language source. The compiler also supports many command-line options and language extensions to take full advantage of the dsPIC30F device hardware capabilities, and afford fine control of the compiler code generator.

MPLAB C30 is distributed with a complete ANSI C standard library. All library functions have been validated and conform to the ANSI C library standard. The library includes functions for string manipulation, dynamic memory allocation, data conversion, time-keeping, and math functions (trigonometric, exponential and hyperbolic). The compiler provides symbolic information for high level source debugging with the MPLAB IDE.

11.6 MPLAB ASM30 Assembler, Linker, and Librarian

MPLAB ASM30 assembler produces relocatable machine code from symbolic assembly language for dsPIC30F devices. MPLAB C30 compiler uses the assembler to produce it's object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire dsPIC30F instruction set
- Support for fixed-point and floating-point data
- Command line interface
- Rich directive set
- Flexible macro language
- MPLAB IDE compatibility

11.7 MPLAB SIM Software Simulator

The MPLAB SIM software simulator allows code development in a PC hosted environment by simulating the PICmicro series microcontrollers on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a file, or user defined key press, to any pin. The execution can be performed in Single-Step, Execute Until Break, or Trace mode.

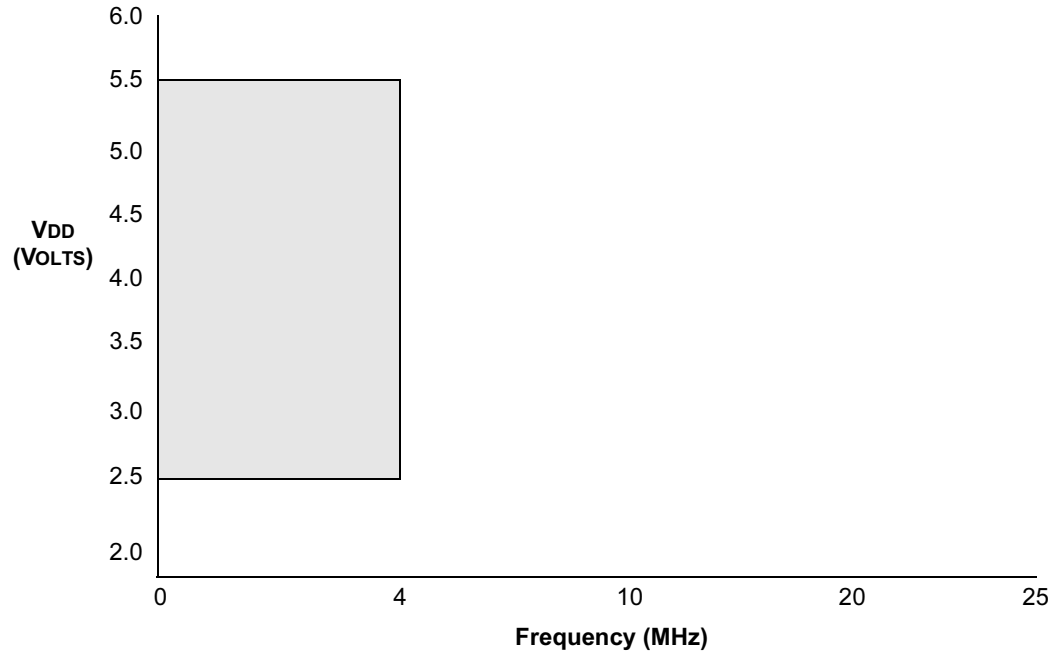
The MPLAB SIM simulator fully supports symbolic debugging using the MPLAB C17 and MPLAB C18 C Compilers, as well as the MPASM assembler. The software simulator offers the flexibility to develop and debug code outside of the laboratory environment, making it an excellent, economical software development tool.

11.8 MPLAB SIM30 Software Simulator

The MPLAB SIM30 software simulator allows code development in a PC hosted environment by simulating the dsPIC30F series microcontrollers on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a file, or user defined key press, to any of the pins.

The MPLAB SIM30 simulator fully supports symbolic debugging using the MPLAB C30 C Compiler and MPLAB ASM30 assembler. The simulator runs in either a Command Line mode for automated tasks, or from MPLAB IDE. This high speed simulator is designed to debug, analyze and optimize time intensive DSP routines.

FIGURE 12-9: PIC16LCR62XA VOLTAGE-FREQUENCY GRAPH, -40°C ≤ TA ≤ +125°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

2: The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.

12.1 DC Characteristics: PIC16C62X-04 (Commercial, Industrial, Extended) PIC16C62X-20 (Commercial, Industrial, Extended) PIC16LC62X-04 (Commercial, Industrial, Extended) (CONT.)

PIC16C62X			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial and -40°C ≤ TA ≤ +125°C for extended				
PIC16LC62X			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial and -40°C ≤ TA ≤ +125°C for extended Operating voltage VDD range is the PIC16C62X range.				
Param. No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D022	ΔIWDT	WDT Current(5)	—	6.0	20	µA	VDD=4.0V
					25	µA	(125°C)
D022A	ΔIBOR	Brown-out Reset Current(5)	—	350	425	µA	BOD enabled, VDD = 5.0V
D023	ΔICOMP	Comparator Current for each Comparator(5)	—	—	100	µA	VDD = 4.0V
D023A	ΔIVREF	VREF Current(5)	—	—	300	µA	VDD = 4.0V
D022	ΔIWDT	WDT Current(5)	—	6.0	15	µA	VDD=3.0V
D022A	ΔIBOR	Brown-out Reset Current(5)	—	350	425	µA	BOD enabled, VDD = 5.0V
D023	ΔICOMP	Comparator Current for each Comparator(5)	—	—	100	µA	VDD = 3.0V
D023A	ΔIVREF	VREF Current(5)	—	—	300	µA	VDD = 3.0V
1A	FOSC	LP Oscillator Operating Frequency	0	—	200	kHz	All temperatures
		RC Oscillator Operating Frequency	0	—	4	MHz	All temperatures
		XT Oscillator Operating Frequency	0	—	4	MHz	All temperatures
		HS Oscillator Operating Frequency	0	—	20	MHz	All temperatures
1A	FOSC	LP Oscillator Operating Frequency	0	—	200	kHz	All temperatures
		RC Oscillator Operating Frequency	0	—	4	MHz	All temperatures
		XT Oscillator Operating Frequency	0	—	4	MHz	All temperatures
		HS Oscillator Operating Frequency	0	—	20	MHz	All temperatures

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in Active Operation mode are:
OSC1 = external square wave, from rail to rail; all I/O pins tri-stated, pulled to VDD,
MCLR = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or VSS.

4: For RC osc configuration, current through REXT is not included. The current through the resistor can be estimated by the formula: Ir = VDD/2REXT (mA) with REXT in kΩ.

5: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

12.3 DC CHARACTERISTICS: PIC16CR62XA-04 (Commercial, Industrial, Extended) PIC16CR62XA-20 (Commercial, Industrial, Extended) PIC16LCR62XA-04 (Commercial, Industrial, Extended)

PIC16CR62XA-04 **PIC16CR62XA-20**			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial and -40°C ≤ TA ≤ +125°C for extended				
PIC16LCR62XA-04			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial and -40°C ≤ TA ≤ +125°C for extended				
Param. No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D001	VDD	Supply Voltage	3.0	—	5.5	V	See Figures 12-7, 12-8, 12-9
D001	VDD	Supply Voltage	2.5	—	5.5	V	See Figures 12-7, 12-8, 12-9
D002	VDR	RAM Data Retention Voltage(1)	—	1.5*	—	V	Device in SLEEP mode
D002	VDR	RAM Data Retention Voltage(1)	—	1.5*	—	V	Device in SLEEP mode
D003	VPOR	VDD start voltage to ensure Power-on Reset	—	VSS	—	V	See section on Power-on Reset for details
D003	VPOR	VDD start voltage to ensure Power-on Reset	—	VSS	—	V	See section on Power-on Reset for details
D004	SVDD	VDD rise rate to ensure Power-on Reset	0.05*	—	—	V/ms	See section on Power-on Reset for details
D004	SVDD	VDD rise rate to ensure Power-on Reset	0.05*	—	—	V/ms	See section on Power-on Reset for details
D005	VBOR	Brown-out Detect Voltage	3.7	4.0	4.35	V	BOREN configuration bit is cleared
D005	VBOR	Brown-out Detect Voltage	3.7	4.0	4.35	V	BOREN configuration bit is cleared
D010	IDD	Supply Current(2)	—	1.2	1.7	mA	FOSC = 4 MHz, VDD = 5.5V, WDT disabled, XT mode, (**Note 4**)*
			—	500	900	μA	FOSC = 4 MHz, VDD = 3.0V, WDT disabled, XT mode, (**Note 4**)
			—	1.0	2.0	mA	FOSC = 10 MHz, VDD = 3.0V, WDT disabled, HS mode, (**Note 6**)
			—	4.0	7.0	mA	FOSC = 20 MHz, VDD = 5.5V, WDT disabled*, HS
			—	3.0	6.0	mA	mode
			—	35	70	μA	FOSC = 20 MHz, VDD = 4.5V, WDT disabled, HS mode FOSC = 32 kHz, VDD = 3.0V, WDT disabled, LP mode
D010	IDD	Supply Current(2)	—	1.2	1.7	mA	FOSC = 4.0 MHz, VDD = 5.5V, WDT disabled, XT mode, (**Note 4**)*
			—	400	800	μA	FOSC = 4.0 MHz, VDD = 2.5V, WDT disabled, XT mode (**Note 4**)
			—	35	70	μA	FOSC = 32 kHz, VDD = 2.5V, WDT disabled, LP mode

12.4 DC Characteristics: PIC16C62X/C62XA/CR62XA (Commercial, Industrial, Extended) PIC16LC62X/LC62XA/LCR62XA (Commercial, Industrial, Extended)

PIC16C62X/C62XA/CR62XA	Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial and -40°C ≤ TA ≤ +125°C for extended
PIC16LC62X/LC62XA/LCR62XA	Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial and -40°C ≤ TA ≤ +125°C for extended

Param. No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	VIL	**Input Low Voltage**					
		I/O ports					
D030		with TTL buffer	VSS	—	0.8V 0.15 VDD	V	VDD = 4.5V to 5.5V otherwise
D031		with Schmitt Trigger input	VSS	—	0.2 VDD	V	
D032		$\overline{MCLR}$, RA4/T0CKI,OSC1 (in RC mode)	Vss	—	0.2 VDD	V	**(Note 1)**
D033		OSC1 (in XT and HS)	Vss	—	0.3 VDD	V	
		OSC1 (in LP)	Vss	—	0.6 VDD-1.0	V	
	VIL	**Input Low Voltage**					
		I/O ports					
D030		with TTL buffer	VSS	—	0.8V 0.15 VDD	V	VDD = 4.5V to 5.5V otherwise
D031		with Schmitt Trigger input	VSS	—	0.2 VDD	V	
D032		$\overline{MCLR}$, RA4/T0CKI,OSC1 (in RC mode)	Vss	—	0.2 VDD	V	**(Note 1)**
D033		OSC1 (in XT and HS)	Vss	—	0.3 VDD	V	
		OSC1 (in LP)	Vss	—	0.6 VDD-1.0	V	
	VIH	Input High Voltage					
		I/O ports					
D040		with TTL buffer	2.0V 0.25 VDD + 0.8V	—	VDD VDD	V	VDD = 4.5V to 5.5V otherwise
D041		with Schmitt Trigger input	0.8 VDD	—	VDD		
D042		$\overline{MCLR}$ RA4/T0CKI	0.8 VDD	—	VDD	V	
D043 D043A		OSC1 (XT, HS and LP) OSC1 (in RC mode)	0.7 VDD 0.9 VDD	—	VDD	V	**(Note 1)**

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1 pin is a Schmitt Trigger input. It is not recommended that the PIC16C62X(A) be driven with external clock in RC mode.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

12.6 DC Characteristics: PIC16C620A/C621A/C622A-40(3) (Commercial) PIC16CR620A-40(3) (Commercial)

DC CHARACTERISTICS Power Supply Pins			Standard Operating Conditions (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for commercial			
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Supply Voltage	VDD	4.5	—	5.5	V	HS Option from 20 - 40 MHz
Supply Current(2)	IDD	— —	5.5 7.7	11.5 16	mA mA	FOSC = 40 MHz, VDD = 4.5V, HS mode FOSC = 40 MHz, VDD = 5.5V, HS mode
HS Oscillator Operating Frequency	FOSC	20	—	40	MHz	OSC1 pin is externally driven, OSC2 pin not connected
Input Low Voltage OSC1	VIL	VSS	—	0.2VDD	V	HS mode, OSC1 externally driven
Input High Voltage OSC1	VIH	0.8VDD	—	VDD	V	HS mode, OSC1 externally driven

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in Active Operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VSS,
T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT disabled, HS mode with OSC2 not connected.

3: For device operation between DC and 20 MHz. See Table 12-1 and Table 12-2.

12.7 AC Characteristics: PIC16C620A/C621A/C622A-40(2) (Commercial) PIC16CR620A-40(2) (Commercial)

AC CHARACTERISTICS All Pins Except Power Supply Pins			Standard Operating Conditions (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for commercial			
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
External CLKIN Frequency	FOSC	20	—	40	MHz	HS mode, OSC1 externally driven
External CLKIN Period	TOSC	25	—	50	ns	HS mode (40), OSC1 externally driven
Clock in (OSC1) Low or High Time	TOSL, TOSH	6	—	—	ns	HS mode, OSC1 externally driven
Clock in (OSC1) Rise or Fall Time	TOSR, TOSF	—	—	6.5	ns	HS mode, OSC1 externally driven
OSC1↑ (Q1 cycle) to Port out valid	TOSH2IOV	—	—	100	ns	—
OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TOSH2IOI	50	—	—	ns	—

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: For device operation between DC and 20 MHz. See Table 12-1 and Table 12-2.

TABLE 12-1: COMPARATOR SPECIFICATIONS

Operating Conditions: V_{DD} range as described in Table 12-1, -40°C<T_A<+125°C. Current consumption is specified in Table 12-1.

Characteristics	Sym	Min	Typ	Max	Units	Comments
Input offset voltage			± 5.0	± 10	mV	
Input common mode voltage		0		V_{DD} - 1.5	V	
CMRR		+55*			δβ	
Response Time(1)			150*	400* 600*	ns ns	PIC16C62X(A) PIC16LC62X
Comparator mode change to output valid				10*	μs	

* These parameters are characterized but not tested.

Note 1: Response time measured with one comparator input at (V_{DD} - 1.5)/2, while the other input transitions from V_{SS} to V_{DD}.

TABLE 12-2: VOLTAGE REFERENCE SPECIFICATIONS

Operating Conditions:V_{DD} range as described in Table 12-1, -40°C<T_A<+125°C. Current consumption is specified in Table 12-1.

Characteristics	Sym	Min	Typ	Max	Units	Comments
Resolution			V_{DD}/24 V_{DD}/32		LSB LSB	Low Range (V_{RR}=1) High Range (V_{RR}=0)
Absolute Accuracy				±1/4 ±1/2	LSB LSB	Low Range (V_{RR}=1) High Range (V_{RR}=0)
Unit Resistor Value (R)			2K*		Ω	Figure 8-1
Settling Time(1)				10*	μs	

* These parameters are characterized but not tested.

Note 1: Settling time measured while V_{RR} = 1 and V_R<3:0> transitions from 0000 to 1111.

12.8 Timing Parameter Symbology

The timing parameter symbols have been created with one of the following formats:

1. TppS2ppS
2. TppS

T			
F	Frequency	T	Time

Lowercase subscripts (pp) and their meanings:

pp			
ck	CLKOUT	osc	OSC1
io	I/O port	t0	T0CKI
mc	$\overline{\text{MCLR}}$		

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-Impedance

FIGURE 12-11: LOAD CONDITIONS