



Welcome to [E-XFL.COM](https://www.e-xfl.com)

### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	13
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	80 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	18-SOIC
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic16lc621-04e-so">https://www.e-xfl.com/product-detail/microchip-technology/pic16lc621-04e-so</a>

# PIC16C62X

**TABLE 1-1: PIC16C62X FAMILY OF DEVICES**

		PIC16C620 <sup>(3)</sup>	PIC16C620A <sup>(1)(4)</sup>	PIC16CR620A <sup>(2)</sup>	PIC16C621 <sup>(3)</sup>	PIC16C621A <sup>(1)(4)</sup>	PIC16C622 <sup>(3)</sup>	PIC16C622A <sup>(1)(4)</sup>
Clock	Maximum Frequency of Operation (MHz)	20	40	20	20	40	20	40
Memory	EPROM Program Memory (x14 words)	512	512	512	1K	1K	2K	2K
	Data Memory (bytes)	80	96	96	80	96	128	128
Peripherals	Timer Module(s)	TMR0	TMR0	TMRO	TMR0	TMR0	TMR0	TMR0
	Comparators(s)	2	2	2	2	2	2	2
	Internal Reference Voltage	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Features	Interrupt Sources	4	4	4	4	4	4	4
	I/O Pins	13	13	13	13	13	13	13
	Voltage Range (Volts)	2.5-6.0	2.7-5.5	2.5-5.5	2.5-6.0	2.7-5.5	2.5-6.0	2.7-5.5
	Brown-out Reset	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	Packages	18-pin DIP, SOIC, 20-pin SSOP	18-pin DIP, SOIC, 20-pin SSOP	18-pin DIP, SOIC, 20-pin SSOP	18-pin DIP, SOIC, 20-pin SSOP	18-pin DIP, SOIC, 20-pin SSOP	18-pin DIP, SOIC, 20-pin SSOP	18-pin DIP, SOIC, 20-pin SSOP

All PICmicro<sup>®</sup> Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability. All PIC16C62X Family devices use serial programming with clock pin RB6 and data pin RB7.

- Note 1:** If you change from this device to another device, please verify oscillator characteristics in your application.
- 2:** For ROM parts, operation from 2.0V - 2.5V will require the PIC16LCR62XA parts.
- 3:** For OTP parts, operation from 2.5V - 3.0V will require the PIC16LC62X part.
- 4:** For OTP parts, operation from 2.7V - 3.0V will require the PIC16LC62XA part.

# PIC16C62X

### 3.1 Clocking Scheme/Instruction Cycle

The clock input (OSC1/CLKIN pin) is internally divided by four to generate four non-overlapping quadrature clocks namely Q1, Q2, Q3 and Q4. Internally, the program counter (PC) is incremented every Q1, the instruction is fetched from the program memory and latched into the instruction register in Q4. The instruction is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow is shown in Figure 3-2.

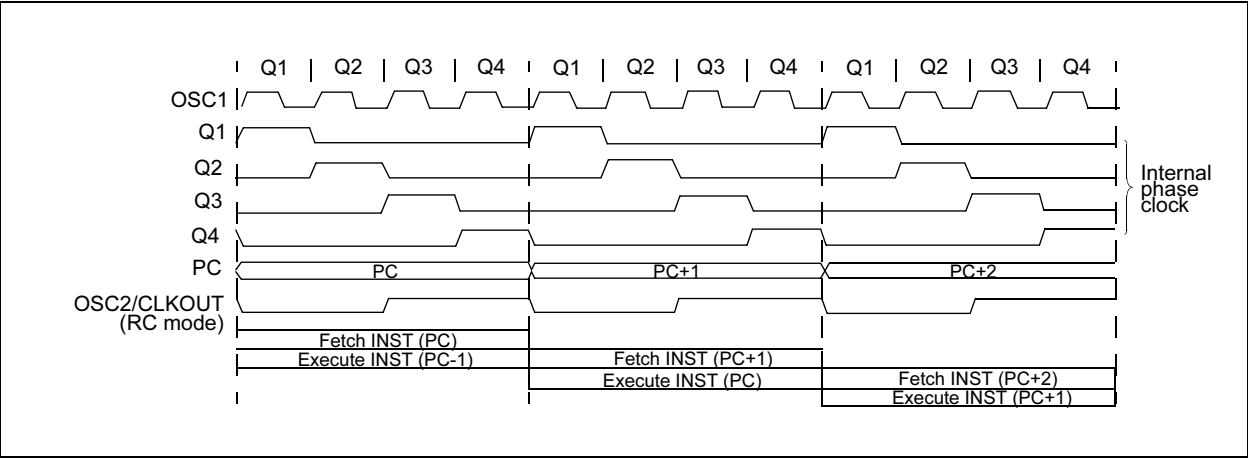
### 3.2 Instruction Flow/Pipelining

An "Instruction Cycle" consists of four Q cycles (Q1, Q2, Q3 and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle while decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g., GOTO) then two cycles are required to complete the instruction (Example 3-1).

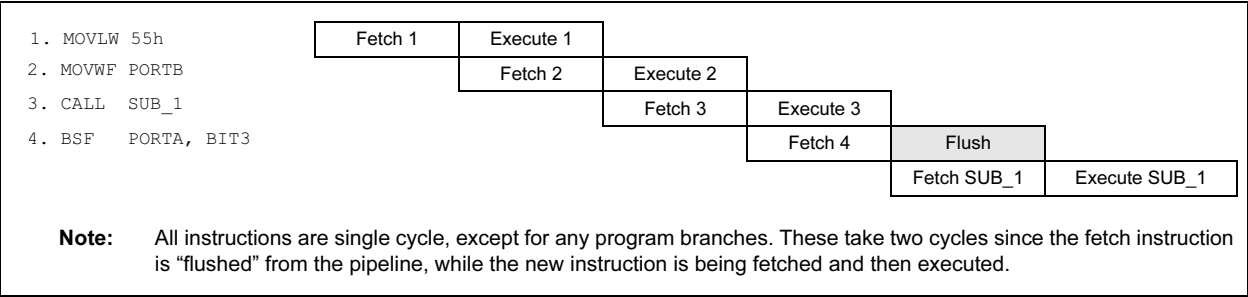
A fetch cycle begins with the program counter (PC) incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the "Instruction Register (IR)" in cycle Q1. This instruction is then decoded and executed during the Q2, Q3 and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

FIGURE 3-2: CLOCK/INSTRUCTION CYCLE



EXAMPLE 3-1: INSTRUCTION PIPELINE FLOW



# PIC16C62X

---

## 4.2 Data Memory Organization

The data memory (Figure 4-4, Figure 4-5, Figure 4-6 and Figure 4-7) is partitioned into two banks, which contain the General Purpose Registers and the Special Function Registers. Bank 0 is selected when the RP0 bit is cleared. Bank 1 is selected when the RP0 bit (STATUS <5>) is set. The Special Function Registers are located in the first 32 locations of each bank. Register locations 20-7Fh (Bank0) on the PIC16C620A/CR620A/621A and 20-7Fh (Bank0) and A0-BFh (Bank1) on the PIC16C622 and PIC16C622A are General Purpose Registers implemented as static RAM. Some Special Purpose Registers are mapped in Bank 1.

Addresses F0h-FFh of bank1 are implemented as common ram and mapped back to addresses 70h-7Fh in bank0 on the PIC16C620A/621A/622A/CR620A.

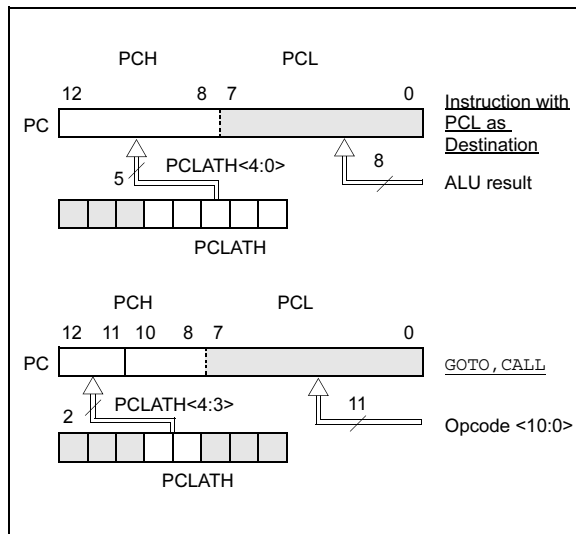
### 4.2.1 GENERAL PURPOSE REGISTER FILE

The register file is organized as 80 x 8 in the PIC16C620/621, 96 x 8 in the PIC16C620A/621A/CR620A and 128 x 8 in the PIC16C622(A). Each is accessed either directly or indirectly through the File Select Register FSR (Section 4.4).

## 4.3 PCL and PCLATH

The program counter (PC) is 13-bits wide. The low byte comes from the PCL register, which is a readable and writable register. The high byte (PC<12:8>) is not directly readable or writable and comes from PCLATH. On any RESET, the PC is cleared. Figure 4-8 shows the two situations for the loading of the PC. The upper example in the figure shows how the PC is loaded on a write to PCL (PCLATH<4:0> → PCH). The lower example in the figure shows how the PC is loaded during a CALL or GOTO instruction (PCLATH<4:3> → PCH).

**FIGURE 4-8: LOADING OF PC IN DIFFERENT SITUATIONS**



### 4.3.1 COMPUTED GOTO

A computed GOTO is accomplished by adding an offset to the program counter (ADDWF PCL). When doing a table read using a computed GOTO method, care should be exercised if the table location crosses a PCL memory boundary (each 256 byte block). Refer to the application note, "Implementing a Table Read" (AN556).

### 4.3.2 STACK

The PIC16C62X family has an 8-level deep x 13-bit wide hardware stack (Figure 4-2 and Figure 4-3). The stack space is not part of either program or data space and the stack pointer is not readable or writable. The PC is PUSHed onto the stack when a CALL instruction is executed or an interrupt causes a branch. The stack is POPed in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not affected by a PUSH or POP operation.

The stack operates as a circular buffer. This means that after the stack has been PUSHed eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on).

**Note 1:** There are no STATUS bits to indicate stack overflow or stack underflow conditions.

**2:** There are no instructions/mnemonics called PUSH or POP. These are actions that occur from the execution of the CALL, RETURN, RETLW and RETFIE instructions, or the vectoring to an interrupt address.

The code example in Example 7-1 depicts the steps required to configure the comparator module. RA3 and RA4 are configured as digital output. RA0 and RA1 are configured as the V- inputs and RA2 as the V+ input to both comparators.

## EXAMPLE 7-1: INITIALIZING COMPARATOR MODULE

```

MOVLW 0x03      ;Init comparator mode
MOVWF CMCON      ;CM<2:0> = 011
CLRF PORTA       ;Init PORTA
BSF STATUS,RP0   ;Select Bank1
MOVLW 0x07      ;Initialize data direction
MOVWF TRISA      ;Set RA<2:0> as inputs
                  ;RA<4:3> as outputs
                  ;TRISA<7:5> always read '0'

BCF STATUS,RP0   ;Select Bank 0
CALL DELAY 10    ;10µs delay
MOVF CMCON,F     ;Read CMCON to end change condition
BCF PIR1,CMIF    ;Clear pending interrupts
BSF STATUS,RP0   ;Select Bank 1
BSF PIE1,CMIE    ;Enable comparator interrupts
BCF STATUS,RP0   ;Select Bank 0
BSF INTCON,PEIE  ;Enable peripheral interrupts
BSF INTCON,GIE   ;Global interrupt enable
    
```

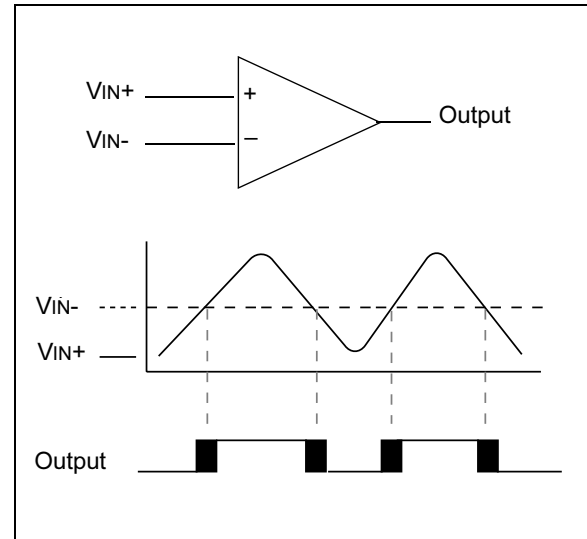
## 7.2 Comparator Operation

A single comparator is shown in Figure 7-2 along with the relationship between the analog input levels and the digital output. When the analog input at VIN+ is less than the analog input VIN-, the output of the comparator is a digital low level. When the analog input at VIN+ is greater than the analog input VIN-, the output of the comparator is a digital high level. The shaded areas of the output of the comparator in Figure 7-2 represent the uncertainty due to input offsets and response time.

## 7.3 Comparator Reference

An external or internal reference signal may be used depending on the comparator Operating mode. The analog signal that is present at VIN- is compared to the signal at VIN+, and the digital output of the comparator is adjusted accordingly (Figure 7-2).

FIGURE 7-2: SINGLE COMPARATOR



### 7.3.1 EXTERNAL REFERENCE SIGNAL

When external voltage references are used, the comparator module can be configured to have the comparators operate from the same or different reference sources. However, threshold detector applications may require the same reference. The reference signal must be between VSS and VDD, and can be applied to either pin of the comparator(s).

### 7.3.2 INTERNAL REFERENCE SIGNAL

The comparator module also allows the selection of an internally generated voltage reference for the comparators. Section 10, Instruction Sets, contains a detailed description of the Voltage Reference Module that provides this signal. The internal reference signal is used when the comparators are in mode CM<2:0>=010 (Figure 7-1). In this mode, the internal voltage reference is applied to the VIN+ pin of both comparators.

## 9.0 SPECIAL FEATURES OF THE CPU

Special circuits to deal with the needs of real-time applications are what sets a microcontroller apart from other processors. The PIC16C62X family has a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection.

These are:

1. OSC selection
2. RESET
  - Power-on Reset (POR)
  - Power-up Timer (PWRT)
  - Oscillator Start-up Timer (OST)
  - Brown-out Reset (BOR)
3. Interrupts
4. Watchdog Timer (WDT)
5. SLEEP
6. Code protection
7. ID Locations
8. In-Circuit Serial Programming™

The PIC16C62X devices have a Watchdog Timer which is controlled by configuration bits. It runs off its own RC oscillator for added reliability. There are two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in RESET until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay of 72 ms (nominal) on power-up only, designed to keep the part in RESET while the power supply stabilizes. There is also circuitry to RESET the device if a brown-out occurs, which provides at least a 72 ms RESET. With these three functions on-chip, most applications need no external RESET circuitry.

The SLEEP mode is designed to offer a very low current Power-down mode. The user can wake-up from SLEEP through external RESET, Watchdog Timer wake-up or through an interrupt. Several oscillator options are also made available to allow the part to fit the application. The RC oscillator option saves system cost, while the LP crystal option saves power. A set of configuration bits are used to select various options.

## 9.4.5 TIME-OUT SEQUENCE

On power-up the time-out sequence is as follows: First PWRT time-out is invoked after POR has expired. Then OST is activated. The total time-out will vary based on oscillator configuration and  $\overline{\text{PWRTE}}$  bit status. For example, in RC mode with  $\overline{\text{PWRTE}}$  bit erased ( $\overline{\text{PWRT}}$  disabled), there will be no time-out at all. Figure 9-8, Figure 9-9 and Figure 9-10 depict time-out sequences.

Since the time-outs occur from the POR pulse, if  $\overline{\text{MCLR}}$  is kept low long enough, the time-outs will expire. Then bringing  $\overline{\text{MCLR}}$  high will begin execution immediately (see Figure 9-9). This is useful for testing purposes or to synchronize more than one PIC16C62X device operating in parallel.

Table 9-4 shows the RESET conditions for some special registers, while Table 9-5 shows the RESET conditions for all the registers.

## 9.4.6 POWER CONTROL (PCON)/ STATUS REGISTER

The power control/STATUS register, PCON (address 8Eh), has two bits.

Bit0 is  $\overline{\text{BOR}}$  (Brown-out).  $\overline{\text{BOR}}$  is unknown on Power-on Reset. It must then be set by the user and checked on subsequent RESETS to see if  $\overline{\text{BOR}} = 0$ , indicating that a brown-out has occurred. The  $\overline{\text{BOR}}$  STATUS bit is a don't care and is not necessarily predictable if the brown-out circuit is disabled (by setting BODEN bit = 0 in the Configuration word).

Bit1 is  $\overline{\text{POR}}$  (Power-on Reset). It is a '0' on Power-on Reset and unaffected otherwise. The user must write a '1' to this bit following a Power-on Reset. On a subsequent RESET, if  $\overline{\text{POR}}$  is '0', it will indicate that a Power-on Reset must have occurred ( $\text{VDD}$  may have gone too low).

**TABLE 9-1: TIME-OUT IN VARIOUS SITUATIONS**

Oscillator Configuration	Power-up		Brown-out Reset	Wake-up from SLEEP
	$\overline{\text{PWRTE}} = 0$	$\overline{\text{PWRTE}} = 1$		
XT, HS, LP	72 ms + 1024 T <sub>osc</sub>	1024 T <sub>osc</sub>	72 ms + 1024 T <sub>osc</sub>	1024 T <sub>osc</sub>
RC	72 ms	—	72 ms	—

**TABLE 9-2: STATUS/PCON BITS AND THEIR SIGNIFICANCE**

POR	BOR	TO	PD	
0	X	1	1	Power-on Reset
0	X	0	X	Illegal, $\overline{\text{TO}}$ is set on $\overline{\text{POR}}$
0	X	X	0	Illegal, $\overline{\text{PD}}$ is set on $\overline{\text{POR}}$
1	0	X	X	Brown-out Reset
1	1	0	u	WDT Reset
1	1	0	0	WDT Wake-up
1	1	u	u	$\overline{\text{MCLR}}$ Reset during normal operation
1	1	1	0	$\overline{\text{MCLR}}$ Reset during SLEEP

Legend: u = unchanged, x = unknown

**TABLE 9-3: SUMMARY OF REGISTERS ASSOCIATED WITH BROWN-OUT**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR Reset	Value on all other RESETS <sup>(1)</sup>
83h	STATUS				$\overline{\text{TO}}$	$\overline{\text{PD}}$				0001 1xxx	000q quuu
8Eh	PCON	—	—	—	—	—	—	$\overline{\text{POR}}$	$\overline{\text{BOR}}$	---- --0x	---- --uq

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0', q = value depends on condition.

**Note 1:** Other (non Power-up) Resets include  $\overline{\text{MCLR}}$  Reset, Brown-out Reset and Watchdog Timer Reset during normal operation.



# PIC16C62X

BCF		Bit Clear f						
Syntax:	[ <i>label</i> ] BCF    f,b							
Operands:	$0 \leq f \leq 127$ $0 \leq b \leq 7$							
Operation:	$0 \rightarrow (f<b>)$							
Status Affected:	None							
Encoding:	<table border="1"><tr><td>01</td><td>00bb</td><td>bfff</td><td>ffff</td></tr></table>				01	00bb	bfff	ffff
01	00bb	bfff	ffff					
Description:	Bit 'b' in register 'f' is cleared.							
Words:	1							
Cycles:	1							
Example	<div>BCF            FLAG_REG, 7</div> <div>Before Instruction</div> <div>FLAG_REG = 0xC7</div> <div>After Instruction</div> <div>FLAG_REG = 0x47</div>							

BSF		Bit Set f			
Syntax:	[ <i>label</i> ] BSF f,b				
Operands:	$0 \leq f \leq 127$ $0 \leq b \leq 7$				
Operation:	$1 \rightarrow (f<b>)$				
Status Affected:	None				
Encoding:	01	01bb	bfff	ffff	
Description:	Bit 'b' in register 'f' is set.				
Words:	1				
Cycles:	1				
Example	BSF FLAG_REG, 7				
	Before Instruction				
	FLAG_REG = 0x0A				
	After Instruction				
	FLAG_REG = 0x8A				

BTFSC		Bit Test, Skip if Clear			
Syntax:	[ <i>label</i> ] BTFSC f,b				
Operands:	$0 \leq f \leq 127$ $0 \leq b \leq 7$				
Operation:	skip if (f<b>) = 0				
Status Affected:	None				
Encoding:	01	10bb	bfff	ffff	
Description:	If bit 'b' in register 'f' is '0', then the next instruction is skipped. If bit 'b' is '0', then the next instruction fetched during the current instruction execution is discarded, and a NOP is executed instead, making this a two-cycle instruction.				
Words:	1				
Cycles:	1(2)				
Example	HERE FALSE TRUE	BTFSC GOTO • • •	FLAG,1 PROCESS_CO DE		

Before Instruction  
PC = address HERE

After Instruction  
if FLAG<1> = 0,  
PC = address TRUE  
if FLAG<1> = 1,  
PC = address FALSE

# PIC16C62X

## CLRW Clear W

Syntax: [ *label* ] CLRW

Operands: None

Operation: 00h → (W)  
1 → Z

Status Affected: Z

Encoding: 

00	0001	0000	0011
----	------	------	------

Description: W register is cleared. Zero bit (Z) is set.

Words: 1

Cycles: 1

Example CLRW

Before Instruction  
W = 0x5A  
After Instruction  
W = 0x00  
Z = 1

## CLRWDT Clear Watchdog Timer

Syntax: [ *label* ] CLRWDT

Operands: None

Operation: 00h → WDT  
0 → WDT prescaler,  
1 →  $\overline{TO}$   
1 →  $\overline{PD}$

Status Affected:  $\overline{TO}$ ,  $\overline{PD}$

Encoding: 

00	0000	0110	0100
----	------	------	------

Description: CLRWDT instruction resets the Watchdog Timer. It also resets the prescaler of the WDT. STATUS bits  $\overline{TO}$  and  $\overline{PD}$  are set.

Words: 1

Cycles: 1

Example CLRWDT

Before Instruction  
WDT counter = ?  
After Instruction  
WDT counter = 0x00  
WDT prescaler = 0  
 $\overline{TO}$  = 1  
 $\overline{PD}$  = 1

## COMF Complement f

Syntax: [ *label* ] COMF f,d

Operands:  $0 \leq f \leq 127$   
 $d \in [0,1]$

Operation:  $(\bar{f}) \rightarrow (\text{dest})$

Status Affected: Z

Encoding: 

00	1001	dfff	ffff
----	------	------	------

Description: The contents of register 'f' are complemented. If 'd' is 0, the result is stored in W. If 'd' is 1, the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example COMF REG1,0

Before Instruction  
REG1 = 0x13  
After Instruction  
REG1 = 0x13  
W = 0xEC

## DECF Decrement f

Syntax: [ *label* ] DECF f,d

Operands:  $0 \leq f \leq 127$   
 $d \in [0,1]$

Operation:  $(f) - 1 \rightarrow (\text{dest})$

Status Affected: Z

Encoding: 

00	0011	dfff	ffff
----	------	------	------

Description: Decrement register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example DECF CNT, 1

Before Instruction  
CNT = 0x01  
Z = 0  
After Instruction  
CNT = 0x00  
Z = 1

## DECFSZ      Decrement f, Skip if 0

**Syntax:**      `[label] DECFSZ f,d`

**Operands:**       $0 \leq f \leq 127$   
 $d \in [0,1]$

**Operation:**       $(f) - 1 \rightarrow (\text{dest}); \quad \text{skip if result} = 0$

**Status Affected:**      None

**Encoding:**

00	1011	dfff	ffff
----	------	------	------

**Description:**      The contents of register 'f' are decremented. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'.  
 If the result is 0, the next instruction, which is already fetched, is discarded. A NOP is executed instead making it a two-cycle instruction.

**Words:**      1

**Cycles:**      1(2)

**Example**

```

    HERE      DECFSZ  CNT, 1
              GOTO    LOOP
    CONTINUE  •
              •
              •
    
```

**Before Instruction**  
 PC = address HERE

**After Instruction**  
 CNT = CNT - 1  
 if CNT = 0,  
 PC = address CONTINUE  
 if CNT  $\neq$  0,  
 PC = address HERE+1

## GOTO      Unconditional Branch

**Syntax:**      `[label] GOTO k`

**Operands:**       $0 \leq k \leq 2047$

**Operation:**       $k \rightarrow \text{PC}<10:0>$   
 $\text{PCLATH}<4:3> \rightarrow \text{PC}<12:11>$

**Status Affected:**      None

**Encoding:**

10	1kkk	kkkk	kkkk
----	------	------	------

**Description:**      GOTO is an unconditional branch. The eleven bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH<4:3>. GOTO is a two-cycle instruction.

**Words:**      1

**Cycles:**      2

**Example**

```

    GOTO THERE
    
```

**After Instruction**  
 PC = Address THERE

## INCF      Increment f

**Syntax:**      `[label] INCF f,d`

**Operands:**       $0 \leq f \leq 127$   
 $d \in [0,1]$

**Operation:**       $(f) + 1 \rightarrow (\text{dest})$

**Status Affected:**      Z

**Encoding:**

00	1010	dfff	ffff
----	------	------	------

**Description:**      The contents of register 'f' are incremented. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'.

**Words:**      1

**Cycles:**      1

**Example**

```

    INCF  CNT, 1
    
```

**Before Instruction**  
 CNT = 0xFF  
 Z = 0

**After Instruction**  
 CNT = 0x00  
 Z = 1

# PIC16C62X

## SUBLW Subtract W from Literal

Syntax: [ *label* ] SUBLW k

Operands:  $0 \leq k \leq 255$

Operation:  $k - (W) \rightarrow (W)$

Status C, DC, Z

Affected:

Encoding: 

11	110x	kkkk	kkkk
----	------	------	------

Description: The W register is subtracted (2's complement method) from the eight bit literal 'k'. The result is placed in the W register.

Words: 1

Cycles: 1

Example 1: SUBLW 0x02

Before Instruction

W = 1  
C = ?

After Instruction

W = 1  
C = 1; result is positive

Example 2: Before Instruction

W = 2  
C = ?

After Instruction

W = 0  
C = 1; result is zero

Example 3: Before Instruction

W = 3  
C = ?

After Instruction

W = 0xFF  
C = 0; result is negative

## SUBWF Subtract W from f

Syntax: [ *label* ] SUBWF f,d

Operands:  $0 \leq f \leq 127$   
 $d \in [0,1]$

Operation:  $(f) - (W) \rightarrow (\text{dest})$

Status C, DC, Z

Affected:

Encoding: 

00	0010	dfff	ffff
----	------	------	------

Description: Subtract (2's complement method) W register from register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example 1: SUBWF REG1,1

Before Instruction

REG1= 3  
W = 2  
C = ?

After Instruction

REG1= 1  
W = 2  
C = 1; result is positive

Example 2: Before Instruction

REG1= 2  
W = 2  
C = ?

After Instruction

REG1= 0  
W = 2  
C = 1; result is zero

Example 3: Before Instruction

REG1= 1  
W = 2  
C = ?

After Instruction

REG1= 0xFF  
W = 2  
C = 0; result is negative

SWAPF		Swap Nibbles in f							
Syntax:	[ <i>label</i> ] SWAPF f,d								
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$								
Operation:	$(f<3:0>) \rightarrow (dest<7:4>),$ $(f<7:4>) \rightarrow (dest<3:0>)$								
Status Affected:	None								
Encoding:	<table><tr><td>00</td><td>1110</td><td>dfff</td><td>ffff</td></tr></table>					00	1110	dfff	ffff
00	1110	dfff	ffff						
Description:	The upper and lower nibbles of register 'f' are exchanged. If 'd' is 0, the result is placed in W register. If 'd' is 1, the result is placed in register 'f'.								
Words:	1								
Cycles:	1								
Example	SWAPF REG, 0								
	Before Instruction								
	REG1 = 0xA5								
	After Instruction								
	REG1 = 0xA5								
	W = 0x5A								

TRIS	Load TRIS Register				
Syntax:	[ <i>label</i> ] TRIS f				
Operands:	$5 \leq f \leq 7$				
Operation:	(W) → TRIS register f;				
Status Affected:	None				
Encoding:	<table><tr><td>00</td><td>0000</td><td>0110</td><td>0fff</td></tr></table>	00	0000	0110	0fff
00	0000	0110	0fff		
Description:	The instruction is supported for code compatibility with the PIC16C5X products. Since TRIS registers are readable and writable, the user can directly address them.				
Words:	1				
Cycles:	1				
Example	<div><b>To maintain upward compatibility with future PICmicro<sup>®</sup> products, do not use this instruction.</b></div>				

XORLW		Exclusive OR Literal with W			
Syntax:	[ <i>label</i> XORLW   k 				

XORWF

Exclusive OR W with f

Syntax:

[ *label* ] XORWF f,d

Operands:

$0 \leq f \leq 127$   
 $d \in [0,1]$

Operation:

(W) .XOR. (f) → (dest)

Status Affected:

Z

Encoding:

00	0110	dfff	ffff
----	------	------	------

Description:

Exclusive OR the contents of the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

Words:

1

Cycles:

1

Example

XORWF REG 1

Before Instruction

REG = 0xAF

W = 0xB5

After Instruction

REG = 0x1A

W = 0xB5

## 11.9 MPLAB ICE 2000 High Performance Universal In-Circuit Emulator

The MPLAB ICE 2000 universal in-circuit emulator is intended to provide the product development engineer with a complete microcontroller design tool set for PICmicro microcontrollers. Software control of the MPLAB ICE 2000 in-circuit emulator is advanced by the MPLAB Integrated Development Environment, which allows editing, building, downloading and source debugging from a single environment.

The MPLAB ICE 2000 is a full-featured emulator system with enhanced trace, trigger and data monitoring features. Interchangeable processor modules allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the MPLAB ICE in-circuit emulator allows expansion to support new PICmicro microcontrollers.

The MPLAB ICE 2000 in-circuit emulator system has been designed as a real-time emulation system with advanced features that are typically found on more expensive development tools. The PC platform and Microsoft® Windows 32-bit operating system were chosen to best make these features available in a simple, unified application.

## 11.10 MPLAB ICE 4000 High Performance Universal In-Circuit Emulator

The MPLAB ICE 4000 universal in-circuit emulator is intended to provide the product development engineer with a complete microcontroller design tool set for high-end PICmicro microcontrollers. Software control of the MPLAB ICE in-circuit emulator is provided by the MPLAB Integrated Development Environment, which allows editing, building, downloading and source debugging from a single environment.

The MPLAB ICE 4000 is a premium emulator system, providing the features of MPLAB ICE 2000, but with increased emulation memory and high speed performance for dsPIC30F and PIC18XXXX devices. Its advanced emulator features include complex triggering and timing, up to 2 Mb of emulation memory, and the ability to view variables in real-time.

The MPLAB ICE 4000 in-circuit emulator system has been designed as a real-time emulation system with advanced features that are typically found on more expensive development tools. The PC platform and Microsoft Windows 32-bit operating system were chosen to best make these features available in a simple, unified application.

## 11.11 MPLAB ICD 2 In-Circuit Debugger

Microchip's In-Circuit Debugger, MPLAB ICD 2, is a powerful, low cost, run-time development tool, connecting to the host PC via an RS-232 or high speed USB interface. This tool is based on the FLASH PICmicro MCUs and can be used to develop for these and other PICmicro microcontrollers. The MPLAB ICD 2 utilizes the in-circuit debugging capability built into the FLASH devices. This feature, along with Microchip's In-Circuit Serial Programming™ (ICSP™) protocol, offers cost effective in-circuit FLASH debugging from the graphical user interface of the MPLAB Integrated Development Environment. This enables a designer to develop and debug source code by setting breakpoints, single-stepping and watching variables, CPU status and peripheral registers. Running at full speed enables testing hardware and applications in real-time. MPLAB ICD 2 also serves as a development programmer for selected PICmicro devices.

## 11.12 PRO MATE II Universal Device Programmer

The PRO MATE II is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features an LCD display for instructions and error messages and a modular detachable socket assembly to support various package types. In Stand-Alone mode, the PRO MATE II device programmer can read, verify, and program PICmicro devices without a PC connection. It can also set code protection in this mode.

## 11.13 PICSTART Plus Development Programmer

The PICSTART Plus development programmer is an easy-to-use, low cost, prototype programmer. It connects to the PC via a COM (RS-232) port. MPLAB Integrated Development Environment software makes using the programmer simple and efficient. The PICSTART Plus development programmer supports most PICmicro devices up to 40 pins. Larger pin count devices, such as the PIC16C92X and PIC17C76X, may be supported with an adapter socket. The PICSTART Plus development programmer is CE compliant.

## 12.0 ELECTRICAL SPECIFICATIONS

### Absolute Maximum Ratings †

Ambient Temperature under bias .....	-40° to +125°C
Storage Temperature .....	-65° to +150°C
Voltage on any pin with respect to VSS (except VDD and $\overline{\text{MCLR}}$ ) .....	-0.6V to VDD +0.6V
Voltage on VDD with respect to VSS .....	0 to +7.5V
Voltage on $\overline{\text{MCLR}}$ with respect to VSS ( <b>Note 2</b> ) .....	0 to +14V
Voltage on RA4 with respect to VSS .....	8.5V
Total power Dissipation ( <b>Note 1</b> ) .....	1.0W
Maximum Current out of VSS pin .....	300 mA
Maximum Current into VDD pin .....	250 mA
Input Clamp Current, I <sub>IK</sub> (V <sub>I</sub> < 0 or V <sub>I</sub> > VDD) .....	±20 mA
Output Clamp Current, I <sub>OK</sub> (V <sub>O</sub> < 0 or V <sub>O</sub> > VDD) .....	±20 mA
Maximum Output Current sunk by any I/O pin .....	25 mA
Maximum Output Current sourced by any I/O pin .....	25 mA
Maximum Current sunk by PORTA and PORTB .....	200 mA
Maximum Current sourced by PORTA and PORTB .....	200 mA

**Note 1:** Power dissipation is calculated as follows:  $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$ .

**2:** Voltage spikes below VSS at the  $\overline{\text{MCLR}}$  pin, inducing currents greater than 80 mA, may cause latchup. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the  $\overline{\text{MCLR}}$  pin rather than pulling this pin directly to VSS.

† **NOTICE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

## 12.1 DC Characteristics: PIC16C62X-04 (Commercial, Industrial, Extended) PIC16C62X-20 (Commercial, Industrial, Extended) PIC16LC62X-04 (Commercial, Industrial, Extended) (CONT.)

PIC16C62X		Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial and $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial and $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended					
PIC16LC62X		Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial and $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial and $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended Operating voltage $V_{DD}$ range is the PIC16C62X range.					
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D022	$\Delta I_{WDT}$	WDT Current <sup>(5)</sup>	—	6.0	20	$\mu\text{A}$	$V_{DD}=4.0\text{V}$ (125°C)
D022A	$\Delta I_{BOR}$	Brown-out Reset Current <sup>(5)</sup>	—	350	425	$\mu\text{A}$	BOD enabled, $V_{DD} = 5.0\text{V}$
D023	$\Delta I_{COMP}$	Comparator Current for each Comparator <sup>(5)</sup>	—	—	100	$\mu\text{A}$	$V_{DD} = 4.0\text{V}$
D023A	$\Delta I_{VREF}$	VREF Current <sup>(5)</sup>	—	—	300	$\mu\text{A}$	$V_{DD} = 4.0\text{V}$
D022	$\Delta I_{WDT}$	WDT Current <sup>(5)</sup>	—	6.0	15	$\mu\text{A}$	$V_{DD}=3.0\text{V}$
D022A	$\Delta I_{BOR}$	Brown-out Reset Current <sup>(5)</sup>	—	350	425	$\mu\text{A}$	BOD enabled, $V_{DD} = 5.0\text{V}$
D023	$\Delta I_{COMP}$	Comparator Current for each Comparator <sup>(5)</sup>	—	—	100	$\mu\text{A}$	$V_{DD} = 3.0\text{V}$
D023A	$\Delta I_{VREF}$	VREF Current <sup>(5)</sup>	—	—	300	$\mu\text{A}$	$V_{DD} = 3.0\text{V}$
1A	FOSC	LP Oscillator Operating Frequency	0	—	200	kHz	All temperatures
		RC Oscillator Operating Frequency	0	—	4	MHz	All temperatures
		XT Oscillator Operating Frequency	0	—	4	MHz	All temperatures
		HS Oscillator Operating Frequency	0	—	20	MHz	All temperatures
1A	FOSC	LP Oscillator Operating Frequency	0	—	200	kHz	All temperatures
		RC Oscillator Operating Frequency	0	—	4	MHz	All temperatures
		XT Oscillator Operating Frequency	0	—	4	MHz	All temperatures
		HS Oscillator Operating Frequency	0	—	20	MHz	All temperatures

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** This is the limit to which  $V_{DD}$  can be lowered without losing RAM data.

**2:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all  $I_{DD}$  measurements in Active Operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tri-stated, pulled to  $V_{DD}$ ,

MCLR =  $V_{DD}$ ; WDT enabled/disabled as specified.

**3:** The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to  $V_{DD}$  or  $V_{SS}$ .

**4:** For RC osc configuration, current through REXT is not included. The current through the resistor can be estimated by the formula:  $I_r = V_{DD}/2R_{EXT}$  (mA) with  $R_{EXT}$  in k $\Omega$ .

**5:** The  $\Delta$  current is the additional current consumed when this peripheral is enabled. This current should be added to the base  $I_{DD}$  or  $I_{PD}$  measurement.



## 12.2 DC Characteristics: PIC16C62XA-04 (Commercial, Industrial, Extended) PIC16C62XA-20 (Commercial, Industrial, Extended) PIC16LC62XA-04 (Commercial, Industrial, Extended) (CONT.)

PIC16C62XA			Standard Operating Conditions (unless otherwise stated)				
			Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial and -40°C ≤ TA ≤ +125°C for extended				
PIC16LC62XA			Standard Operating Conditions (unless otherwise stated)				
			Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial and -40°C ≤ TA ≤ +125°C for extended				
Param. No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D010	IDD	Supply Current <sup>(2, 4)</sup>	—	1.2	2.0	mA	FOSC = 4 MHz, VDD = 5.5V, WDT disabled, XT mode, <b>(Note 4)*</b>
			—	0.4	1.2	mA	FOSC = 4 MHz, VDD = 3.0V, WDT disabled, XT mode, <b>(Note 4)*</b>
			—	1.0	2.0	mA	FOSC = 10 MHz, VDD = 3.0V, WDT disabled, HS mode, <b>(Note 6)</b>
			—	4.0	6.0	mA	FOSC = 20 MHz, VDD = 4.5V, WDT disabled, HS mode
			—	4.0	7.0	mA	FOSC = 20 MHz, VDD = 5.5V, WDT disabled*, HS mode
			—	35	70	μA	FOSC = 32 kHz, VDD = 3.0V, WDT disabled, LP mode
D010	IDD	Supply Current <sup>(2)</sup>	—	1.2	2.0	mA	FOSC = 4 MHz, VDD = 5.5V, WDT disabled, XT mode, <b>(Note 4)*</b>
			—	—	1.1	mA	FOSC = 4 MHz, VDD = 2.5V, WDT disabled, XT mode, <b>(Note 4)</b>
			—	35	70	μA	FOSC = 32 kHz, VDD = 2.5V, WDT disabled, LP mode
D020	IPD	Power-down Current <sup>(3)</sup>	—	—	2.2	μA	VDD = 3.0V
			—	—	5.0	μA	VDD = 4.5V*
			—	—	9.0	μA	VDD = 5.5V
			—	—	15	μA	VDD = 5.5V Extended Temp.
D020	IPD	Power-down Current <sup>(3)</sup>	—	—	2.0	μA	VDD = 2.5V
			—	—	2.2	μA	VDD = 3.0V*
			—	—	9.0	μA	VDD = 5.5V
			—	—	15	μA	VDD = 5.5V Extended Temp.

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** This is the limit to which VDD can be lowered without losing RAM data.

**2:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in Active Operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tri-stated, pulled to VDD,

MCLR = VDD; WDT enabled/disabled as specified.

**3:** The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or VSS.

**4:** For RC osc configuration, current through REXT is not included. The current through the resistor can be estimated by the formula:  $I_r = V_{DD}/2R_{EXT}$  (mA) with REXT in kΩ.

**5:** The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

**6:** Commercial temperature range only.

# PIC16C62X

## 12.2 DC Characteristics: PIC16C62XA-04 (Commercial, Industrial, Extended) PIC16C62XA-20 (Commercial, Industrial, Extended) PIC16LC62XA-04 (Commercial, Industrial, Extended (CONT.))

PIC16C62XA			Standard Operating Conditions (unless otherwise stated)				
			Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial and -40°C ≤ TA ≤ +125°C for extended				
PIC16LC62XA			Standard Operating Conditions (unless otherwise stated)				
			Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial and -40°C ≤ TA ≤ +125°C for extended				
Param. No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D022	ΔI <sub>WDT</sub>	WDT Current <sup>(5)</sup>	—	6.0	10	μA	V <sub>DD</sub> = 4.0V (125°C)
D022A	ΔI <sub>BOR</sub>	Brown-out Reset Current <sup>(5)</sup>	—	75	125	μA	BOD enabled, V <sub>DD</sub> = 5.0V
D023	ΔI <sub>COMP</sub>	Comparator Current for each Comparator <sup>(5)</sup>	—	30	60	μA	V <sub>DD</sub> = 4.0V
D023A	ΔI <sub>VREF</sub>	VREF Current <sup>(5)</sup>	—	80	135	μA	V <sub>DD</sub> = 4.0V
D022	ΔI <sub>WDT</sub>	WDT Current <sup>(5)</sup>	—	6.0	10	μA	V <sub>DD</sub> = 4.0V (125°C)
D022A	ΔI <sub>BOR</sub>	Brown-out Reset Current <sup>(5)</sup>	—	75	125	μA	BOD enabled, V <sub>DD</sub> = 5.0V
D023	ΔI <sub>COMP</sub>	Comparator Current for each Comparator <sup>(5)</sup>	—	30	60	μA	V <sub>DD</sub> = 4.0V
D023A	ΔI <sub>VREF</sub>	VREF Current <sup>(5)</sup>	—	80	135	μA	V <sub>DD</sub> = 4.0V
1A	FOSC	LP Oscillator Operating Frequency	0	—	200	kHz	All temperatures
		RC Oscillator Operating Frequency	0	—	4	MHz	All temperatures
		XT Oscillator Operating Frequency	0	—	4	MHz	All temperatures
		HS Oscillator Operating Frequency	0	—	20	MHz	All temperatures
1A	FOSC	LP Oscillator Operating Frequency	0	—	200	kHz	All temperatures
		RC Oscillator Operating Frequency	0	—	4	MHz	All temperatures
		XT Oscillator Operating Frequency	0	—	4	MHz	All temperatures
		HS Oscillator Operating Frequency	0	—	20	MHz	All temperatures

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** This is the limit to which V<sub>DD</sub> can be lowered without losing RAM data.

**2:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all I<sub>DD</sub> measurements in Active Operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tri-stated, pulled to V<sub>DD</sub>,

MCLR = V<sub>DD</sub>; WDT enabled/disabled as specified.

**3:** The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to V<sub>DD</sub> or V<sub>SS</sub>.

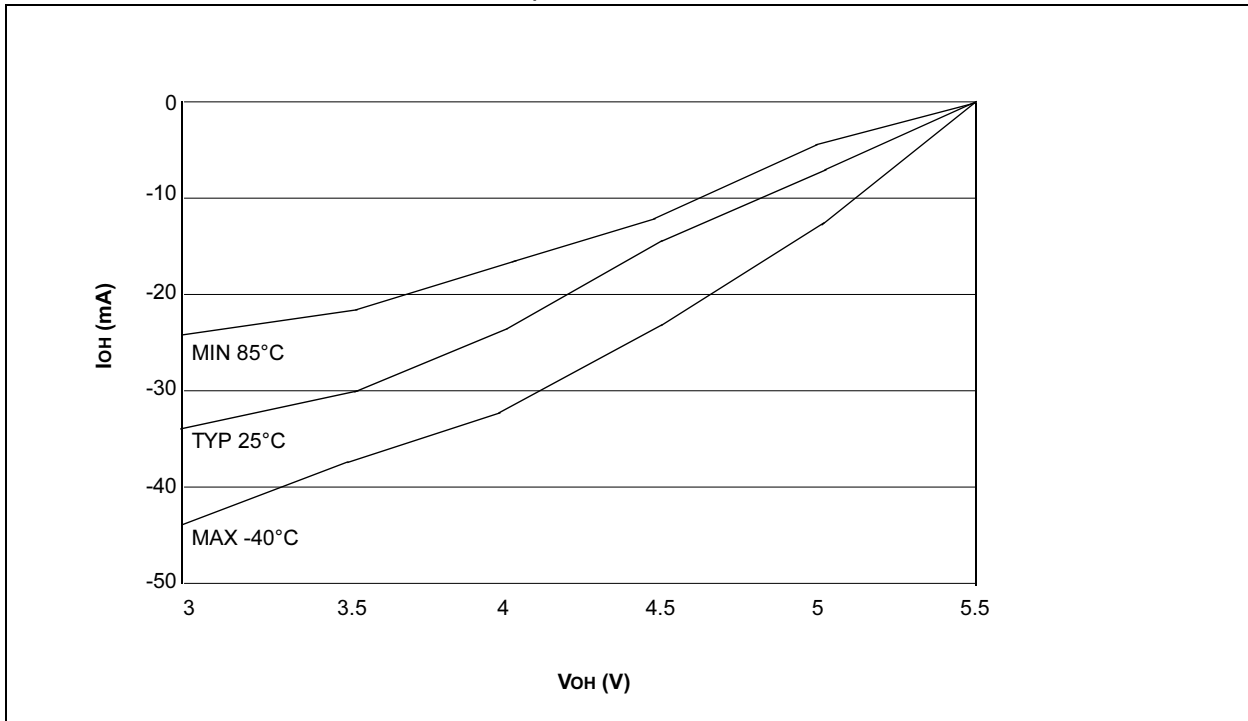
**4:** For RC osc configuration, current through R<sub>EXT</sub> is not included. The current through the resistor can be estimated by the formula: I<sub>r</sub> = V<sub>DD</sub>/2R<sub>EXT</sub> (mA) with R<sub>EXT</sub> in kΩ.

**5:** The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base I<sub>DD</sub> or I<sub>PD</sub> measurement.

**6:** Commercial temperature range only.

# PIC16C62X

FIGURE 13-7:  $I_{OH}$  vs.  $V_{OH}$ ,  $V_{DD} = 5.5V$



# PIC16C62X

---

NOTES:

## APPENDIX A: ENHANCEMENTS

The following are the list of enhancements over the PIC16C5X microcontroller family:

1. Instruction word length is increased to 14 bits. This allows larger page sizes both in program memory (4K now as opposed to 512 before) and register file (up to 128 bytes now versus 32 bytes before).
2. A PC high latch register (PCLATH) is added to handle program memory paging. PA2, PA1, PA0 bits are removed from STATUS register.
3. Data memory paging is slightly redefined. STATUS register is modified.
4. Four new instructions have been added: RETURN, RETFIE, ADDLW, and SUBLW. Two instructions TRIS and OPTION are being phased out, although they are kept for compatibility with PIC16C5X.
5. OPTION and TRIS registers are made addressable.
6. Interrupt capability is added. Interrupt vector is at 0004h.
7. Stack size is increased to 8 deep.
8. RESET vector is changed to 0000h.
9. RESET of all registers is revisited. Five different RESET (and wake-up) types are recognized. Registers are reset differently.
10. Wake-up from SLEEP through interrupt is added.
11. Two separate timers, Oscillator Start-up Timer (OST) and Power-up Timer (PWRT) are included for more reliable power-up. These timers are invoked selectively to avoid unnecessary delays on power-up and wake-up.
12. PORTB has weak pull-ups and interrupt-on-change feature.
13. Timer0 clock input, T0CKI pin is also a port pin (RA4/T0CKI) and has a TRIS bit.
14. FSR is made a full 8-bit register.
15. "In-circuit programming" is made possible. The user can program PIC16CXX devices using only five pins: VDD, VSS, VPP, RB6 (clock) and RB7 (data in/out).
16. PCON STATUS register is added with a Power-on-Reset (POR) STATUS bit and a Brown-out Reset STATUS bit (BOD).
17. Code protection scheme is enhanced such that portions of the program memory can be protected, while the remainder is unprotected.
18. PORTA inputs are now Schmitt Trigger inputs.
19. Brown-out Reset reset has been added.
20. Common RAM registers F0h-FFh implemented in bank1.

## APPENDIX B: COMPATIBILITY

To convert code written for PIC16C5X to PIC16CXX, the user should take the following steps:

1. Remove any program memory page select operations (PA2, PA1, PA0 bits) for CALL, GOTO.
2. Revisit any computed jump operations (write to PC or add to PC, etc.) to make sure page bits are set properly under the new scheme.
3. Eliminate any data memory page switching. Redefine data variables to reallocate them.
4. Verify all writes to STATUS, OPTION, and FSR registers since these have changed.
5. Change RESET vector to 0000h.