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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	13
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	96 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	18-DIP (0.300", 7.62mm)
Supplier Device Package	18-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lc621a-04e-p

EPROM-Based 8-Bit CMOS Microcontrollers

Devices included in this data sheet:

Referred to collectively as PIC16C62X.

- PIC16C620 • PIC16C620A
- PIC16C621 • PIC16C621A
- PIC16C622 • PIC16C622A
- PIC16CR620A

High Performance RISC CPU:

- Only 35 instructions to learn
- All single cycle instructions (200 ns), except for program branches which are two-cycle
- Operating speed:
 - DC - 40 MHz clock input
 - DC - 100 ns instruction cycle

Device	Program Memory	Data Memory
PIC16C620	512	80
PIC16C620A	512	96
PIC16CR620A	512	96
PIC16C621	1K	80
PIC16C621A	1K	96
PIC16C622	2K	128
PIC16C622A	2K	128

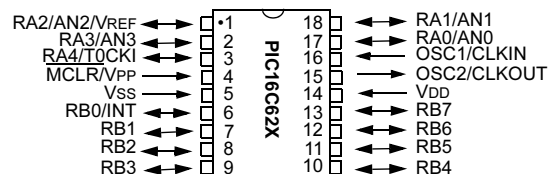
- Interrupt capability
- 16 special function hardware registers
- 8-level deep hardware stack
- Direct, Indirect and Relative addressing modes

Peripheral Features:

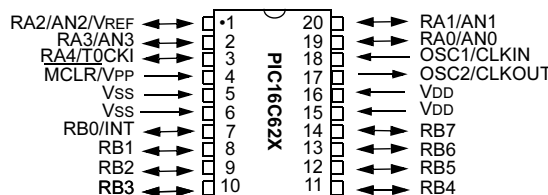
- 13 I/O pins with individual direction control
- High current sink/source for direct LED drive
- Analog comparator module with:
 - Two analog comparators
 - Programmable on-chip voltage reference (VREF) module
 - Programmable input multiplexing from device inputs and internal voltage reference
 - Comparator outputs can be output signals
- Timer0: 8-bit timer/counter with 8-bit programmable prescaler

Pin Diagrams

PDIP, SOIC, Windowed Cerdip



SSOP



Special Microcontroller Features:

- Power-on Reset (POR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Brown-out Reset
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Programmable code protection
- Power saving SLEEP mode
- Selectable oscillator options
- Serial in-circuit programming (via two pins)
- Four user programmable ID locations

CMOS Technology:

- Low power, high speed CMOS EPROM technology
- Fully static design
- Wide operating range
 - 2.5V to 5.5V
- Commercial, industrial and extended temperature range
- Low power consumption
 - < 2.0 mA @ 5.0V, 4.0 MHz
 - 15 μ A typical @ 3.0V, 32 kHz
 - < 1.0 μ A typical standby current @ 3.0V

PIC16C62X

Device Differences

Device	Voltage Range	Oscillator	Process Technology (Microns)
PIC16C620 ⁽³⁾	2.5 - 6.0	See Note 1	0.9
PIC16C621 ⁽³⁾	2.5 - 6.0	See Note 1	0.9
PIC16C622 ⁽³⁾	2.5 - 6.0	See Note 1	0.9
PIC16C620A ⁽⁴⁾	2.7 - 5.5	See Note 1	0.7
PIC16CR620A ⁽²⁾	2.5 - 5.5	See Note 1	0.7
PIC16C621A ⁽⁴⁾	2.7 - 5.5	See Note 1	0.7
PIC16C622A ⁽⁴⁾	2.7 - 5.5	See Note 1	0.7

Note 1: If you change from this device to another device, please verify oscillator characteristics in your application.

2: For ROM parts, operation from 2.5V - 3.0V will require the PIC16LCR62X parts.

3: For OTP parts, operation from 2.5V - 3.0V will require the PIC16LC62X parts.

4: For OTP parts, operations from 2.7V - 3.0V will require the PIC16LC62XA parts.

PIC16C62X

TABLE 1-1: PIC16C62X FAMILY OF DEVICES

		PIC16C620 ⁽³⁾	PIC16C620A ⁽¹⁾⁽⁴⁾	PIC16CR620A ⁽²⁾	PIC16C621 ⁽³⁾	PIC16C621A ⁽¹⁾⁽⁴⁾	PIC16C622 ⁽³⁾	PIC16C622A ⁽¹⁾⁽⁴⁾
Clock	Maximum Frequency of Operation (MHz)	20	40	20	20	40	20	40
Memory	EPROM Program Memory (x14 words)	512	512	512	1K	1K	2K	2K
	Data Memory (bytes)	80	96	96	80	96	128	128
Peripherals	Timer Module(s)	TMR0	TMR0	TMRO	TMR0	TMR0	TMR0	TMR0
	Comparators(s)	2	2	2	2	2	2	2
	Internal Reference Voltage	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Features	Interrupt Sources	4	4	4	4	4	4	4
	I/O Pins	13	13	13	13	13	13	13
	Voltage Range (Volts)	2.5-6.0	2.7-5.5	2.5-5.5	2.5-6.0	2.7-5.5	2.5-6.0	2.7-5.5
	Brown-out Reset	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	Packages	18-pin DIP, SOIC, 20-pin SSOP	18-pin DIP, SOIC, 20-pin SSOP	18-pin DIP, SOIC, 20-pin SSOP	18-pin DIP, SOIC, 20-pin SSOP	18-pin DIP, SOIC, 20-pin SSOP	18-pin DIP, SOIC, 20-pin SSOP	18-pin DIP, SOIC, 20-pin SSOP

All PICmicro[®] Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability. All PIC16C62X Family devices use serial programming with clock pin RB6 and data pin RB7.

- Note 1:** If you change from this device to another device, please verify oscillator characteristics in your application.
- 2:** For ROM parts, operation from 2.0V - 2.5V will require the PIC16LCR62XA parts.
- 3:** For OTP parts, operation from 2.5V - 3.0V will require the PIC16LC62X part.
- 4:** For OTP parts, operation from 2.7V - 3.0V will require the PIC16LC62XA part.

2.0 PIC16C62X DEVICE VARIETIES

A variety of frequency ranges and packaging options are available. Depending on application and production requirements, the proper device option can be selected using the information in the PIC16C62X Product Identification System section at the end of this data sheet. When placing orders, please use this page of the data sheet to specify the correct part number.

2.1 UV Erasable Devices

The UV erasable version, offered in CERDIP package, is optimal for prototype development and pilot programs. This version can be erased and reprogrammed to any of the Oscillator modes.

Microchip's PICSTART® and PRO MATE® programmers both support programming of the PIC16C62X.

Note: Microchip does not recommend code protecting windowed devices.

2.2 One-Time-Programmable (OTP) Devices

The availability of OTP devices is especially useful for customers who need the flexibility for frequent code updates and small volume applications. In addition to the program memory, the configuration bits must also be programmed.

2.3 Quick-Turnaround-Production (QTP) Devices

Microchip offers a QTP programming service for factory production orders. This service is made available for users who chose not to program a medium to high quantity of units and whose code patterns have stabilized. The devices are identical to the OTP devices, but with all EPROM locations and configuration options already programmed by the factory. Certain code and prototype verification procedures apply before production shipments are available. Please contact your Microchip Technology sales office for more details.

2.4 Serialized Quick-Turnaround-ProductionSM (SQTPSM) Devices

Microchip offers a unique programming service where a few user-defined locations in each device are programmed with different serial numbers. The serial numbers may be random, pseudo-random or sequential.

Serial programming allows each device to have a unique number, which can serve as an entry-code, password or ID number.

TABLE 3-1: PIC16C62X PINOUT DESCRIPTION

Name	DIP/SOIC Pin #	SSOP Pin #	I/O/P Type	Buffer Type	Description
OSC1/CLKIN	16	18	I	ST/CMOS	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	15	17	O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. In RC mode, OSC2 pin outputs CLKOUT, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
MCLR/VPP	4	4	I/P	ST	Master Clear (Reset) input/programming voltage input. This pin is an Active Low Reset to the device.
RA0/AN0	17	19	I/O	ST	PORTA is a bi-directional I/O port. Analog comparator input Analog comparator input Analog comparator input or VREF output Analog comparator input /output Can be selected to be the clock input to the Timer0 timer/counter or a comparator output. Output is open drain type.
RA1/AN1	18	20	I/O	ST	
RA2/AN2/VREF	1	1	I/O	ST	
RA3/AN3	2	2	I/O	ST	
RA4/T0CKI	3	3	I/O	ST	
RB0/INT	6	7	I/O	TTL/ST ⁽¹⁾	PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs. RB0/INT can also be selected as an external interrupt pin. Interrupt-on-change pin. Interrupt-on-change pin. Interrupt-on-change pin. Serial programming clock. Interrupt-on-change pin. Serial programming data.
RB1	7	8	I/O	TTL	
RB2	8	9	I/O	TTL	
RB3	9	10	I/O	TTL	
RB4	10	11	I/O	TTL	
RB5	11	12	I/O	TTL	
RB6	12	13	I/O	TTL/ST ⁽²⁾	
RB7	13	14	I/O	TTL/ST ⁽²⁾	
Vss	5	5,6	P	—	Ground reference for logic and I/O pins.
VDD	14	15,16	P	—	Positive supply for logic and I/O pins.

Legend: O = output I/O = input/output P = power
 — = Not used I = Input ST = Schmitt Trigger input
 TTL = TTL input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.
Note 2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.

PIC16C62X

4.2 Data Memory Organization

The data memory (Figure 4-4, Figure 4-5, Figure 4-6 and Figure 4-7) is partitioned into two banks, which contain the General Purpose Registers and the Special Function Registers. Bank 0 is selected when the RP0 bit is cleared. Bank 1 is selected when the RP0 bit (STATUS <5>) is set. The Special Function Registers are located in the first 32 locations of each bank. Register locations 20-7Fh (Bank0) on the PIC16C620A/CR620A/621A and 20-7Fh (Bank0) and A0-BFh (Bank1) on the PIC16C622 and PIC16C622A are General Purpose Registers implemented as static RAM. Some Special Purpose Registers are mapped in Bank 1.

Addresses F0h-FFh of bank1 are implemented as common ram and mapped back to addresses 70h-7Fh in bank0 on the PIC16C620A/621A/622A/CR620A.

4.2.1 GENERAL PURPOSE REGISTER FILE

The register file is organized as 80 x 8 in the PIC16C620/621, 96 x 8 in the PIC16C620A/621A/CR620A and 128 x 8 in the PIC16C622(A). Each is accessed either directly or indirectly through the File Select Register FSR (Section 4.4).

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TABLE 9-4: INITIALIZATION CONDITION FOR SPECIAL REGISTERS

Condition	Program Counter	STATUS Register	PCON Register
Power-on Reset	000h	0001 1xxx	---- --0x
MCLR Reset during normal operation	000h	000u uuuu	---- --uu
MCLR Reset during SLEEP	000h	0001 0uuu	---- --uu
WDT Reset	000h	0000 uuuu	---- --uu
WDT Wake-up	PC + 1	uuu0 0uuu	---- --uu
Brown-out Reset	000h	000x xuuu	---- --u0
Interrupt Wake-up from SLEEP	PC + 1 ⁽¹⁾	uuu1 0uuu	---- --uu

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0'.

Note 1: When the wake-up is due to an interrupt and global enable bit, GIE is set, the PC is loaded with the interrupt vector (0004h) after execution of PC+1.

TABLE 9-5: INITIALIZATION CONDITION FOR REGISTERS

Register	Address	Power-on Reset	<ul style="list-style-type: none"> MCLR Reset during normal operation MCLR Reset during SLEEP WDT Reset Brown-out Reset ⁽¹⁾ 	<ul style="list-style-type: none"> Wake-up from SLEEP through interrupt Wake-up from SLEEP through WDT time-out
W	—	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF	00h	—	—	—
TMR0	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	02h	0000 0000	0000 0000	PC + 1 ⁽³⁾
STATUS	03h	0001 1xxx	000q quuu ⁽⁴⁾	uuuq quuu ⁽⁴⁾
FSR	04h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTA	05h	--x xxxx	--u uuuu	--u uuuu
PORTB	06h	xxxx xxxx	uuuu uuuu	uuuu uuuu
CMCON	1Fh	00-- 0000	00-- 0000	uu-- uuuu
PCLATH	0Ah	---0 0000	---0 0000	---u uuuu
INTCON	0Bh	0000 000x	0000 000u	uuuu uqqq ⁽²⁾
PIR1	0Ch	-0-- ----	-0-- ----	-q-- ---- ^(2,5)
OPTION	81h	1111 1111	1111 1111	uuuu uuuu
TRISA	85h	---1 1111	---1 1111	---u uuuu
TRISB	86h	1111 1111	1111 1111	uuuu uuuu
PIE1	8Ch	-0-- ----	-0-- ----	-u-- ----
PCON	8Eh	---- --0x	---- --uq ^(1,6)	---- --uu
VRCON	9Fh	000- 0000	000- 0000	uuu- uuuu

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0', q = value depends on condition.

Note 1: If VDD goes too low, Power-on Reset will be activated and registers will be affected differently.

Note 2: One or more bits in INTCON, PIR1 and/or PIR2 will be affected (to cause wake-up).

Note 3: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

Note 4: See Table 9-4 for RESET value for specific condition.

Note 5: If wake-up was due to comparator input changing, then bit 6 = 1. All other interrupts generating a wake-up will cause bit 6 = u.

Note 6: If RESET was due to brown-out, then bit 0 = 0. All other RESETS will cause bit 0 = u.

10.1 Instruction Descriptions

ADDLW		Add Literal and W							
Syntax:	[<i>label</i>] ADDLW k								
Operands:	$0 \leq k \leq 255$								
Operation:	$(W) + k \rightarrow (W)$								
Status Affected:	C, DC, Z								
Encoding:	<table border="1"><tr><td>11</td><td>111x</td><td>kkkk</td><td>kkkk</td></tr></table>					11	111x	kkkk	kkkk
11	111x	kkkk	kkkk						
Description:	The contents of the W register are added to the eight bit literal 'k' and the result is placed in the W register.								
Words:	1								
Cycles:	1								
Example	ADDLW 0x15								
	Before Instruction								
	W = 0x10								
	After Instruction								
	W = 0x25								

ADDWF		Add W and f							
Syntax:	[<i>label</i>] ADDWF f,d								
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$								
Operation:	$(W) + (f) \rightarrow (\text{dest})$								
Status Affected:	C, DC, Z								
Encoding:	<table><tr><td>00</td><td>0111</td><td>dfff</td><td>ffff</td></tr></table>					00	0111	dfff	ffff
00	0111	dfff	ffff						
Description:	Add the contents of the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.								
Words:	1								
Cycles:	1								
Example	ADDWF FSR, 0								
	Before Instruction								
	W = 0x17								
	FSR = 0xC2								
	After Instruction								
	W = 0xD9								
	FSR = 0xC2								

ANDLW		AND Literal with W							
Syntax:	[<i>label</i>] ANDLW k								
Operands:	$0 \leq k \leq 255$								
Operation:	$(W) .\text{AND}. (k) \rightarrow (W)$								
Status Affected:	Z								
Encoding:	<table border="1"><tr><td>11</td><td>1001</td><td>kkkk</td><td>kkkk</td></tr></table>					11	1001	kkkk	kkkk
11	1001	kkkk	kkkk						
Description:	The contents of W register are AND'ed with the eight bit literal 'k'. The result is placed in the W register.								
Words:	1								
Cycles:	1								
Example	ANDLW 0x5F								
	Before Instruction								
	W = 0xA3								
	After Instruction								
	W = 0x03								

ANDWF		AND W with f							
Syntax:	[<i>label</i>] ANDWF f,d								
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$								
Operation:	(W) .AND. (f) \rightarrow (dest)								
Status Affected:	Z								
Encoding:	<table border="1"><tr><td>00</td><td>0101</td><td>dfff</td><td>ffff</td></tr></table>					00	0101	dfff	ffff
00	0101	dfff	ffff						
Description:	AND the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.								
Words:	1								
Cycles:	1								
Example	ANDWF FSR, 1								
	Before Instruction								
	W = 0x17								
	FSR = 0xC2								
	After Instruction								
	W = 0x17								
	FSR = 0x02								

Encoding:

00	0000	0000	1001
----	------	------	------

Words: 1

Example RETFIE

Encoding:	11	01xx	kkkk	kkkk
-----------	----	------	------	------

TABLE		;W now has table value
	.	
	.	
	.	
	ADDWF PC	;W = offset
	RETLW k1	;Begin table
	RETLW k2	;
	.	
	.	
	.	
	RETLW kn	; End of table
	Before Instruction	
	W	= 0x07
	After Instruction	
	W	= value of k8

Encoding:

00	0000	0000	1000
----	------	------	------

After Interrupt
PC = TOS

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SUBLW Subtract W from Literal

Syntax: [*label*] SUBLW *k*

Operands: $0 \leq k \leq 255$

Operation: $k - (W) \rightarrow (W)$

Status C, DC, Z

Affected:

Encoding:

11	110x	kkkk	kkkk
----	------	------	------

Description: The W register is subtracted (2's complement method) from the eight bit literal 'k'. The result is placed in the W register.

Words: 1

Cycles: 1

Example 1: SUBLW 0x02

Before Instruction

W = 1
C = ?

After Instruction

W = 1
C = 1; result is positive

Example 2: Before Instruction

W = 2
C = ?

After Instruction

W = 0
C = 1; result is zero

Example 3: Before Instruction

W = 3
C = ?

After Instruction

W = 0xFF
C = 0; result is negative

SUBWF Subtract W from f

Syntax: [*label*] SUBWF *f,d*

Operands: $0 \leq f \leq 127$
 $d \in [0,1]$

Operation: $(f) - (W) \rightarrow (\text{dest})$

Status C, DC, Z

Affected:

Encoding:

00	0010	dfff	ffff
----	------	------	------

Description: Subtract (2's complement method) W register from register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example 1: SUBWF REG1, 1

Before Instruction

REG1 = 3
W = 2
C = ?

After Instruction

REG1 = 1
W = 2
C = 1; result is positive

Example 2: Before Instruction

REG1 = 2
W = 2
C = ?

After Instruction

REG1 = 0
W = 2
C = 1; result is zero

Example 3: Before Instruction

REG1 = 1
W = 2
C = ?

After Instruction

REG1 = 0xFF
W = 2
C = 0; result is negative

PIC16C62X

FIGURE 12-1: PIC16C62X VOLTAGE-FREQUENCY GRAPH, $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$

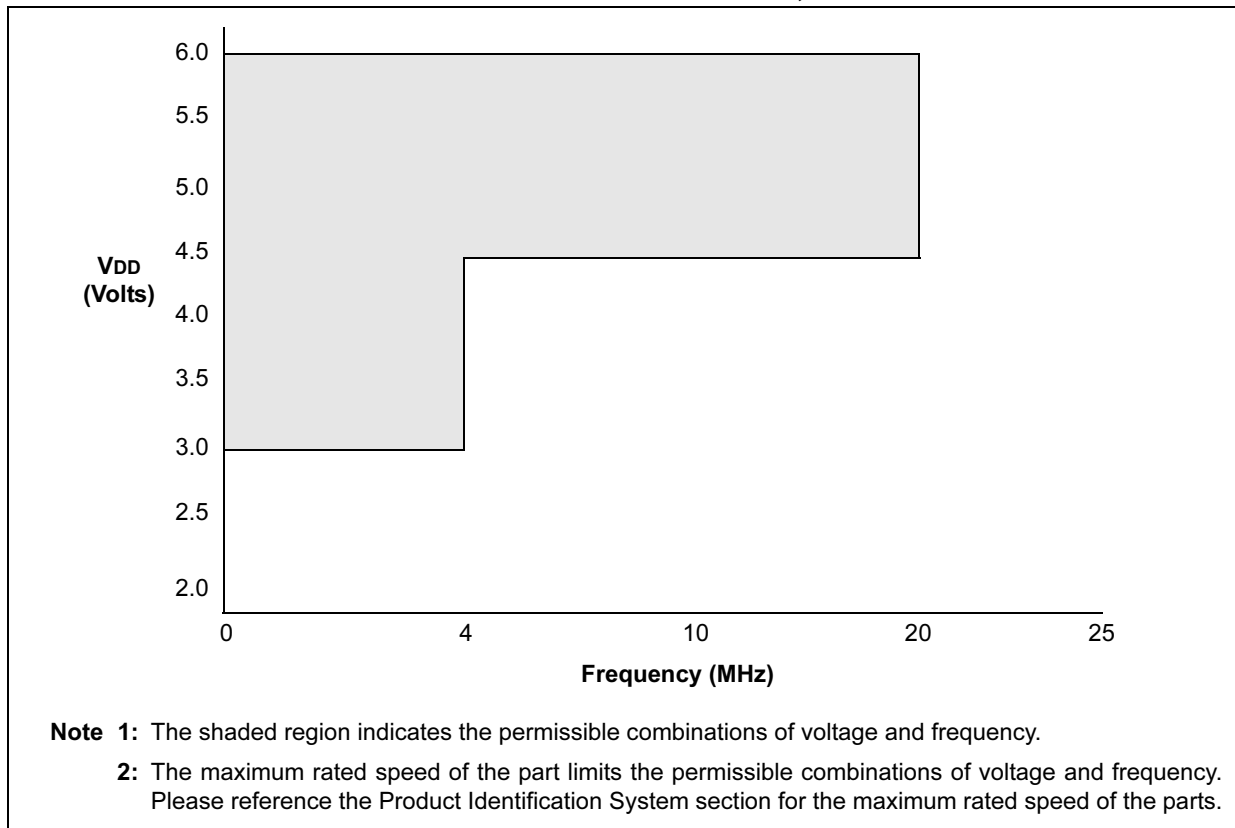
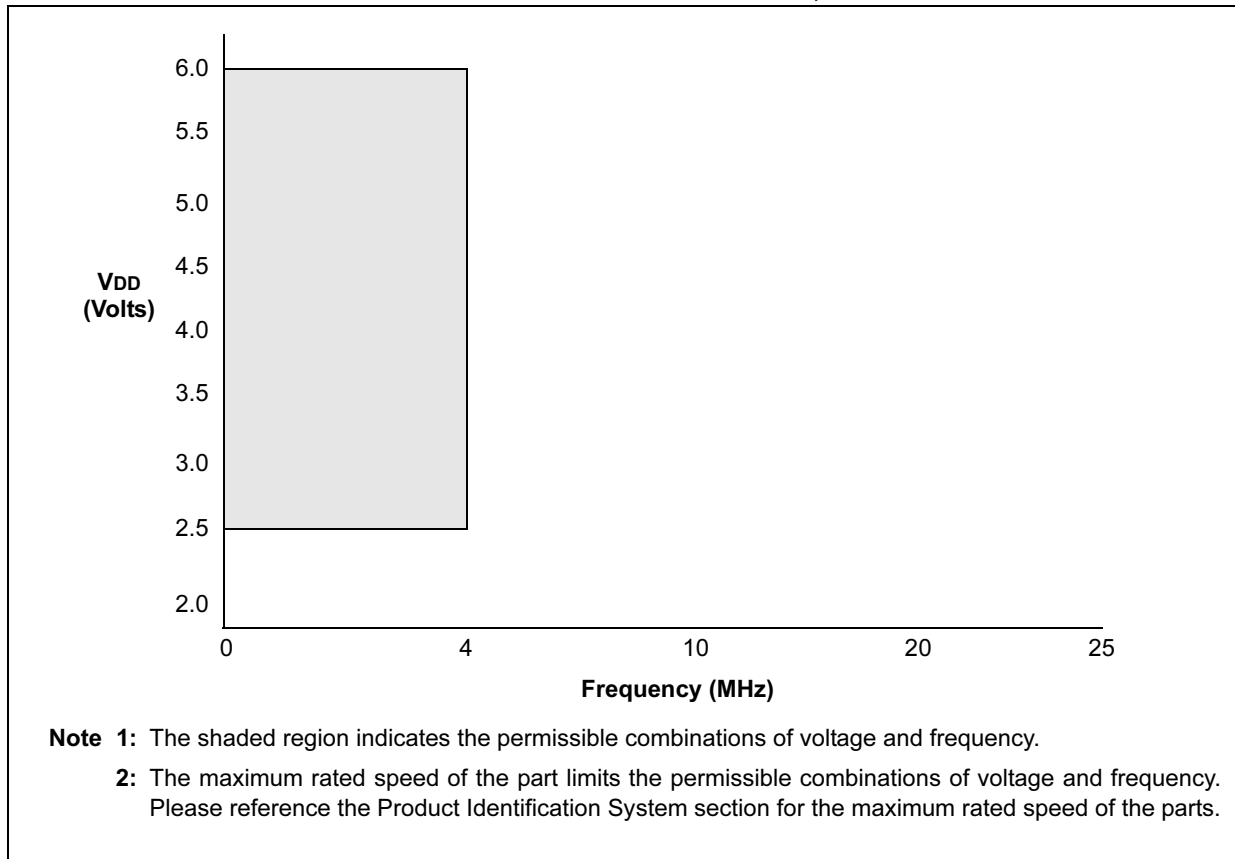


FIGURE 12-2: PIC16LC62X VOLTAGE-FREQUENCY GRAPH, $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$



PIC16C62X

FIGURE 12-5: PIC16LC620A/LC621A/LC622A VOLTAGE-FREQUENCY GRAPH, $-40^{\circ}\text{C} \leq T_A \leq 0^{\circ}\text{C}$

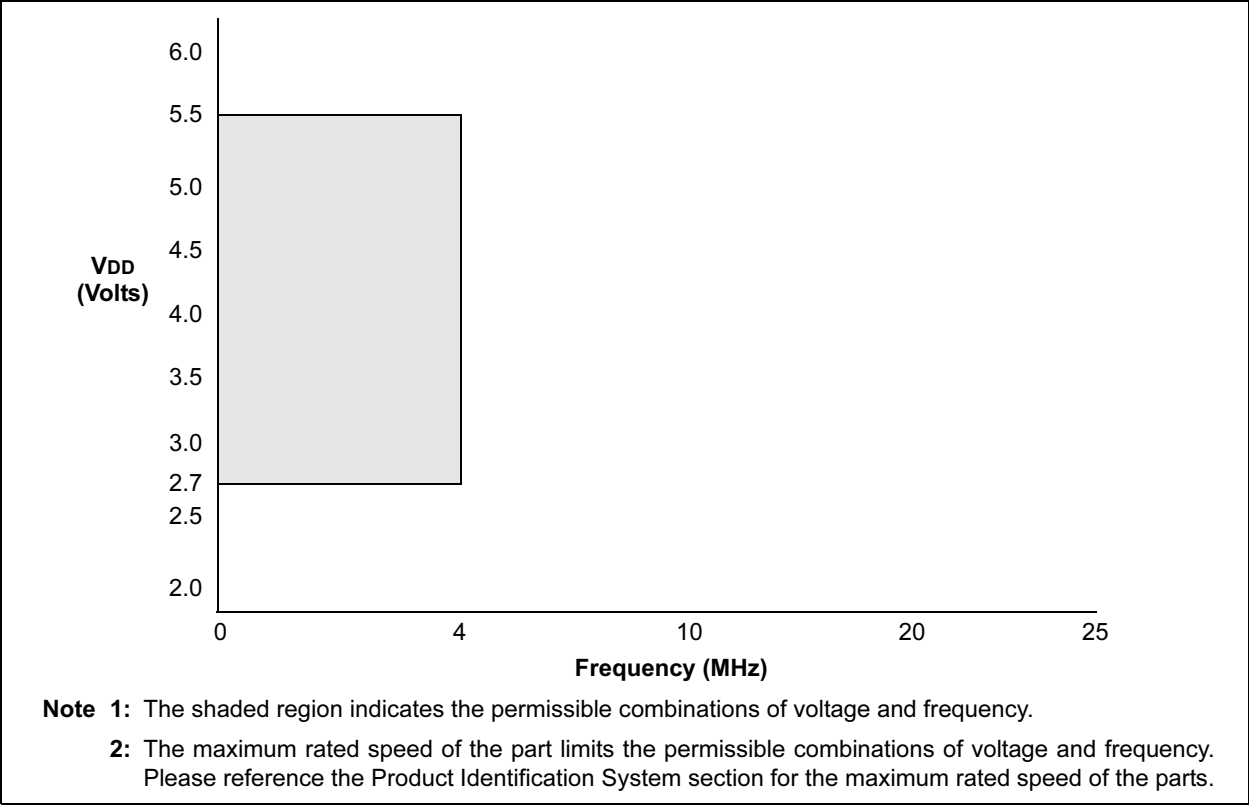
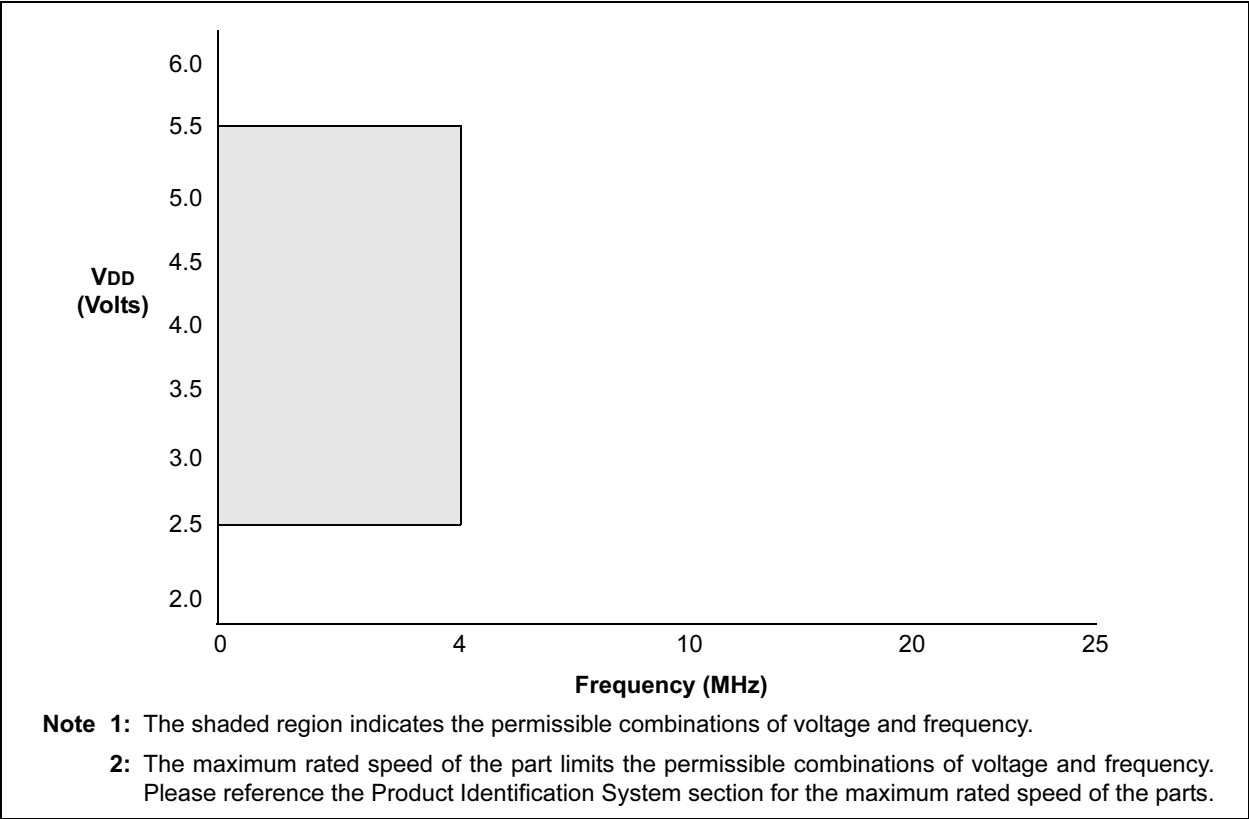


FIGURE 12-6: PIC16LC620A/LC621A/LC622A VOLTAGE-FREQUENCY GRAPH, $0^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$



12.4 DC Characteristics: PIC16C62X/C62XA/CR62XA (Commercial, Industrial, Extended) PIC16LC62X/LC62XA/LCR62XA (Commercial, Industrial, Extended) (CONT.)

PIC16C62X/C62XA/CR62XA			Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial and $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial and $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended				
PIC16LC62X/LC62XA/LCR62XA			Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial and $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial and $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended				
Param. No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D040	V _{IH}	Input High Voltage I/O ports with TTL buffer	2.0V 0.25 V _{DD} + 0.8V	—	V _{DD} V _{DD}	V	V _{DD} = 4.5V to 5.5V otherwise (Note 1)
D041		with Schmitt Trigger input	0.8 V _{DD}	—	V _{DD}	V	
D042		MCLR RA4/T0CKI	0.8 V _{DD}	—	V _{DD}	V	
D043 D043A		OSC1 (XT, HS and LP) OSC1 (in RC mode)	0.7 V _{DD} 0.9 V _{DD}	—	V _{DD}	V	
D070	IPURB	PORTB weak pull-up current	50	200	400	μA	V _{DD} = 5.0V, V _{PIN} = V _{SS}
D070	IPURB	PORTB weak pull-up current	50	200	400	μA	V _{DD} = 5.0V, V _{PIN} = V _{SS}
D060	I _{IL}	Input Leakage Current ^(2, 3) I/O ports (Except PORTA)	—	—	±1.0	μA	V _{SS} ≤ V _{PIN} ≤ V _{DD} , pin at hi-impedance
D061		PORTA	—	—	±0.5	μA	V _{SS} ≤ V _{PIN} ≤ V _{DD} , pin at hi-impedance
D063		RA4/T0CKI	—	—	±1.0	μA	V _{SS} ≤ V _{PIN} ≤ V _{DD}
D063		OSC1, MCLR	—	—	±5.0	μA	V _{SS} ≤ V _{PIN} ≤ V _{DD} , XT, HS and LP osc configuration
D060	I _{IL}	Input Leakage Current ^(2, 3) I/O ports (Except PORTA)	—	—	±1.0	μA	V _{SS} ≤ V _{PIN} ≤ V _{DD} , pin at hi-impedance
D061		PORTA	—	—	±0.5	μA	V _{SS} ≤ V _{PIN} ≤ V _{DD} , pin at hi-impedance
D063		RA4/T0CKI	—	—	±1.0	μA	V _{SS} ≤ V _{PIN} ≤ V _{DD}
D063		OSC1, MCLR	—	—	±5.0	μA	V _{SS} ≤ V _{PIN} ≤ V _{DD} , XT, HS and LP osc configuration
D080	V _{OL}	Output Low Voltage I/O ports	—	—	0.6	V	I _{OL} = 8.5 mA, V _{DD} = 4.5V, -40° to $+85^{\circ}\text{C}$
D083		OSC2/CLKOUT (RC only)	—	—	0.6	V	I _{OL} = 7.0 mA, V _{DD} = 4.5V, $+125^{\circ}\text{C}$
D083		OSC2/CLKOUT (RC only)	—	—	0.6	V	I _{OL} = 1.6 mA, V _{DD} = 4.5V, -40° to $+85^{\circ}\text{C}$
D083		OSC2/CLKOUT (RC only)	—	—	0.6	V	I _{OL} = 1.2 mA, V _{DD} = 4.5V, $+125^{\circ}\text{C}$

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1 pin is a Schmitt Trigger input. It is not recommended that the PIC16C62X(A) be driven with external clock in RC mode.

2: The leakage current on the MCLR pin is strongly dependent on applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

PIC16C62X

12.4 DC Characteristics: PIC16C62X/C62XA/CR62XA (Commercial, Industrial, Extended) PIC16LC62X/LC62XA/LCR62XA (Commercial, Industrial, Extended) (CONT.)

PIC16C62X/C62XA/CR62XA			Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial and $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial and $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended				
PIC16LC62X/LC62XA/LCR62XA			Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial and $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial and $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended				
Param. No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D080	VOL	Output Low Voltage I/O ports	—	—	0.6	V	IOL = 8.5 mA, VDD = 4.5V, -40° to $+85^{\circ}\text{C}$
			—	—	0.6	V	IOL = 7.0 mA, VDD = 4.5V, $+125^{\circ}\text{C}$
D083		OSC2/CLKOUT (RC only)	—	—	0.6	V	IOL = 1.6 mA, VDD = 4.5V, -40° to $+85^{\circ}\text{C}$
			—	—	0.6	V	IOL = 1.2 mA, VDD = 4.5V, $+125^{\circ}\text{C}$
D090	VOH	Output High Voltage ⁽³⁾ I/O ports (Except RA4)	VDD-0.7	—	—	V	IOH = -3.0 mA, VDD = 4.5V, -40° to $+85^{\circ}\text{C}$
			VDD-0.7	—	—	V	IOH = -2.5 mA, VDD = 4.5V, $+125^{\circ}\text{C}$
D092		OSC2/CLKOUT (RC only)	VDD-0.7	—	—	V	IOH = -1.3 mA, VDD = 4.5V, -40° to $+85^{\circ}\text{C}$
			VDD-0.7	—	—	V	IOH = -1.0 mA, VDD = 4.5V, $+125^{\circ}\text{C}$
D090	VOH	Output High Voltage ⁽³⁾ I/O ports (Except RA4)	VDD-0.7	—	—	V	IOH = -3.0 mA, VDD = 4.5V, -40° to $+85^{\circ}\text{C}$
			VDD-0.7	—	—	V	IOH = -2.5 mA, VDD = 4.5V, $+125^{\circ}\text{C}$
D092		OSC2/CLKOUT (RC only)	VDD-0.7	—	—	V	IOH = -1.3 mA, VDD = 4.5V, -40° to $+85^{\circ}\text{C}$
			VDD-0.7	—	—	V	IOH = -1.0 mA, VDD = 4.5V, $+125^{\circ}\text{C}$
D150	VOD	Open-Drain High Voltage			10 8.5*	V	RA4 pin PIC16C62X, PIC16LC62X RA4 pin PIC16C62XA, PIC16LC62XA, PIC16CR62XA, PIC16LCR62XA
D150	VOD	Open-Drain High Voltage			10 8.5*	V	RA4 pin PIC16C62X, PIC16LC62X RA4 pin PIC16C62XA, PIC16LC62XA, PIC16CR62XA, PIC16LCR62XA
D100	COSC 2	Capacitive Loading Specs on Output Pins OSC2 pin			15	pF	In XT, HS and LP modes when external clock used to drive OSC1.
D101	CIO	All I/O pins/OSC2 (in RC mode)			50	pF	
D100	COSC 2	Capacitive Loading Specs on Output Pins OSC2 pin			15	pF	In XT, HS and LP modes when external clock used to drive OSC1.
D101	CIO	All I/O pins/OSC2 (in RC mode)			50	pF	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

- Note 1:** In RC oscillator configuration, the OSC1 pin is a Schmitt Trigger input. It is not recommended that the PIC16C62X(A) be driven with external clock in RC mode.
- 2:** The leakage current on the MCLR pin is strongly dependent on applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
- 3:** Negative current is defined as coming out of the pin.

PIC16C62X

FIGURE 12-16: TIMER0 CLOCK TIMING

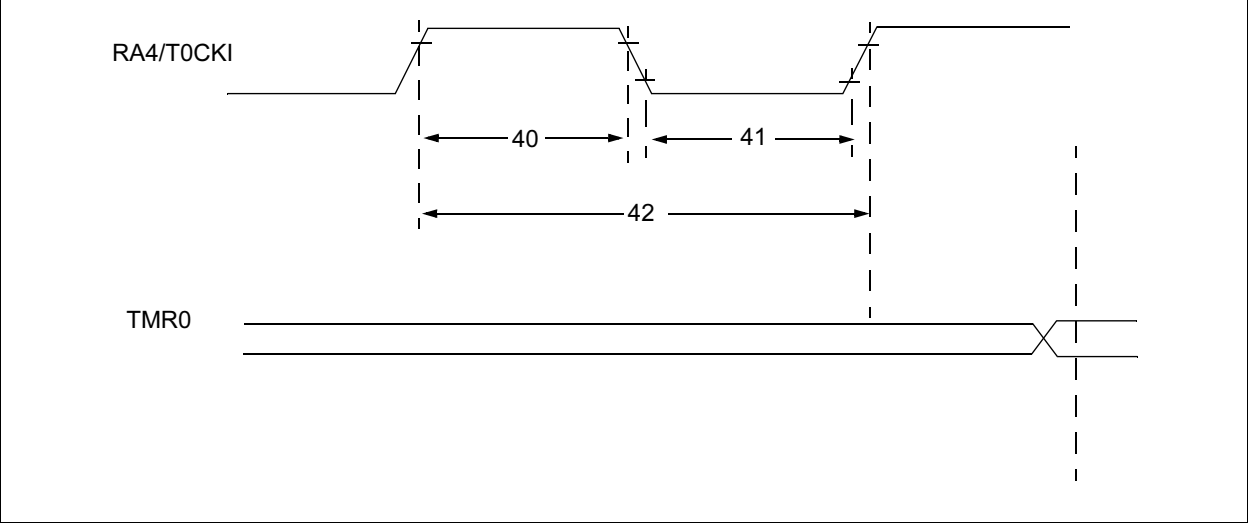


TABLE 12-6: TIMER0 CLOCK REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width	No Prescaler	$0.5 T_{CY} + 20^*$	—	—	ns	
			With Prescaler	10^*	—	—	ns	
41	Tt0L	T0CKI Low Pulse Width	No Prescaler	$0.5 T_{CY} + 20^*$	—	—	ns	
			With Prescaler	10^*	—	—	ns	
42	Tt0P	T0CKI Period		$\frac{T_{CY} + 40^*}{N}$	—	—	ns	N = prescale value (1, 2, 4, ..., 256)

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

PIC16C62X

FIGURE 13-3: I_{DD} VS. V_{DD} (XT OSC 4 MHZ)

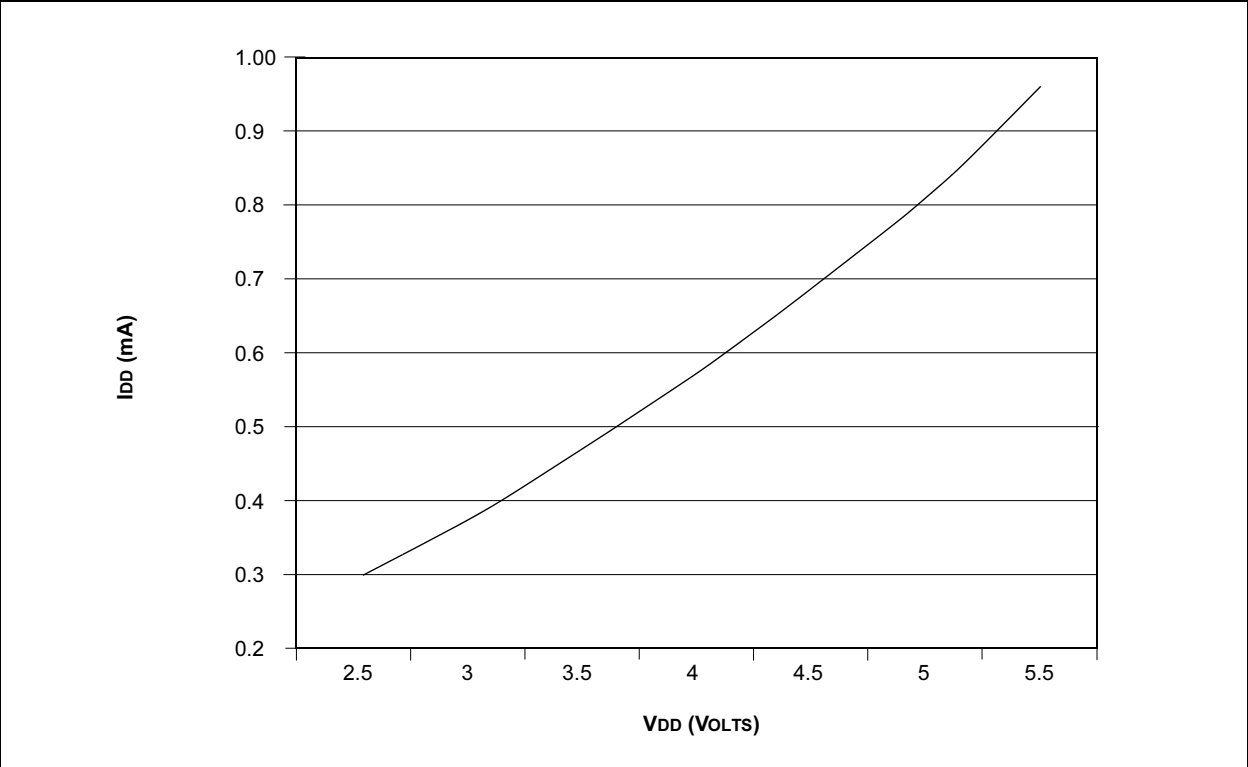
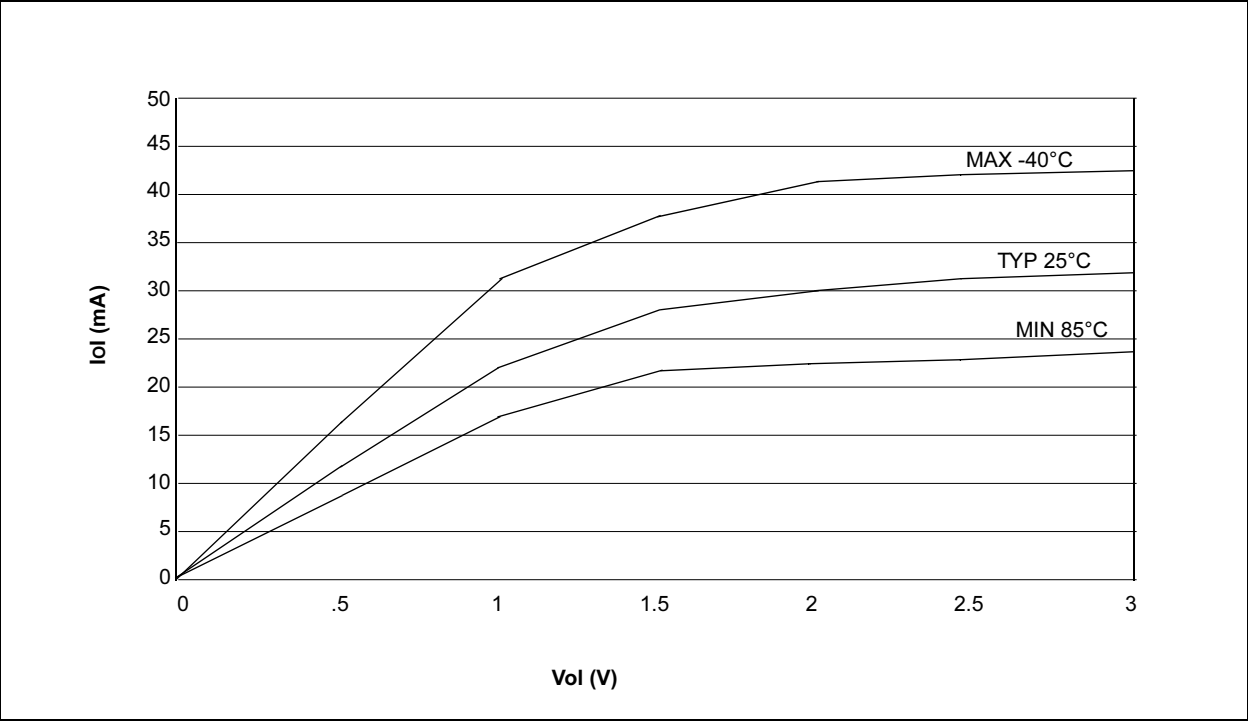
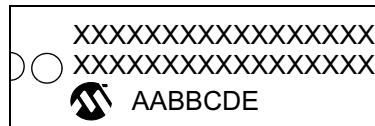


FIGURE 13-4: I_{OL} vs. V_{OL}, V_{DD} = 3.0V

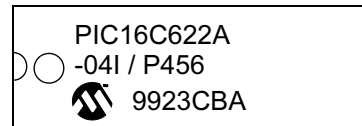


14.1 Package Marking Information

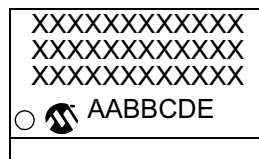
18-Lead PDIP



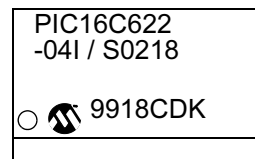
Example



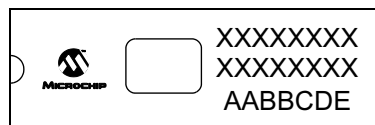
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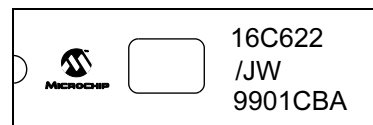
Example



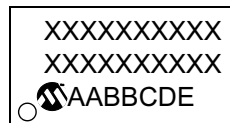
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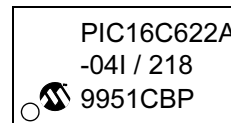
Example



20-Lead SSOP



Example



Legend: XX...X Customer specific information*
 Y Year code (last digit of calendar year)
 YY Year code (last 2 digits of calendar year)
 WW Week code (week of January 1 is week '01')
 NNN Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

* Standard PICmicro device marking consists of Microchip part number, year code, week code, and traceability code. For PICmicro device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

PIC16C62X

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