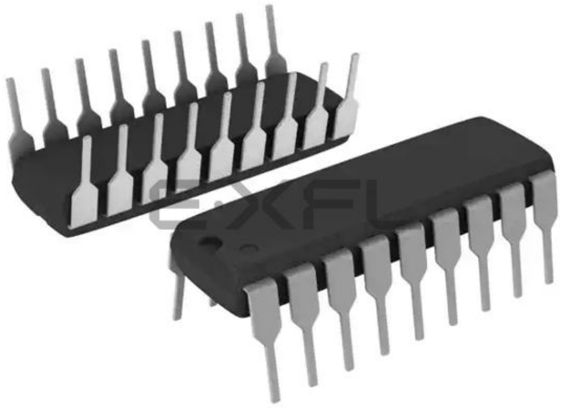

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	13
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	96 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	18-DIP (0.300", 7.62mm)
Supplier Device Package	18-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lc621a-04i-p

Device Differences

Device	Voltage Range	Oscillator	Process Technology (Microns)
PIC16C620(3)	2.5 - 6.0	See **Note 1**	0.9
PIC16C621(3)	2.5 - 6.0	See **Note 1**	0.9
PIC16C622(3)	2.5 - 6.0	See **Note 1**	0.9
PIC16C620A(4)	2.7 - 5.5	See **Note 1**	0.7
PIC16CR620A(2)	2.5 - 5.5	See **Note 1**	0.7
PIC16C621A(4)	2.7 - 5.5	See **Note 1**	0.7
PIC16C622A(4)	2.7 - 5.5	See **Note 1**	0.7

Note 1: If you change from this device to another device, please verify oscillator characteristics in your application.

2: For ROM parts, operation from 2.5V - 3.0V will require the PIC16LCR62X parts.

3: For OTP parts, operation from 2.5V - 3.0V will require the PIC16LC62X parts.

4: For OTP parts, operations from 2.7V - 3.0V will require the PIC16LC62XA parts.

1.0 GENERAL DESCRIPTION

The PIC16C62X devices are 18 and 20-Pin ROM/EPROM-based members of the versatile PICmicro® family of low cost, high performance, CMOS, fully-static, 8-bit microcontrollers.

All PICmicro microcontrollers employ an advanced RISC architecture. The PIC16C62X devices have enhanced core features, eight-level deep stack, and multiple internal and external interrupt sources. The separate instruction and data buses of the Harvard architecture allow a 14-bit wide instruction word with the separate 8-bit wide data. The two-stage instruction pipeline allows all instructions to execute in a single cycle, except for program branches (which require two cycles). A total of 35 instructions (reduced instruction set) are available. Additionally, a large register set gives some of the architectural innovations used to achieve a very high performance.

PIC16C62X microcontrollers typically achieve a 2:1 code compression and a 4:1 speed improvement over other 8-bit microcontrollers in their class.

The PIC16C620A, PIC16C621A and PIC16CR620A have 96 bytes of RAM. The PIC16C622(A) has 128 bytes of RAM. Each device has 13 I/O pins and an 8-bit timer/counter with an 8-bit programmable prescaler. In addition, the PIC16C62X adds two analog comparators with a programmable on-chip voltage reference module. The comparator module is ideally suited for applications requiring a low cost analog interface (e.g., battery chargers, threshold detectors, white goods controllers, etc).

PIC16C62X devices have special features to reduce external components, thus reducing system cost, enhancing system reliability and reducing power consumption. There are four oscillator options, of which the single pin RC oscillator provides a low cost solution, the LP oscillator minimizes power consumption, XT is a standard crystal, and the HS is for High Speed crystals. The SLEEP (Power-down) mode offers power savings. The user can wake-up the chip from SLEEP through several external and internal interrupts and RESET.

A highly reliable Watchdog Timer with its own on-chip RC oscillator provides protection against software lock- up.

A UV-erasable CERDIP-packaged version is ideal for code development while the cost effective One-Time-Programmable (OTP) version is suitable for production in any volume.

Table 1-1 shows the features of the PIC16C62X mid-range microcontroller families.

A simplified block diagram of the PIC16C62X is shown in Figure 3-1.

The PIC16C62X series fits perfectly in applications ranging from battery chargers to low power remote sensors. The EPROM technology makes customization of application programs (detection levels, pulse generation, timers, etc.) extremely fast and convenient. The small footprint packages make this microcontroller series perfect for all applications with space limitations. Low cost, low power, high performance, ease of use and I/O flexibility make the PIC16C62X very versatile.

1.1 Family and Upward Compatibility

Those users familiar with the PIC16C5X family of microcontrollers will realize that this is an enhanced version of the PIC16C5X architecture. Please refer to Appendix A for a detailed list of enhancements. Code written for the PIC16C5X can be easily ported to PIC16C62X family of devices (Appendix B). The PIC16C62X family fills the niche for users wanting to migrate up from the PIC16C5X family and not needing various peripheral features of other members of the PIC16XX mid-range microcontroller family.

1.2 Development Support

The PIC16C62X family is supported by a full-featured macro assembler, a software simulator, an in-circuit emulator, a low cost development programmer and a full-featured programmer. Third Party “C” compilers are also available.

NOTES:

4.2 Data Memory Organization

The data memory (Figure 4-4, Figure 4-5, Figure 4-6 and Figure 4-7) is partitioned into two banks, which contain the General Purpose Registers and the Special Function Registers. Bank 0 is selected when the RP0 bit is cleared. Bank 1 is selected when the RP0 bit (STATUS <5>) is set. The Special Function Registers are located in the first 32 locations of each bank. Register locations 20-7Fh (Bank0) on the PIC16C620A/CR620A/621A and 20-7Fh (Bank0) and A0-BFh (Bank1) on the PIC16C622 and PIC16C622A are General Purpose Registers implemented as static RAM. Some Special Purpose Registers are mapped in Bank 1.

Addresses F0h-FFh of bank1 are implemented as common ram and mapped back to addresses 70h-7Fh in bank0 on the PIC16C620A/621A/622A/CR620A.

4.2.1 GENERAL PURPOSE REGISTER FILE

The register file is organized as 80 x 8 in the PIC16C620/621, 96 x 8 in the PIC16C620A/621A/CR620A and 128 x 8 in the PIC16C622(A). Each is accessed either directly or indirectly through the File Select Register FSR (Section 4.4).

4.2.2.4 PIE1 Register

This register contains the individual enable bit for the comparator interrupt.

REGISTER 4-4: PIE1 REGISTER (ADDRESS 8CH)

U-0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0
—	CMIE	—	—	—	—	—	—
bit 7							bit 0

bit 7 **Unimplemented:** Read as '0'

bit 6 **CMIE**: Comparator Interrupt Enable bit
1 = Enables the Comparator interrupt
0 = Disables the Comparator interrupt

bit 5-0 **Unimplemented**: Read as '0'

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
- n = Value at POR	’1’ = Bit is set	’0’ = Bit is cleared	x = Bit is unknown

4.2.2.5 PIR1 Register

This register contains the individual flag bit for the comparator interrupt.

> **Note:** Interrupt flag bits get set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 4-5: PIR1 REGISTER (ADDRESS 0CH)

U-0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0
—	CMIF	—	—	—	—	—	—
bit 7							bit 0

bit 7 **Unimplemented:** Read as '0'

bit 6 **CMIF**: Comparator Interrupt Flag bit
1 = Comparator input has changed
0 = Comparator input has not changed

bit 5-0 **Unimplemented**: Read as '0'

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
- n = Value at POR	’1’ = Bit is set	’0’ = Bit is cleared	x = Bit is unknown

FIGURE 5-3: BLOCK DIAGRAM OF RA3 PIN

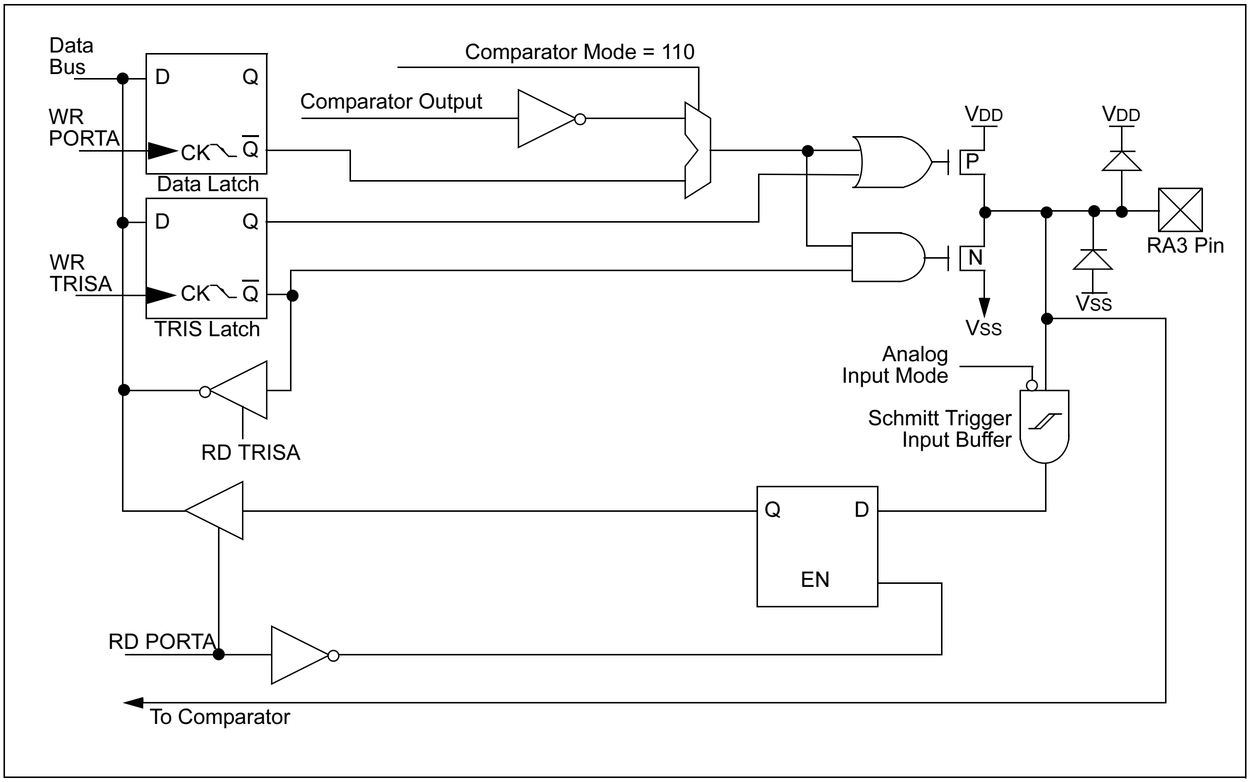
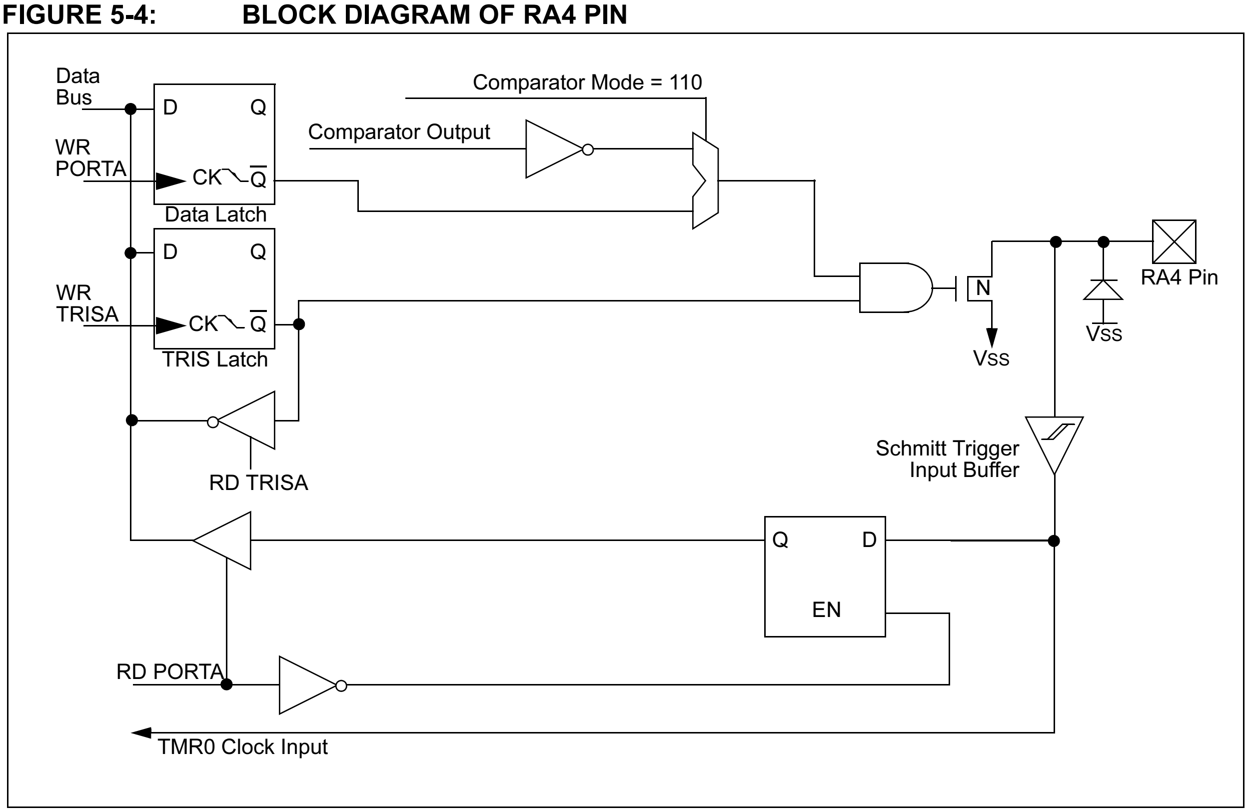


FIGURE 5-4: BLOCK DIAGRAM OF RA4 PIN



5.2 PORTB and TRISB Registers

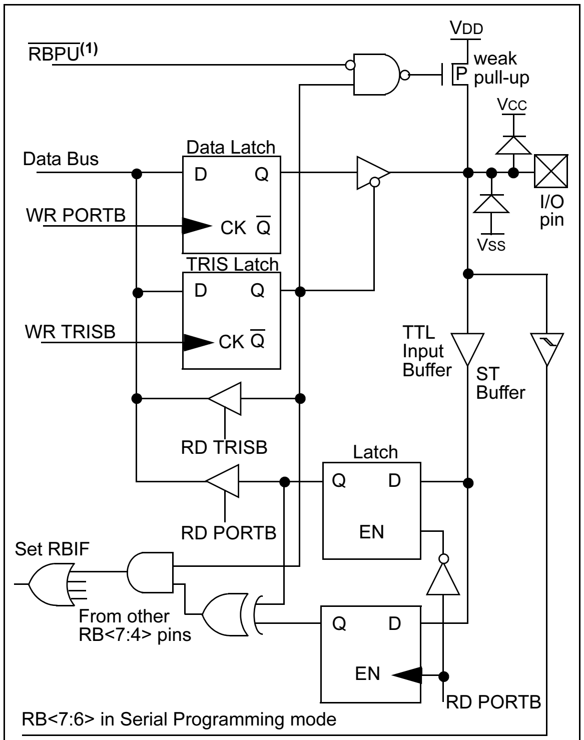
PORTB is an 8-bit wide, bi-directional port. The corresponding data direction register is TRISB. A '1' in the TRISB register puts the corresponding output driver in a High Impedance mode. A '0' in the TRISB register puts the contents of the output latch on the selected pin(s).

Reading PORTB register reads the status of the pins, whereas writing to it will write to the port latch. All write operations are read-modify-write operations. So a write to a port implies that the port pins are first read, then this value is modified and written to the port data latch.

Each of the PORTB pins has a weak internal pull-up (≈200 μA typical). A single control bit can turn on all the pull-ups. This is done by clearing the $\overline{\text{RBPU}}$ (OPTION<7>) bit. The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on Power-on Reset.

Four of PORTB's pins, RB<7:4>, have an interrupt on change feature. Only pins configured as inputs can cause this interrupt to occur (e.g., any RB<7:4> pin configured as an output is excluded from the interrupt on change comparison). The input pins (of RB<7:4>) are compared with the old value latched on the last read of PORTB. The "mismatch" outputs of RB<7:4> are OR'ed together to generate the RBIF interrupt (flag latched in INTCON<0>).

FIGURE 5-5: BLOCK DIAGRAM OF RB<7:4> PINS



Note 1: TRISB = 1 enables weak pull-up if $\overline{\text{RBPU}}$ = '0' (OPTION<7>).

This interrupt can wake the device from SLEEP. The user, in the interrupt service routine, can clear the interrupt in the following manner:

a) Any read or write of PORTB. This will end the mismatch condition.

b) Clear flag bit RBIF.

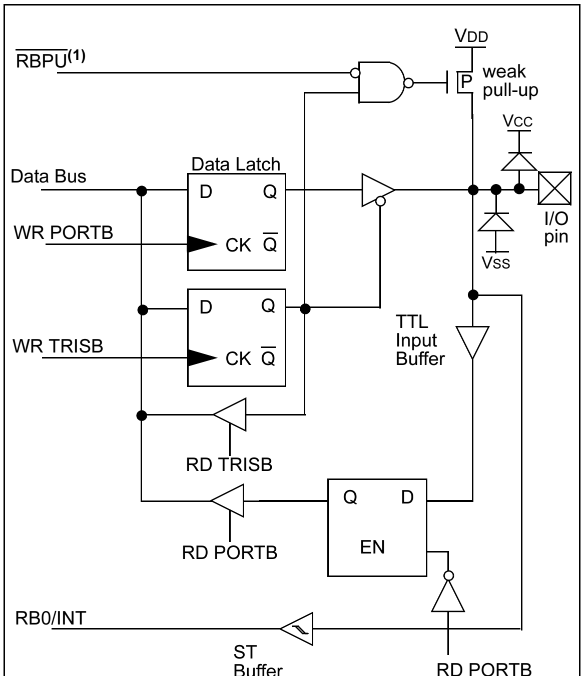
A mismatch condition will continue to set flag bit RBIF. Reading PORTB will end the mismatch condition and allow flag bit RBIF to be cleared.

This interrupt on mismatch feature, together with software configurable pull-ups on these four pins allow easy interface to a key pad and make it possible for wake-up on key-depression. (See AN552, "Implementing Wake-Up on Key Strokes.)

Note:	If a change on the I/O pin should occur when the read operation is being executed (start of the Q2 cycle), then the RBIF interrupt flag may not get set.

The interrupt-on-change feature is recommended for wake-up on key depression operation and operations where PORTB is only used for the interrupt on change feature. Polling of PORTB is not recommended while using the interrupt-on-change feature.

FIGURE 5-6: BLOCK DIAGRAM OF RB<3:0> PINS



Note 1: TRISB = 1 enables weak pull-up if $\overline{\text{RBPU}}$ = '0' (OPTION<7>).

6.3.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control (i.e., it can be changed “on-the-fly” during program execution). To avoid an unintended device RESET, the following instruction sequence (Example 6-1) must be executed when changing the prescaler assignment from Timer0 to WDT.)

EXAMPLE 6-1: CHANGING PRESCALER (TIMER0→WDT)

```
 1.BCF      STATUS, RP0    ;Skip if already in
                           ;Bank 0
 2.CLRWDT                  ;Clear WDT
 3.CLRF     TMR0           ;Clear TMR0 & Prescaler
 4.BSF      STATUS, RP0    ;Bank 1
 5.MOVLW    '00101111'b;   ;These 3 lines (5, 6, 7)
 6.MOVWF    OPTION         ;are required only if
                           ;desired PS<2:0> are
 7.CLRWDT                  ;000 or 001
 8.MOVLW    '00101xxx'b    ;Set Postscaler to
 9.MOVWF    OPTION         ;desired WDT rate
10.BCF      STATUS, RP0    ;Return to Bank 0
```

To change prescaler from the WDT to the TMR0 module, use the sequence shown in Example 6-2. This precaution must be taken even if the WDT is disabled.

EXAMPLE 6-2: CHANGING PRESCALER (WDT→TIMER0)

```
 CLRWDT                        ;Clear WDT and
                               ;prescaler
BSF        STATUS, RP0
MOVLW      b'xxxx0xxx'         ;Select TMR0, new
                               ;prescale value and
                               ;clock source
MOVWF      OPTION_REG
BCF       STATUS, RP0
```

TABLE 6-1: REGISTERS ASSOCIATED WITH TIMER0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Value on All Other RESETS
01h	TMR0	Timer0 module register								xxxx xxxx	uuuu uuuu
0Bh/8Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
81h	OPTION	$\overline{\text{RBPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
85h	TRISA	—	—	—	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	---1 1111	---1 1111

Legend: — = Unimplemented locations, read as ‘0’, u = unchanged, x = unknown

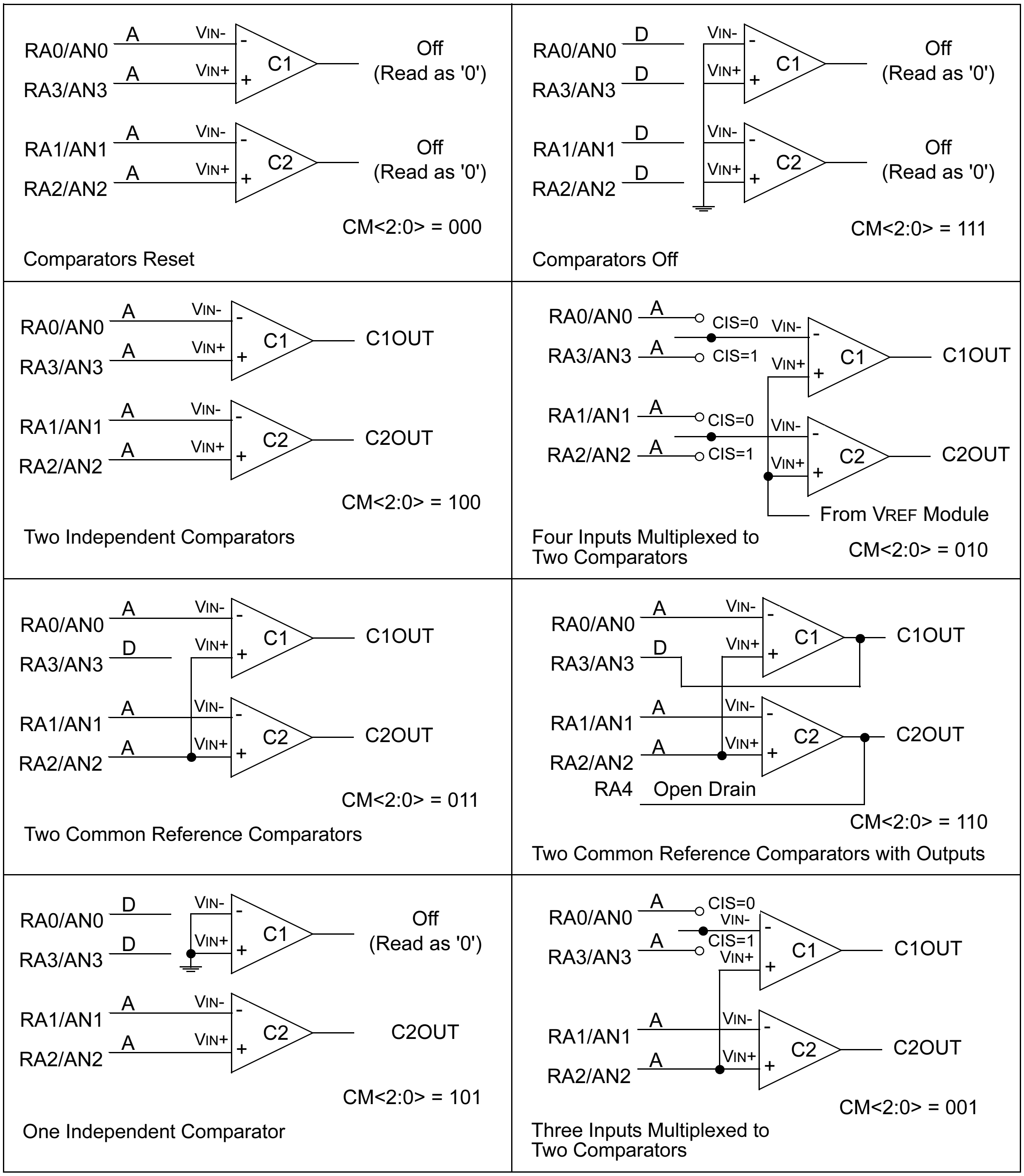
Note: Shaded bits are not used by TMR0 module.

7.1 Comparator Configuration

There are eight modes of operation for the comparators. The CMCON register is used to select the mode. Figure 7-1 shows the eight possible modes. The TRISA register controls the data direction of the comparator pins for each mode. If the Comparator mode is changed, the comparator output level may not be valid for the specified mode change delay shown in Table 12-2.

Note:	Comparator interrupts should be disabled during a Comparator mode change otherwise a false interrupt may occur.

FIGURE 7-1: COMPARATOR I/O OPERATING MODES



A = Analog Input, Port Reads Zeros Always
D = Digital Input
CIS = CMCON<3>, Comparator Input Switch

8.0 VOLTAGE REFERENCE MODULE

The Voltage Reference is a 16-tap resistor ladder network that provides a selectable voltage reference. The resistor ladder is segmented to provide two ranges of VREF values and has a power-down function to conserve power when the reference is not being used. The VRCON register controls the operation of the reference as shown in Register 8-1. The block diagram is given in Figure 8-1.

8.1 Configuring the Voltage Reference

The Voltage Reference can output 16 distinct voltage levels for each range. The equations used to calculate the output of the Voltage Reference are as follows:

if VRR = 1: VREF = (VR<3:0>/24) x VDD

if VRR = 0: VREF = (VDD x 1/4) + (VR<3:0>/32) x VDD

The setting time of the Voltage Reference must be considered when changing the VREF output (Table 12-1). Example 8-1 shows an example of how to configure the Voltage Reference for an output voltage of 1.25V with VDD = 5.0V.

REGISTER 8-1: VRCON REGISTER(ADDRESS 9Fh)

R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
VREN	VROE	VRR	—	VR3	VR2	VR1	VR0
bit 7							bit 0

bit 7 **VREN:** VREF Enable
1 = VREF circuit powered on
0 = VREF circuit powered down, no IDD drain

bit 6 **VROE:** VREF Output Enable
1 = VREF is output on RA2 pin
0 = VREF is disconnected from RA2 pin

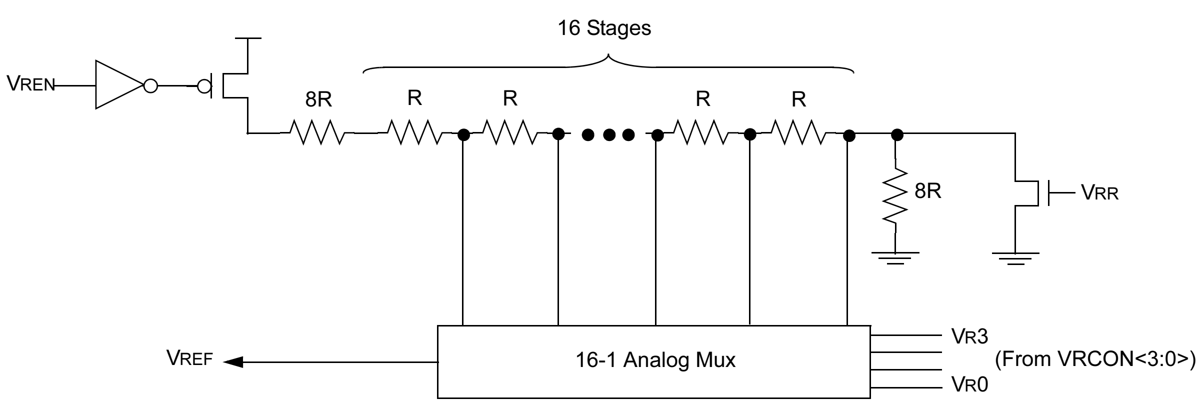
bit 5 **VRR:** VREF Range selection
1 = Low Range
0 = High Range

bit 4 **Unimplemented:** Read as '0'

bit 3-0 **VR<3:0>**: VREF value selection $0 \leq$ VR [3:0] ≤ 15
when VRR = 1: VREF = (VR<3:0>/ 24) * VDD
when VRR = 0: VREF = 1/4 * VDD + (VR<3:0>/ 32) * VDD

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
- n = Value at POR	’1’ = Bit is set	’0’ = Bit is cleared	x = Bit is unknown

FIGURE 8-1: VOLTAGE REFERENCE BLOCK DIAGRAM



Note: R is defined in Table 12-2.

9.4.5 TIME-OUT SEQUENCE

On power-up the time-out sequence is as follows: First PWRT time-out is invoked after POR has expired. Then OST is activated. The total time-out will vary based on oscillator configuration and PWRTE bit status. For example, in RC mode with PWRTE bit erased (PWRT disabled), there will be no time-out at all. Figure 9-8, Figure 9-9 and Figure 9-10 depict time-out sequences.

Since the time-outs occur from the POR pulse, if MCLR is kept low long enough, the time-outs will expire. Then bringing MCLR high will begin execution immediately (see Figure 9-9). This is useful for testing purposes or to synchronize more than one PIC16C62X device operating in parallel.

Table 9-4 shows the RESET conditions for some special registers, while Table 9-5 shows the RESET conditions for all the registers.

9.4.6 POWER CONTROL (PCON)/ STATUS REGISTER

The power control/STATUS register, PCON (address 8Eh), has two bits.

Bit0 is BOR (Brown-out). BOR is unknown on Power-on Reset. It must then be set by the user and checked on subsequent RESETS to see if BOR = 0, indicating that a brown-out has occurred. The BOR STATUS bit is a don't care and is not necessarily predictable if the brown-out circuit is disabled (by setting BODEN bit = 0 in the Configuration word).

Bit1 is POR (Power-on Reset). It is a '0' on Power-on Reset and unaffected otherwise. The user must write a '1' to this bit following a Power-on Reset. On a subsequent RESET, if POR is '0', it will indicate that a Power-on Reset must have occurred (VDD may have gone too low).

TABLE 9-1: TIME-OUT IN VARIOUS SITUATIONS

Oscillator Configuration	Power-up		Brown-out Reset	Wake-up from SLEEP
	PWRTE = 0	PWRTE = 1		
XT, HS, LP	72 ms + 1024 TOSC	1024 TOSC	72 ms + 1024 TOSC	1024 TOSC
RC	72 ms	—	72 ms	—

TABLE 9-2: STATUS/PCON BITS AND THEIR SIGNIFICANCE

POR	BOR	TO	PD	
0	X	1	1	Power-on Reset
0	X	0	X	Illegal, TO is set on POR
0	X	X	0	Illegal, PD is set on POR
1	0	X	X	Brown-out Reset
1	1	0	u	WDT Reset
1	1	0	0	WDT Wake-up
1	1	u	u	MCLR Reset during normal operation
1	1	1	0	MCLR Reset during SLEEP

Legend: u = unchanged, x = unknown

TABLE 9-3: SUMMARY OF REGISTERS ASSOCIATED WITH BROWN-OUT

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR Reset	Value on all other RESETS(1)
83h	STATUS				TO	PD				0001 1xxx	000q quuu
8Eh	PCON	—	—	—	—	—	—	POR	BOR	---- --0x	---- --uq

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0', q = value depends on condition.

Note 1: Other (non Power-up) Resets include MCLR Reset, Brown-out Reset and Watchdog Timer Reset during normal operation.

10.0 INSTRUCTION SET SUMMARY

Each PIC16C62X instruction is a 14-bit word divided into an OPCODE which specifies the instruction type and one or more operands which further specify the operation of the instruction. The PIC16C62X instruction set summary in Table 10-2 lists **byte-oriented**, **bit-oriented,** and **literal and control** operations. Table 10-1 shows the opcode field descriptions.

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator specifies which file register is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is zero, the result is placed in the W register. If 'd' is one, the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator which selects the number of the bit affected by the operation, while 'f' represents the number of the file in which the bit is located.

For **literal and control** operations, 'k' represents an eight or eleven bit constant or literal value.

TABLE 10-1: OPCODE FIELD DESCRIPTIONS

Field	Description
`f`	Register file address (0x00 to 0x7F)
`W`	Working register (accumulator)
`b`	Bit address within an 8-bit file register
`k`	Literal field, constant data or label
`x`	Don't care location (= 0 or 1) The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
`d`	Destination select; d = 0: store result in W, d = 1: store result in file register f. Default is d = 1
`label`	Label name
`TOS`	Top of Stack
`PC`	Program Counter
`PCLATH`	Program Counter High Latch
`GIE`	Global Interrupt Enable bit
`WDT`	Watchdog Timer/Counter
`TO`	Time-out bit
`PD`	Power-down bit
`dest`	Destination either the W register or the specified register file location
[ ]	Options
( )	Contents
→	Assigned to
< >	Register bit field
∈	In the set of
italics	User defined term (font is courier)

The instruction set is highly orthogonal and is grouped into three basic categories:

- **Byte-oriented** operations
- **Bit-oriented** operations
- **Literal and control** operations

All instructions are executed within one single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles with the second cycle executed as a `NOP`. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 μs. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time is 2 μs.

Table 10-1 lists the instructions recognized by the MPASM™ assembler.

Figure 10-1 shows the three general formats that the instructions can have.

> **Note:** To maintain upward compatibility with future PICmicro® products, do not use the `OPTION` and `TRIS` instructions.

All examples use the following format to represent a hexadecimal number:

0xhh

where h signifies a hexadecimal digit.

FIGURE 10-1: GENERAL FORMAT FOR INSTRUCTIONS

Byte-oriented file register operations

13 — 8	7	6 — 0
OPCODE	d	f (FILE #)

d = 0 for destination W
d = 1 for destination f
f = 7-bit file register address

Bit-oriented file register operations

13 — 10	9 — 7	6 — 0
OPCODE	b (BIT #)	f (FILE #)

b = 3-bit bit address
f = 7-bit file register address

Literal and control operations

General

13 — 8	7 — 0
OPCODE	k (literal)

k = 8-bit immediate value

`CALL` and `GOTO` instructions only

13 — 11	10 — 0
OPCODE	k (literal)

k = 11-bit immediate value

RETFIE — Return from Interrupt

Syntax:	[*label*] RETFIE
Operands:	None
Operation:	TOS → PC, 1 → GIE
Status Affected:	None
Encoding:	`00` `0000` `0000` `1001`
Description:	Return from Interrupt. Stack is POPed and Top of Stack (TOS) is loaded in the PC. Interrupts are enabled by setting Global Interrupt Enable bit, GIE (INTCON<7>). This is a two-cycle instruction.
Words:	1
Cycles:	2
Example	`RETFIE`

After Interrupt
PC = TOS
GIE = 1

RETLW — Return with Literal in W

Syntax:	[*label*] RETLW k
Operands:	$0 \le k \le 255$
Operation:	k → (W); TOS → PC
Status Affected:	None
Encoding:	`11` `01xx` `kkkk` `kkkk`
Description:	The W register is loaded with the eight bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a two-cycle instruction.
Words:	1
Cycles:	2

Example

```
        CALL TABLE;W contains table
                  ;offset value
TABLE   •         ;W now has table value
        •
        •
        ADDWF PC   ;W = offset
        RETLW k1   ;Begin table
        RETLW k2   ;
        •
        •
        •
        RETLW kn   ; End of table
```

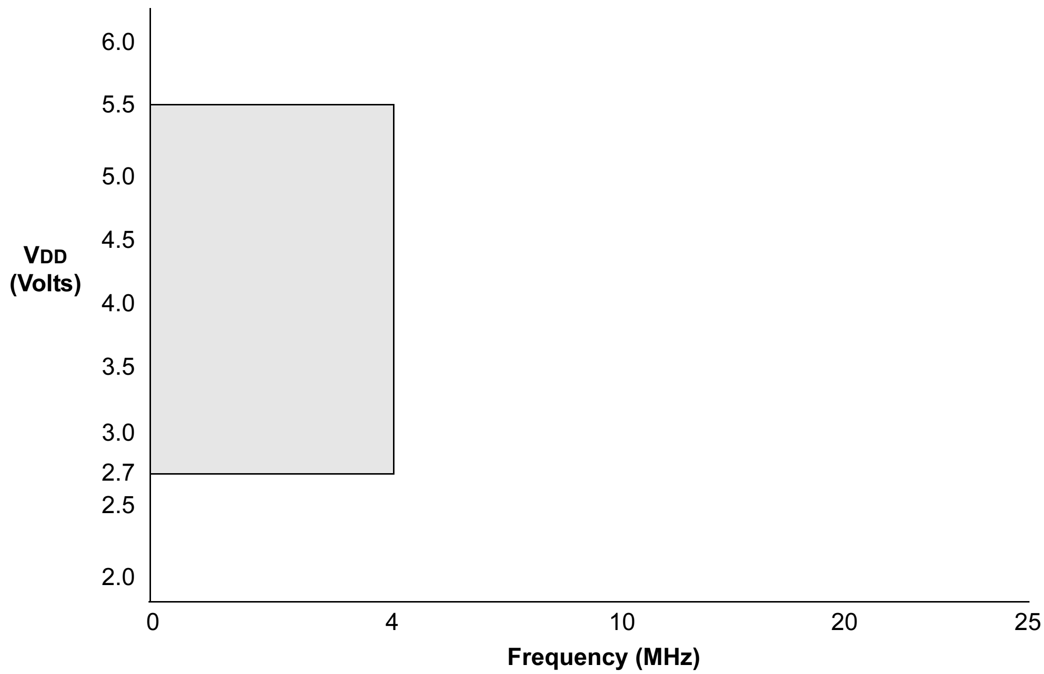
Before Instruction
W = 0x07
After Instruction
W = value of k8

RETURN — Return from Subroutine

Syntax:	[*label*] RETURN
Operands:	None
Operation:	TOS → PC
Status Affected:	None
Encoding:	`00` `0000` `0000` `1000`
Description:	Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a two-cycle instruction.
Words:	1
Cycles:	2
Example	`RETURN`

After Interrupt
PC = TOS

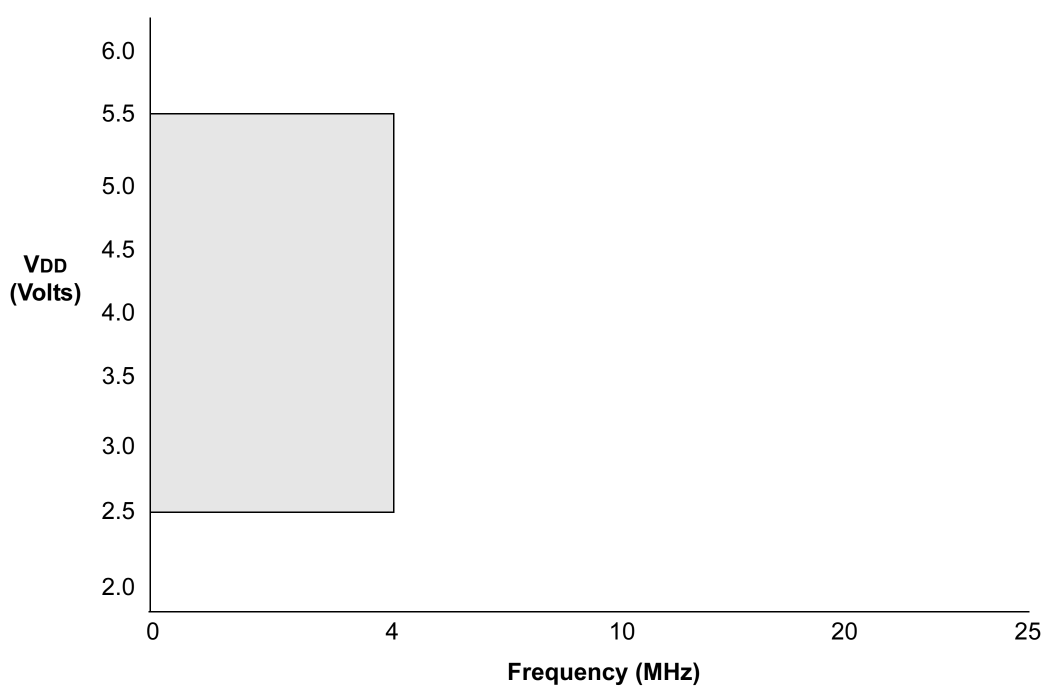
FIGURE 12-5: PIC16LC620A/LC621A/LC622A VOLTAGE-FREQUENCY GRAPH, -40°C ≤ TA ≤ 0°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

2: The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.

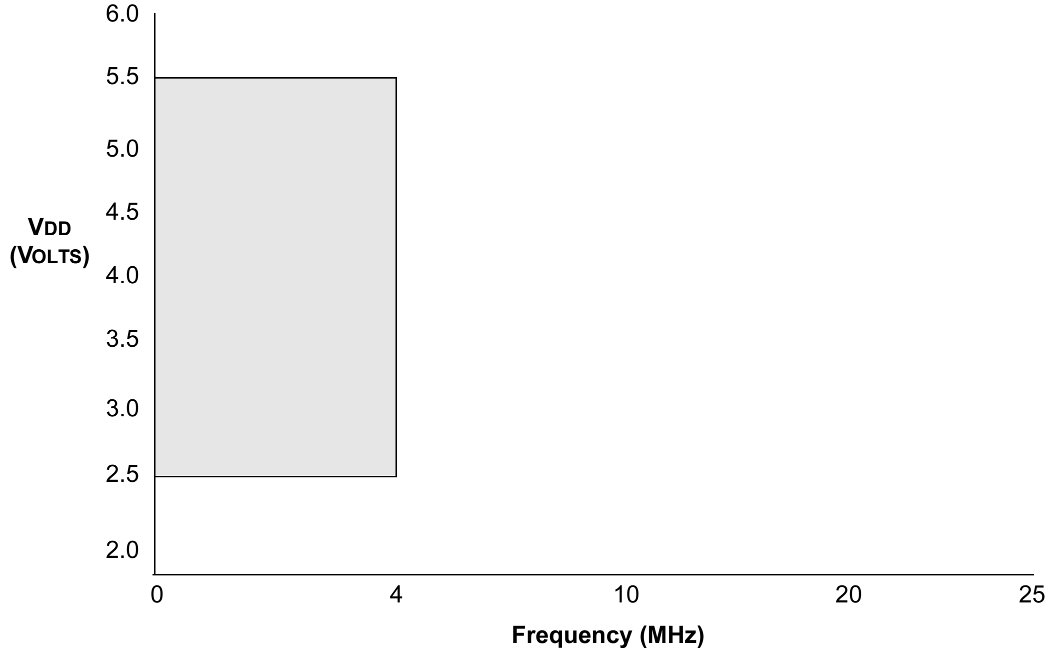
FIGURE 12-6: PIC16LC620A/LC621A/LC622A VOLTAGE-FREQUENCY GRAPH, 0°C ≤ TA ≤ +125°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

2: The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.

FIGURE 12-9: PIC16LCR62XA VOLTAGE-FREQUENCY GRAPH, -40°C ≤ TA ≤ +125°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

2: The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.

12.2 DC Characteristics: PIC16C62XA-04 (Commercial, Industrial, Extended) PIC16C62XA-20 (Commercial, Industrial, Extended) PIC16LC62XA-04 (Commercial, Industrial, Extended)

PIC16C62XA			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial and -40°C ≤ TA ≤ +125°C for extended				
PIC16LC62XA			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial and -40°C ≤ TA ≤ +125°C for extended				
Param. No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D001	VDD	Supply Voltage	3.0	—	5.5	V	See Figures 12-1, 12-2, 12-3, 12-4, and 12-5
D001	VDD	Supply Voltage	2.5	—	5.5	V	See Figures 12-1, 12-2, 12-3, 12-4, and 12-5
D002	VDR	RAM Data Retention Voltage(1)	—	1.5*	—	V	Device in SLEEP mode
D002	VDR	RAM Data Retention Voltage(1)	—	1.5*	—	V	Device in SLEEP mode
D003	VPOR	VDD start voltage to ensure Power-on Reset	—	VSS	—	V	See section on Power-on Reset for details
D003	VPOR	VDD start voltage to ensure Power-on Reset	—	VSS	—	V	See section on Power-on Reset for details
D004	SVDD	VDD rise rate to ensure Power-on Reset	0.05*	—	—	V/ms	See section on Power-on Reset for details
D004	SVDD	VDD rise rate to ensure Power-on Reset	0.05*	—	—	V/ms	See section on Power-on Reset for details
D005	VBOR	Brown-out Detect Voltage	3.7	4.0	4.35	V	BOREN configuration bit is cleared
D005	VBOR	Brown-out Detect Voltage	3.7	4.0	4.35	V	BOREN configuration bit is cleared

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in Active Operation mode are:
OSC1 = external square wave, from rail to rail; all I/O pins tri-stated, pulled to VDD,
$\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or VSS.

4: For RC osc configuration, current through REXT is not included. The current through the resistor can be estimated by the formula: Ir = VDD/2REXT (mA) with REXT in kΩ.

5: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

6: Commercial temperature range only.

12.6 DC Characteristics: PIC16C620A/C621A/C622A-40(3) (Commercial) PIC16CR620A-40(3) (Commercial)

DC CHARACTERISTICS Power Supply Pins			Standard Operating Conditions (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for commercial			
Characteristic	Sym	Min	Typ(1)	Max	Units	Conditions
Supply Voltage	VDD	4.5	—	5.5	V	HS Option from 20 - 40 MHz
Supply Current(2)	IDD	— —	5.5 7.7	11.5 16	mA mA	FOSC = 40 MHz, VDD = 4.5V, HS mode FOSC = 40 MHz, VDD = 5.5V, HS mode
HS Oscillator Operating Frequency	FOSC	20	—	40	MHz	OSC1 pin is externally driven, OSC2 pin not connected
Input Low Voltage OSC1	VIL	VSS	—	0.2VDD	V	HS mode, OSC1 externally driven
Input High Voltage OSC1	VIH	0.8VDD	—	VDD	V	HS mode, OSC1 externally driven

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in Active Operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VSS,
T0CKI = VDD, $\overline{\text{MCLR}}$ = VDD; WDT disabled, HS mode with OSC2 not connected.

3: For device operation between DC and 20 MHz. See Table 12-1 and Table 12-2.

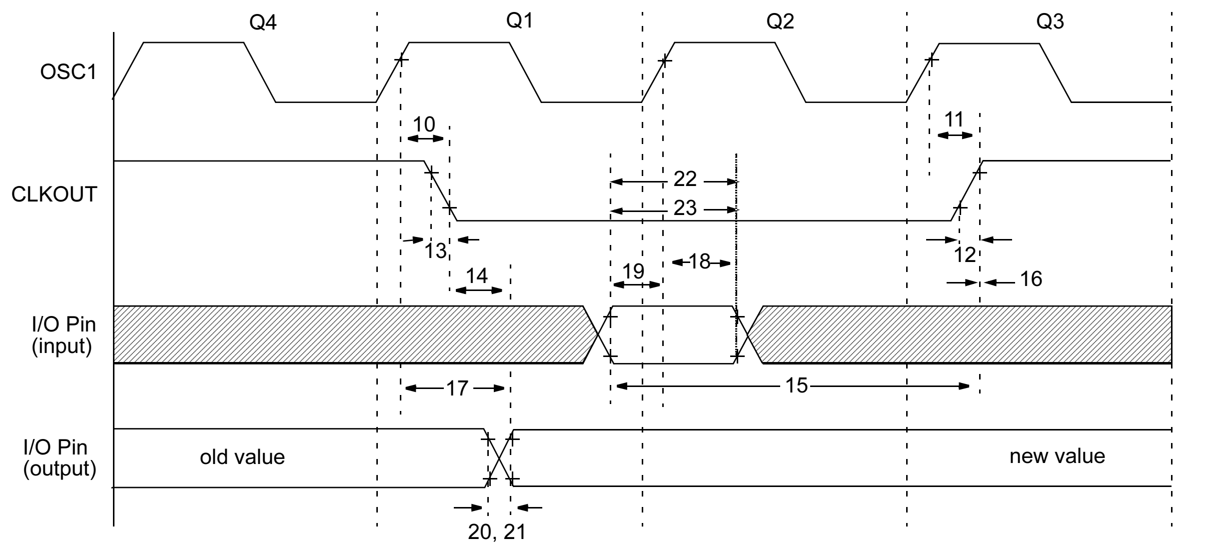
12.7 AC Characteristics: PIC16C620A/C621A/C622A-40(2) (Commercial) PIC16CR620A-40(2) (Commercial)

AC CHARACTERISTICS All Pins Except Power Supply Pins			Standard Operating Conditions (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for commercial			
Characteristic	Sym	Min	Typ(1)	Max	Units	Conditions
External CLKIN Frequency	FOSC	20	—	40	MHz	HS mode, OSC1 externally driven
External CLKIN Period	TOSC	25	—	50	ns	HS mode (40), OSC1 externally driven
Clock in (OSC1) Low or High Time	TOSL, TOSH	6	—	—	ns	HS mode, OSC1 externally driven
Clock in (OSC1) Rise or Fall Time	TOSR, TOSF	—	—	6.5	ns	HS mode, OSC1 externally driven
OSC1↑ (Q1 cycle) to Port out valid	TOSH2IOV	—	—	100	ns	—
OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TOSH2IOI	50	—	—	ns	—

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: For device operation between DC and 20 MHz. See Table 12-1 and Table 12-2.

FIGURE 12-13: CLKOUT AND I/O TIMING



Note: All tests must be done with specified capacitance loads (Figure 12-11) 50 pF on I/O pins and CLKOUT.

13.0 DEVICE CHARACTERIZATION INFORMATION

The graphs and tables provided in this section are for design guidance and are not tested. In some graphs or tables, the data presented is outside specified operating range (e.g., outside specified VDD range). This is for information only and devices will operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. "Typical" represents the mean of the distribution, while "max" or "min" represents (mean + 3σ) and (mean – 3σ) respectively, where σ is standard deviation.

FIGURE 13-1: IDD VS. FREQUENCY (XT MODE, VDD = 5.5V)

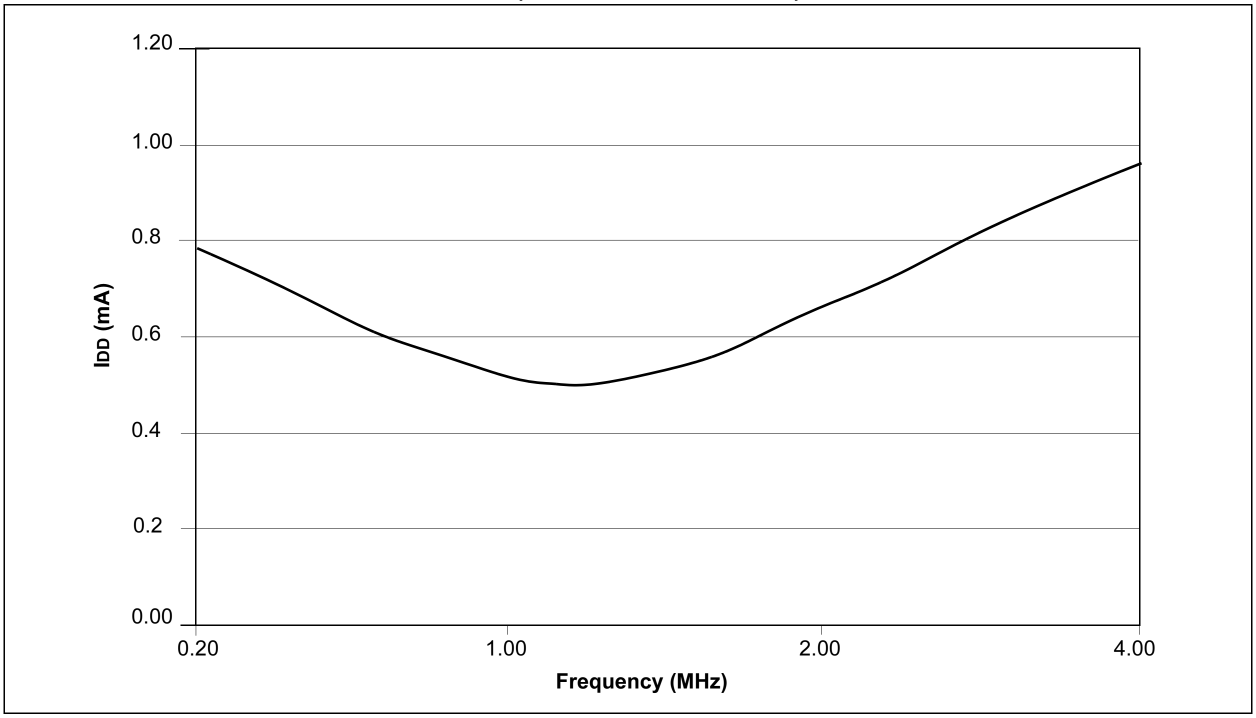
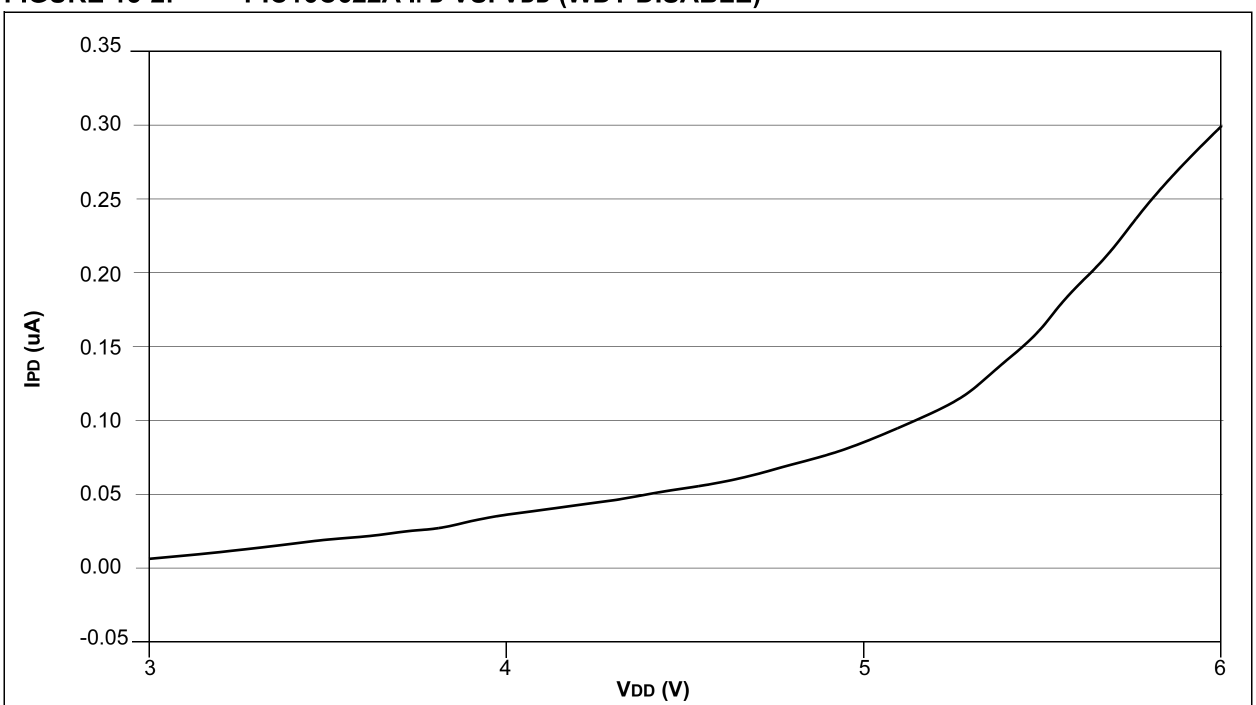


FIGURE 13-2: PIC16C622A IPD VS. VDD (WDT DISABLE)



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