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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	13
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	80 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 6V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lc621t-04-ss

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Device Differences

Device	Voltage Range	Oscillator	Process Technology (Microns)
PIC16C620 ⁽³⁾	2.5 - 6.0	See Note 1	0.9
PIC16C621 ⁽³⁾	2.5 - 6.0	See Note 1	0.9
PIC16C622 ⁽³⁾	2.5 - 6.0	See Note 1	0.9
PIC16C620A ⁽⁴⁾	2.7 - 5.5	See Note 1	0.7
PIC16CR620A ⁽²⁾	2.5 - 5.5	See Note 1	0.7
PIC16C621A ⁽⁴⁾	2.7 - 5.5	See Note 1	0.7
PIC16C622A ⁽⁴⁾	2.7 - 5.5	See Note 1	0.7

Note 1: If you change from this device to another device, please verify oscillator characteristics in your application.

2: For ROM parts, operation from 2.5V - 3.0V will require the PIC16LCR62X parts.

3: For OTP parts, operation from 2.5V - 3.0V will require the PIC16LC62X parts.

4: For OTP parts, operations from 2.7V - 3.0V will require the PIC16LC62XA parts.

NOTES:

4.2.2.6 PCON Register

The PCON register contains flag bits to differentiate between a Power-on Reset, an external MCLR Reset, WDT Reset or a Brown-out Reset.

Note:	BOR is unknown on Power-on Reset. It
	must then be set by the user and checked
	on subsequent RESETS to see if BOR is
	cleared, indicating a brown-out has
	occurred. The $\overline{\text{BOR}}$ STATUS bit is a "don't
	care" and is not necessarily predictable if
	the brown-out circuit is disabled (by
	programming BODEN bit in the
	Configuration word).

REGISTER 4-6: PCON REGISTER (ADDRESS 8Eh)

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	POR	BOR
bit 7							bit 0

bit 7-2 Unimplemented: Read as '0'

bit 1 **POR**: Power-on Reset STATUS bit

- 1 = No Power-on Reset occurred
- 0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)

bit 0 **BOR**: Brown-out Reset STATUS bit

1 = No Brown-out Reset occurred

0 = A Brown-out Reset occurred (must be set in software after a Brown-out Reset occurs)

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented	bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown









6.3 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module, or as a postscaler for the Watchdog Timer, respectively (Figure 6-6). For simplicity, this counter is being referred to as "prescaler" throughout this data sheet. Note that there is only one prescaler available which is mutually exclusive between the Timer0 module and the Watchdog Timer. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the Watchdog Timer and vice-versa.

The PSA and PS<2:0> bits (OPTION<3:0>) determine the prescaler assignment and prescale ratio.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., CLRF 1, MOVWF 1, BSF 1, x....etc.) will clear the prescaler. When assigned to WDT, a CLRWDT instruction will clear the prescaler along with the Watchdog Timer. The prescaler is not readable or writable.



FIGURE 6-6: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER

NOTES:

9.2 Oscillator Configurations

9.2.1 OSCILLATOR TYPES

The PIC16C62X devices can be operated in four different oscillator options. The user can program two configuration bits (FOSC1 and FOSC0) to select one of these four modes:

- LP Low Power Crystal
- XT Crystal/Resonator
- HS High Speed Crystal/Resonator
- RC Resistor/Capacitor

9.2.2 CRYSTAL OSCILLATOR / CERAMIC RESONATORS

In XT, LP or HS modes, a crystal or ceramic resonator is connected to the OSC1 and OSC2 pins to establish oscillation (Figure 9-1). The PIC16C62X oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in XT, LP or HS modes, the device can have an external clock source to drive the OSC1 pin (Figure 9-2).

FIGURE 9-1: CRYSTAL OPERATION (OR CERAMIC RESONATOR) (HS, XT OR LP OSC CONFIGURATION)



See Table 9-1 and Table 9-2 for recommended values of C1 and C2.

Note: A series resistor may be required for AT strip cut crystals.

FIGURE 9-2: EXTERNAL CLOCK INPUT OPERATION (HS, XT OR LP OSC



TABLE 9-1:CAPACITOR SELECTION FOR
CERAMIC RESONATORS

R	~[]				
Mode	Freq	OSC1(C1)	OSC2(C2)		
ХТ	455 kHz 2.0 MHz 4.0 MHz	22 - 100 pF 15 - 68 pF 15 - 68 pF	82 - 100 pF 15 - 68 pF 15 - 68 pF		
HS	8.0 MHz 16.0 MHz 🔨	10-68 bF 10-22 pF	10 - 68 pF 10 - 22 pF		
Higher capacitance increases the stability of the oscil- lator but also increases the start-up time. These wabes are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components.					

TABLE 9-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR

Mode	Freq	OSC1(C1)	OSC2(C2)		
LP	32 kHz	68 - 100 pF	68 - 100 pF		
	200 kHz	15 - 30 pF	15 - 30 pF		
хт	100 kHz	68 - 150 pF	150 - 300 pF		
	2 MHz	15 - 30 pF	15 - 30 pF		
	4 MHz	15 - 30 pF	15 - 30 pF		
HS	8 MHz	15-30 pF	^V 15 - 30 pF		
	10 MHz	15-30 pF	15 - 30 pF		
	20 MHz 🔨	15-30 pF	15 - 30 pF		
Higher capacitance increases the stability of the oscillator but also increases the start-up time. These values are for design guidance only. Rs may be required in HS mode as well as XT mode to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.					

TABLE 9-4: INITIALIZATION CONDITION FOR SPECIAL REGISTERS

Condition	Program Counter	STATUS Register	PCON Register
Power-on Reset	000h	0001 1xxx	0x
MCLR Reset during normal operation	000h	000u uuuu	uu
MCLR Reset during SLEEP	000h	0001 0uuu	uu
WDT Reset	000h	0000 uuuu	uu
WDT Wake-up	PC + 1	uuu0 0uuu	uu
Brown-out Reset	000h	000x xuuu	u0
Interrupt Wake-up from SLEEP	PC + 1 ⁽¹⁾	uuul 0uuu	uu

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0'.

Note 1: When the wake-up is due to an interrupt and global enable bit, GIE is set, the PC is loaded with the interrupt vector (0004h) after execution of PC+1.

Register	Address	Power-on Reset	MCLR Reset during normal operation MCLR Reset during SLEEP WDT Reset Brown-out Reset ⁽¹⁾	 Wake-up from SLEEP through interrupt Wake-up from SLEEP through WDT time-out
W		****		1111111 1111111
INDF	00h		_	_
TMR0	01h	xxxx xxxx	<u>uuuu</u> uuuu	<u>uuuu</u> uuuu
PCL	02h	0000 0000	0000 0000	PC + 1 ⁽³⁾
STATUS	03h	0001 1xxx	000q quuu ⁽⁴⁾	uuuq quuu ⁽⁴⁾
FSR	04h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTA	05h	x xxxx	u uuuu	u uuuu
PORTB	06h	xxxx xxxx	uuuu uuuu	uuuu uuuu
CMCON	1Fh	00 0000	00 0000	uu uuuu
PCLATH	0Ah	0 0000	0 0000	u uuuu
INTCON	0Bh	0000 000x	0000 000u	uuuu uqqq ⁽²⁾
PIR1	0Ch	-0	-0	-q (2,5)
OPTION	81h	1111 1111	1111 1111	սսսս սսսս
TRISA	85h	1 1111	1 1111	u uuuu
TRISB	86h	1111 1111	1111 1111	սսսս սսսս
PIE1	8Ch	-0	-0	-u
PCON	8Eh	0x	uq ^(1,6)	uu
VRCON	9Fh	000- 0000	000- 0000	uuu- uuuu

TABLE 9-5: INITIALIZATION CONDITION FOR REGISTERS

 $\label{eq:legend: u = unchanged, x = unknown, - = unimplemented bit, reads as `0', q = value depends on condition.$

Note 1: If VDD goes too low, Power-on Reset will be activated and registers will be affected differently.

2: One or more bits in INTCON, PIR1 and/or PIR2 will be affected (to cause wake-up).

3: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

4: See Table 9-4 for RESET value for specific condition.

5: If wake-up was due to comparator input changing, then bit 6 = 1. All other interrupts generating a wake-up will cause bit 6 = u.

6: If RESET was due to brown-out, then bit 0 = 0. All other RESETS will cause bit 0 = u.

9.7 Watchdog Timer (WDT)

The Watchdog Timer is a free running on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the RC oscillator of the CLKIN pin. That means that the WDT will run, even if the clock on the OSC1 and OSC2 pins of the device has been stopped, for example, by execution of a SLEEP instruction. During normal operation, a WDT time-out generates a device RESET. If the device is in SLEEP mode, a WDT time-out causes the device to wake-up and continue with normal operation. The WDT can be permanently disabled by programming the configuration bit WDTE as clear (Section 9.1).

9.7.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms, (with no prescaler). The time-out periods vary with temperature, VDD and process variations from part to part (see

DC specs). If longer time-out periods are desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT under software control by writing to the OPTION register. Thus, time-out periods up to 2.3 seconds can be realized.

The CLRWDT and SLEEP instructions clear the WDT and the postscaler, if assigned to the WDT, and prevent it from timing out and generating a device RESET.

The $\overline{\text{TO}}$ bit in the STATUS register will be cleared upon a Watchdog Timer time-out.

9.7.2 WDT PROGRAMMING CONSIDERATIONS

It should also be taken in account that under worst case conditions (VDD = Min., Temperature = Max., max. WDT prescaler) it may take several seconds before a WDT time-out occurs.



FIGURE 9-17: WATCHDOG TIMER BLOCK DIAGRAM

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR Reset	Value on all other RESETS
2007h	Config. bits	—	BODEN	CP1	CP0	PWRTE	WDTE	FOSC1	FOSC0	—	—
81h	OPTION	RBPU	INTEDG	TOCS	TOSE	PSA	PS2	PS1	PS0	1111 1111	1111 1111

Legend: Shaded cells are not used by the Watchdog Timer.

Note: – = Unimplemented location, read as "0"

+ = Reserved for future use

10.1 Instruction Descriptions

ADDLW	Add Literal and W
Syntax:	[<i>label</i>] ADDLW k
Operands:	$0 \leq k \leq 255$
Operation:	$(W) + k \to (W)$
Status Affected:	C, DC, Z
Encoding:	11 111x kkkk kkkk
Description:	added to the eight bit literal 'k' and the result is placed in the W register.
Cycles:	1
Example	ADDLW 0x15
	Before Instruction W = 0x10 After Instruction W = 0x25

ANDLW	AND Literal with W					
Syntax:	[<i>label</i>] ANDLW k					
Operands:	$0 \le k \le 255$					
Operation:	(W) .AND. (k) \rightarrow (W)					
Status Affected:	Z					
Encoding:	11 1001 kkkk kkkk					
Description:	The contents of W register are AND'ed with the eight bit literal 'k'. The result is placed in the W register.					
Words:	1					
Cycles:	1					
Example	ANDLW 0x5F					
	Before Instruction W = 0xA3 After Instruction W = 0x03					
ANDWF	AND W with f					

ADDWF	Add W and f				
Syntax:	[<i>label</i>] ADDWF f,d				
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in [0,1] \end{array}$				
Operation:	$(W) + (f) \rightarrow (dest)$				
Status Affected:	C, DC, Z				
Encoding:	00 0111 dfff ffff				
Description:	Add the contents of the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.				
Words:	1				
Cycles:	1				
Example	ADDWF FSR, O				
	Before Instruction W = 0x17 FSR = 0xC2 After Instruction W = 0xD9 FSR = 0xC2				

ANDWF	AND W with f				
Syntax:	[<i>label</i>] ANDWF f,d				
Operands:	$0 \le f \le 127$ $d \in [0,1]$				
Operation:	(W) .AND. (f) \rightarrow (dest)				
Status Affected:	Z				
Encoding:	00 0101 dfff ffff				
Description:	AND the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.				
Words:	1				
Cycles:	1				
Example	ANDWF FSR, 1				
	Before Instruction W = 0x17 FSR = 0xC2 After Instruction W = 0x17 FSR = 0x02				

INCFSZ	Increment f, Skip if 0	IORWF	Inclusive OR W with f
Syntax:	[label] INCFSZ f,d	Syntax:	[<i>label</i>] IORWF f,d
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in [0,1] \end{array}$	Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(f) + 1 \rightarrow (dest), skip if result = 0	Operation:	(W) .OR. (f) \rightarrow (dest)
Status Affected:	None	Status Affected:	Z
Encoding:	00 1111 dfff ffff	Encoding:	00 0100 dfff ffff
Description:	The contents of register 'f' are incremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'.	Description:	Inclusive OR the W register with register 'f'. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.
	If the result is 0, the next instruc- tion which is already fetched is	Words:	1
	discarded. A NOP is executed	Cycles:	1
	instead making it a two-cycle	Example	IORWF RESULT, 0
	instruction.		Before Instruction
vvords:	1		$\begin{array}{rcl} RESULI &= & 0x13 \\ W &= & 0x91 \end{array}$
Cycles: Example	1(2) HERE INCFSZ CNT, 1 GOTO LOOP CONTINUE • •		After Instruction $\begin{array}{rcl} RESULT &= & 0x13 \\ W & = & 0x93 \\ Z & = & 1 \end{array}$
	Before Instruction	MOVLW	Move Literal to W
	PC = address HERE	Syntax:	[<i>label</i>] MOVLW k
	CNT = CNT + 1	Operands:	$0 \le k \le 255$
	if CNT= 0,	Operation:	$k \rightarrow (W)$
	if $CNT \neq 0$,	Status Affected:	None
	PC = address HERE +1	Encoding:	11 00xx kkkk kkkk
IORLW	Inclusive OR Literal with W	Description:	The eight bit literal 'k' is loaded into W register. The don't cares will assemble as 0's
Syntax:	[<i>label</i>] IORLW k	Words:	1
Operands:	$0 \le k \le 255$	Cycles:	1
Operation:	(W) .OR. $k \rightarrow$ (W)	Example	MOVLW 0x5A
Status Affected:	Z	_//on.pro	After Instruction
Encoding:	11 1000 kkkk kkkk		W = 0x5A
Description:	The contents of the W register is OR'ed with the eight bit literal 'k'. The result is placed in the W register.		
Words:	1		
Cycles:	1		
Example	IORLW 0x35		
	Before Instruction W = 0x9A After Instruction		

W = Z =

0xBF 1

MOVF	Move f					
Syntax:	[label] MOVF f,d					
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in [0,1] \end{array}$					
Operation:	$(f) \rightarrow (dest)$					
Status Affected:	Z					
Encoding:	00 1000 dfff ffff					
Description:	The contents of register f is moved to a destination dependent upon the status of d. If $d = 0$, destination is W register. If $d = 1$, the destination is file register f itself. $d = 1$ is useful to test a file register since status flag Z is affected.					
Words:	1					
Cycles:	1					
Example	MOVF FSR, 0					
	After Instruction W = value in FSR register Z = 1					
MOVWF	Move W to f					
Syntax:	[<i>label</i>] MOVWF f					
Operands:	$0 \leq f \leq 127$					
Operation:	$(W) \rightarrow (f)$					
Status Affected:	None					
Encoding:	00 0000 1fff ffff					
Description:	Move data from W register to reg- ister 'f'.					
Words:	1					
Cycles:	1					
Example	MOVWF OPTION					
	Before Instruction OPTION = 0xFF W = 0x4F					
	After Instruction OPTION = 0x4F W = 0x4F					

NOP	No Operation				
Syntax:	[label]	NOP			
Operands:	None				
Operation:	No operation				
Status Affected:	None				
Encoding:	00	0000	0xx0	0000	
Description:	No operation.				
Words:	1				
Cycles:	1				
Example	NOP				

OPTION	Load Option Register				
Syntax:	[label] OPTION				
Operands:	None				
Operation:	$(W) \rightarrow O$	PTION			
Status Affected:	None				
Encoding:	00	0000	0110	0010	
Description: Words: Cycles:	The contents of the W register are loaded in the OPTION register. This instruction is supported for code compatibility with PIC16C5X products. Since OPTION is a read- able/writable register, the user can directly address it.				
Example					
	To maintain upward compatibil- ity with future PICmicro [®] products, do not use this instruction.				

SUBLW	Subtract W from Literal	SUBWF	Subtract W from f
Syntax:	[<i>label</i>] SUBLW k	Syntax:	[<i>label</i>] SUBWF f,d
Operands:	$0 \le k \le 255$	Operands:	$0 \le f \le 127$
Operation:	$k - (W) \rightarrow (W)$		d ∈ [0,1]
Status Affected:	C, DC, Z	Operation: Status	(f) - (W) \rightarrow (dest) C, DC, Z
Encoding:	11 110x kkkk kkkk	Affected:	
Description:	The W register is subtracted (2's complement method) from the eight bit literal 'k'. The result is placed in the W register.	Encoding: Description:	000010dfffffffSubtract (2's complement method)W register from register 'f'. If 'd' is 0,the result is stored in the W register.If 'd' is 1, the result is stored head in
Words:	1		register 'f'.
Cycles:	1	Words:	1
Example 1:	SUBLW 0x02	Cycles:	1
	Before Instruction	Example 1:	SUBWF REG1,1
	W = 1 $C = ?$		Before Instruction
	After Instruction		REG1= 3
	W = 1		W = 2 C = ?
Example 2:	Before Instruction		After Instruction
Example 2.	W = 2 $C = ?$		REG1= 1 W = 2 C = 1; result is positive
	After Instruction	Example 2:	Before Instruction
	W = 0 C = 1; result is zero		REG1= 2 W = 2
Example 3:	Before Instruction		C = ?
	W = 3 C = ?		After Instruction REG1= 0
	After Instruction		W = 2
	W = 0xFF	Example 3	C = 1; result is zero Before Instruction
	C – 0, result is negative		REG1= 1 W = 2 C = ?
			After Instruction
			REG1= 0xFF W = 2 C = 0; result is negative

SWAPF	Swap Nibbles in f					
Syntax:	[label]	SWAPF	f,d			
Operands:	$\begin{array}{l} 0\leq f\leq 12\\ d\in [0,1] \end{array}$	27				
Operation:	(f<3:0>) - (f<7:4>) -	→ (dest< \rightarrow (dest<	7:4>), 3:0>)			
Status Affected:	None					
Encoding:	00	1110	dfff	Ē	ffff	
Description:	register 'f' are exchanged. If 'd' is 0, the result is placed in W register. If 'd' is 1, the result is placed in register 'f'.					
Words:	1					
Cycles:	1					
Example	SWAPF REG, 0					
	Before Instruction					
		REG1	=	0xA5		
	After Inst	ruction				
		REG1 W	= =	0xA5 0x5A		

TRIS	Load TRIS Register			
Syntax:	[<i>label</i>] TRIS f			
Operands:	$5 \le f \le 7$			
Operation:	(W) \rightarrow TRIS register f;			
Status Affected:	None			
Encoding:	00 0000 0110 Offf			
Description.	code compatibility with the PIC16C5X products. Since TRIS registers are readable and writable, the user can directly address them			
Words:	1			
Cycles:	1			
Example				
	To maintain upward compatibil- ity with future PICmicro [®] prod- ucts, do not use this instruction.			

XORLW	Exclusiv	ve OR L	iteral v	vith W			
Syntax:	[label]	XORL	Wk				
Operands:	$0 \le k \le 2$	$0 \le k \le 255$					
Operation:	(W) .XO	(W) .XOR. $k \rightarrow (W)$					
Status Affected:	Z						
Encoding:	11	11 1010 kkkk kkkk					
Description:	The cont are XOR literal 'k'. the W re	The contents of the W register are XOR'ed with the eight bit literal 'k'. The result is placed in the W register.					
Words:	1						
Cycles:	1						
Example:	XORLW	0xAF					
	Before Ir	nstructio	n				
		W =	0xB	5			
	After Ins	truction					
		W =	0x1A	A			
XORWF	Exclusiv	Exclusive OR W with f					
Syntax:	[label]	XORWF	f,d				
Operands:	$\begin{array}{l} 0 \leq f \leq 12 \\ d \in [0,1] \end{array}$	7					
Operation:	(W) .XOR	$R.(f) \to ($	dest)				
Status Affected:	Z						
Encoding:	00	0110	dfff	ffff			
Description:	Exclusive OR the contents of the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.						
Words:	1						
Cycles:	1						
Example	XORWF	REG	1				
	Before In:	struction	I				
		REG W	= (DxAF DxB5			
	After Inst	ruction					
		REG W	= (0x1A 0xB5			

12.3 DC CHARACTERISTICS: PIC16CR62XA-04 (Commercial, Industrial, Extended) PIC16CR62XA-20 (Commercial, Industrial, Extended) PIC16LCR62XA-04 (Commercial, Industrial, Extended) (CONT.)

		Standard Operating Conditions (unless otherwise stated)							
PIC16CR62XA-04		Operating temperature $-40^{\circ}C \leq TA \leq +85^{\circ}C$ for industrial and							
PIC16CR62XA-20				•			$0^{\circ}C \leq TA \leq +70^{\circ}C$ for commercial and		
						-4	$0^{\circ}C \leq TA \leq +125^{\circ}C$ for extended		
			Standard Operating Conditions (unless otherwise stated)						
			Opera	Operating temperature -40° C < TA < +85°C for industrial and					
PIC16LCR62XA-04		opora	ling ton	porat		0° C < TA < +70°C for commercial and			
						-40	1° C < TA < +125°C for extended		
Dorom	Sum	Characteristic	Min	Tunt	Mox	Unito			
No	Sym	Characteristic	IVIIII	турт	wax	Units	conditions		
NU.	1	(2)			050				
D020	IPD	Power-down Current ⁽³⁾		200	950	nA	VDD = 3.0V		
				0.400	1.0	μΑ			
				0.600	2.2	μΑ	VDD - 5.5V		
Daga	1	- (0)	_	5.0	9.0	μΑ	VDD – 5.5V Extended Temp.		
D020	IPD	Power-down Current ⁽³⁾	_	200	850	nA	VDD = 2.5V		
				200	950	nA A	$VDD = 3.0V^{*}$		
				0.600	2.2	μΑ	VDD = 5.5V		
D aga		(5)		5.0	9.0	μΑ			
D022	Δ IWDT	WD1 Current ⁽³⁾		6.0	10	μA	VDD=4.0V		
D0004	415.05	Decours out Decot Quere at(5)		75	12	μΑ	$\frac{(125^{\circ}C)}{C}$		
DUZZA		Brown-out Reset Current(*)		75	125	μΑ	BOD enabled, $VDD = 5.0V$		
D023		Comparator Current for each		30	60	μA	VDD = 4.0V		
00234		Vere Current ⁽⁵⁾		80	125				
DOZJA		WDT Current ⁽⁵⁾		00	100	μΑ	VDD = 4.0V		
D022		wDT Current(**		6.0	10	μΑ	VDD-4.0V (125°C)		
00224		Brown out Posot Current ⁽⁵⁾		75	12	μΑ	$\frac{(125)}{125}$ C)		
D022A		Comparator Current for each		30	60	μΑ	$V_{DD} = 4.0V$		
0025		Comparator ⁽⁵⁾		50	00	μΛ	VDD - 4.0V		
D023A	Δ IVREF	VREF Current ⁽⁵⁾		80	135	μA	VDD = 4.0V		
1A	Fosc	LP Oscillator Operating Frequency	0	_	200	kHz	All temperatures		
		RC Oscillator Operating Frequency	0		4	MHz	All temperatures		
		XT Oscillator Operating Frequency	0		4	MHz	All temperatures		
		HS Oscillator Operating Frequency	0		20	MHz	All temperatures		
1A	Fosc	LP Oscillator Operating Frequency	0		200	kHz	All temperatures		
		RC Oscillator Operating Frequency	0		4	MHz	All temperatures		
		XT Oscillator Operating Frequency	0	—	4	MHz	All temperatures		
		HS Oscillator Operating Frequency	0	—	20	MHz	All temperatures		

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in Active Operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tri-stated, pulled to VDD,

MCLR = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or Vss.

4: For RC osc configuration, current through REXT is not included. The current through the resistor can be estimated by the formula: Ir = VDD/2REXT (mA) with REXT in kΩ.

5: The ∆ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

6: Commercial temperature range only.

12.5 DC CHARACTERISTICS: PIC16C620A/C621A/C622A-40⁽⁷⁾ (Commercial) PIC16CR620A-40⁽⁷⁾ (Commercial)

DC CH	IARAC [.]	TERISTICS	Standard Operating Conditions (unless otherwise stated)Operating temperature $0^{\circ}C \leq TA \leq +70^{\circ}C$ for commercial					
Param No.	Sym	Characteristic	Min	Тур†	Мах	Unit	Conditions	
	VIL	Input Low Voltage						
		I/O ports						
D030		with TTL buffer	Vss	—	0.8V 0.15Vdd	V	VDD = 4.5V to 5.5V, otherwise	
D031		with Schmitt Trigger input	Vss		0.2VDD	V		
D032		MCLR, RA4/T0CKI, OSC1 (in RC mode)	Vss	—	0.2Vdd	V	(Note 1)	
D033		OSC1 (in XT and HS)	Vss	—	0.3VDD	V		
		OSC1 (in LP)	Vss	—	0.6Vdd - 1.0	V		
	Vih	Input High Voltage						
		I/O ports						
D040		with TTL buffer	2.0V	—	VDD	V	VDD = 4.5V to 5.5V, otherwise	
D044		with Ochavitt Triansations t	0.25 VDD + 0.8		VDD			
D041					VDD			
D042		MCLR RA4/TUCKI		_	VDD	V		
D043 D043A		OSC1 (AT, HS and LP)		_	VDD	v	(Note 1)	
D070	IPURB	PORTB Weak Pull-up Current	50	200	400	μА	$V_{DD} = 5.0V$. VPIN = Vss	
	liL	Input Leakage Current ^(2, 3)						
		I/O ports (except PORTA)			±1.0	μA	VSS \leq VPIN \leq VDD, pin at hi-impedance	
D060		PORTA	_	_	±0.5	μA	Vss \leq VPIN \leq VDD, pin at hi-impedance	
D061		RA4/T0CKI	—	—	±1.0	μA	$Vss \le VPIN \le VDD$	
D063		OSC1, MCLR	_	—	±5.0	μA	$Vss \leq VPIN \leq VDD,$ XT, HS and LP osc configuration	
	Vol	Output Low Voltage						
D080		I/O ports	_	—	0.6	V	IOL = 8.5 mA, VDD = 4.5V, -40° to +85°C	
			—	—	0.6	V	IOL = 7.0 mA, VDD = 4.5V, +125°C	
D083		OSC2/CLKOUT (RC only)	—	—	0.6	V	IOL = 1.6 mA, VDD = 4.5V, -40° to +85°C	
		(2)	_		0.6	V	IOL = 1.2 mA, VDD = 4.5V, +125°C	
	Vон	Output High Voltage ⁽³⁾						
D090		I/O ports (except RA4)	VDD-0.7	—	—	V	IOH = -3.0 mA, VDD = 4.5V, -40° to +85°C	
			VDD-0.7	—	—	V	IOH = -2.5 mA, VDD = 4.5V, +125°C	
D092		OSC2/CLKOUT (RC only)	VDD-0.7	—	—	V	IOH = -1.3 mA, VDD = 4.5V, -40° to +85°C	
*0450	1/25	On an Duain Ulink Matterna	VDD-0.7	_		V	IOH = -1.0 mA, VDD = 4.5V, +125°C	
"D150	VOD	Open Drain High Voltage			8.5	V	RA4 pin	
		Capacitive Loading Specs on Output Pins						
D100	Cosc2	OSC2 pin			15	pF	In XT, HS and LP modes when external clock used to drive OSC1	
D101	Сю	All I/O pins/OSC2 (in RC mode)			50	pF		

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in Active Operation mode are:

OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD, MCLR = VDD; WDT enabled/disabled as specified.
 The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in bi-impedance state and tied to VDD or VSS.

 mode, with all I/O pins in hi-impedance state and tied to VDD or VSs.
 For RC osc configuration, current through REXT is not included. The current through the resistor can be estimated by the formula Ir = VDD/ 2REXT (mA) with REXT in kΩ.

5: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

6: Commercial temperature range only.

7: See Section 12.1 and Section 12.3 for 16C62X and 16CR62X devices for operation between 20 MHz and 40 MHz for valid modified characteristics.

12.9 Timing Diagrams and Specifications

FIGURE 12-12: EXTERNAL CLOCK TIMING



TABLE 12-3: EXTERNAL CLOCK TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
1A	Fosc	External CLKIN Frequency ⁽¹⁾	DC	—	4	MHz	XT and RC Osc mode, VDD=5.0V
			DC	—	20	MHz	HS Osc mode
			DC	—	200	kHz	LP Osc mode
		Oscillator Frequency ⁽¹⁾	DC	—	4	MHz	RC Osc mode, VDD=5.0V
			0.1	_	4	MHz	XT Osc mode
			1	_	20	MHz	HS Osc mode
			DC	_	200	kHz	LP Osc mode
1	Tosc	External CLKIN Period ⁽¹⁾	250	_		ns	XT and RC Osc mode
			50	_		ns	HS Osc mode
			5	_	_	μS	LP Osc mode
		Oscillator Period ⁽¹⁾	250	_		ns	RC Osc mode
			250	_	10,000	ns	XT Osc mode
			50	_	1,000	ns	HS Osc mode
			5	_		μS	LP Osc mode
2	Тсү	Instruction Cycle Time ⁽¹⁾	1.0	Fosc/4	DC	μS	Tcys=Fosc/4
3*	TosL,	External Clock in (OSC1) High or	100*	_		ns	XT oscillator, Tosc L/H duty cycle
	TosH	Low Time	2*	_		μS	LP oscillator, Tosc L/H duty cycle
			20*	_		ns	HS oscillator, Tosc L/H duty cycle
4*	TosR,	External Clock in (OSC1) Rise or	25*	_		ns	XT oscillator
	TosF	Fall Time	50*	—	—	ns	LP oscillator
			15*	—	_	ns	HS oscillator

2: * These parameters are characterized but not tested.

3: † Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1 pin. When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

FIGURE 12-14: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING



FIGURE 12-15: BROWN-OUT RESET TIMING



TABLE 12-5:RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP
TIMER REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
30	TmcL	MCLR Pulse Width (low)	2000	—		ns	-40° to +85°C
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7*	18	33*	ms	VDD = 5.0V, -40° to +85°C
32	Tost	Oscillation Start-up Timer Period	_	1024 Tosc	_		Tosc = OSC1 period
33	Tpwrt	Power-up Timer Period	28*	72	132*	ms	VDD = 5.0V, -40° to +85°C
34	Tioz	I/O hi-impedance from MCLR low		—	2.0	μS	
35	TBOR	Brown-out Reset Pulse Width	100*	_		μs	$3.7V \leq V\text{DD} \leq 4.3V$

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

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