



Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	13
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 6V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lc622-04-ss

PIC16C62X

4.2.2.1 STATUS Register

The STATUS register, shown in Register 4-1, contains the arithmetic status of the ALU, the RESET status and the bank select bits for data memory.

The STATUS register can be the destination for any instruction, like any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper-three bits and set the Z bit. This leaves the STATUS register as 000uu1uu (where u = unchanged).

It is recommended, therefore, that only `BCF`, `BSF`, `SWAPF` and `MOVWF` instructions are used to alter the STATUS register, because these instructions do not affect any STATUS bit. For other instructions not affecting any STATUS bits, see the "Instruction Set Summary".

Note 1: The IRP and RP1 bits (STATUS<7:6>) are not used by the PIC16C62X and should be programmed as '0'. Use of these bits as general purpose R/W bits is NOT recommended, since this may affect upward compatibility with future products.

2: The C and DC bits operate as a Borrow and Digit Borrow out bit, respectively, in subtraction. See the `SUBLW` and `SUBWF` instructions for examples.

REGISTER 4-1: STATUS REGISTER (ADDRESS 03H OR 83H)

Reserved	Reserved	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
IRP	RP1	RP0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C
bit 7							bit 0

- bit 7 **IRP:** Register Bank Select bit (used for indirect addressing)
 1 = Bank 2, 3 (100h - 1FFh)
 0 = Bank 0, 1 (00h - FFh)
 The IRP bit is reserved on the PIC16C62X; always maintain this bit clear.
- bit 6-5 **RP<1:0>:** Register Bank Select bits (used for direct addressing)
 01 = Bank 1 (80h - FFh)
 00 = Bank 0 (00h - 7Fh)
 Each bank is 128 bytes. The RP1 bit is reserved on the PIC16C62X; always maintain this bit clear.
- bit 4 **$\overline{\text{TO}}$:** Time-out bit
 1 = After power-up, `CLRWDT` instruction, or `SLEEP` instruction
 0 = A WDT time-out occurred
- bit 3 **$\overline{\text{PD}}$:** Power-down bit
 1 = After power-up or by the `CLRWDT` instruction
 0 = By execution of the `SLEEP` instruction
- bit 2 **Z:** Zero bit
 1 = The result of an arithmetic or logic operation is zero
 0 = The result of an arithmetic or logic operation is not zero
- bit 1 **DC:** Digit carry/borrow bit (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions)(for borrow the polarity is reversed)
 1 = A carry-out from the 4th low order bit of the result occurred
 0 = No carry-out from the 4th low order bit of the result
- bit 0 **C:** Carry/borrow bit (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions)
 1 = A carry-out from the Most Significant bit of the result occurred
 0 = No carry-out from the Most Significant bit of the result occurred
- Note:** For borrow the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (`RRF`, `RLF`) instructions, this bit is loaded with either the high or low order bit of the source register.

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

6.0 TIMER0 MODULE

The Timer0 module timer/counter has the following features:

- 8-bit timer/counter
- Readable and writable
- 8-bit software programmable prescaler
- Internal or external clock select
- Interrupt on overflow from FFh to 00h
- Edge select for external clock

Figure 6-1 is a simplified block diagram of the Timer0 module.

Timer mode is selected by clearing the T0CS bit (OPTION<5>). In Timer mode, the TMR0 will increment every instruction cycle (without prescaler). If Timer0 is written, the increment is inhibited for the following two cycles (Figure 6-2 and Figure 6-3). The user can work around this by writing an adjusted value to TMR0.

Counter mode is selected by setting the T0CS bit. In this mode, Timer0 will increment either on every rising or falling edge of pin RA4/T0CKI. The incrementing edge is determined by the source edge (T0SE) control bit (OPTION<4>). Clearing the T0SE bit selects the rising edge. Restrictions on the external clock input are discussed in detail in Section 6.2.

The prescaler is shared between the Timer0 module and the Watchdog Timer. The prescaler assignment is controlled in software by the control bit PSA (OPTION<3>). Clearing the PSA bit will assign the prescaler to Timer0. The prescaler is not readable or writable. When the prescaler is assigned to the Timer0 module, prescale value of 1:2, 1:4, ..., 1:256 are selectable. Section 6.3 details the operation of the prescaler.

6.1 TIMER0 Interrupt

Timer0 interrupt is generated when the TMR0 register timer/counter overflows from FFh to 00h. This overflow sets the T0IF bit. The interrupt can be masked by clearing the T0IE bit (INTCON<5>). The T0IF bit (INTCON<2>) must be cleared in software by the Timer0 module interrupt service routine before re-enabling this interrupt. The Timer0 interrupt cannot wake the processor from SLEEP, since the timer is shut off during SLEEP. See Figure 6-4 for Timer0 interrupt timing.

FIGURE 6-1: TIMER0 BLOCK DIAGRAM

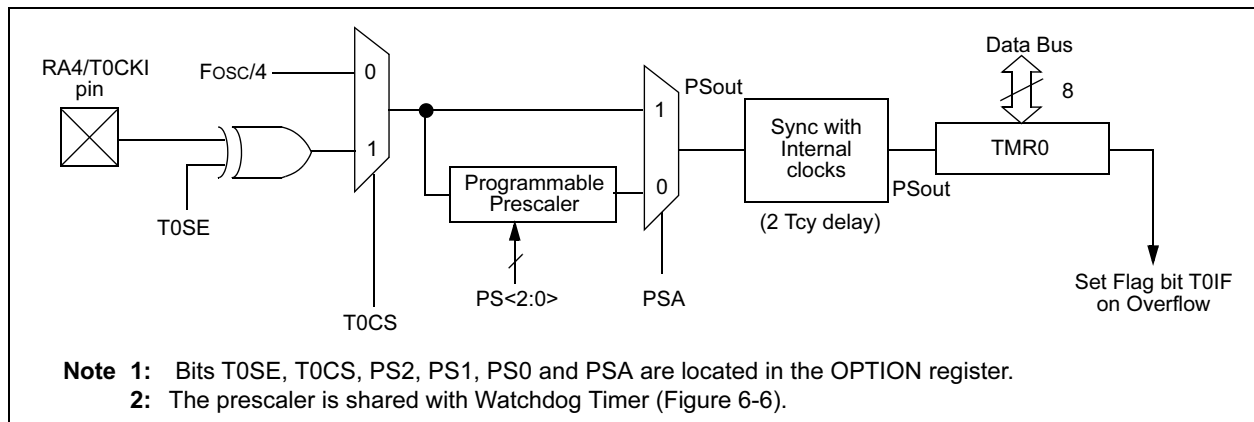
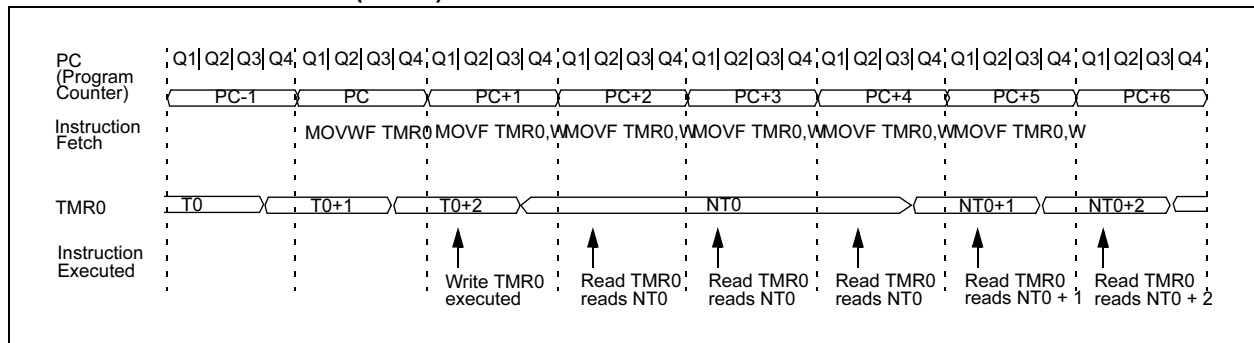


FIGURE 6-2: TIMER0 (TMR0) TIMING: INTERNAL CLOCK/NO PRESCALER



PIC16C62X

7.4 Comparator Response Time

Response time is the minimum time, after selecting a new reference voltage or input source, before the comparator output has a valid level. If the internal reference is changed, the maximum delay of the internal voltage reference must be considered when using the comparator outputs. Otherwise the maximum delay of the comparators should be used (Table 12-2).

7.5 Comparator Outputs

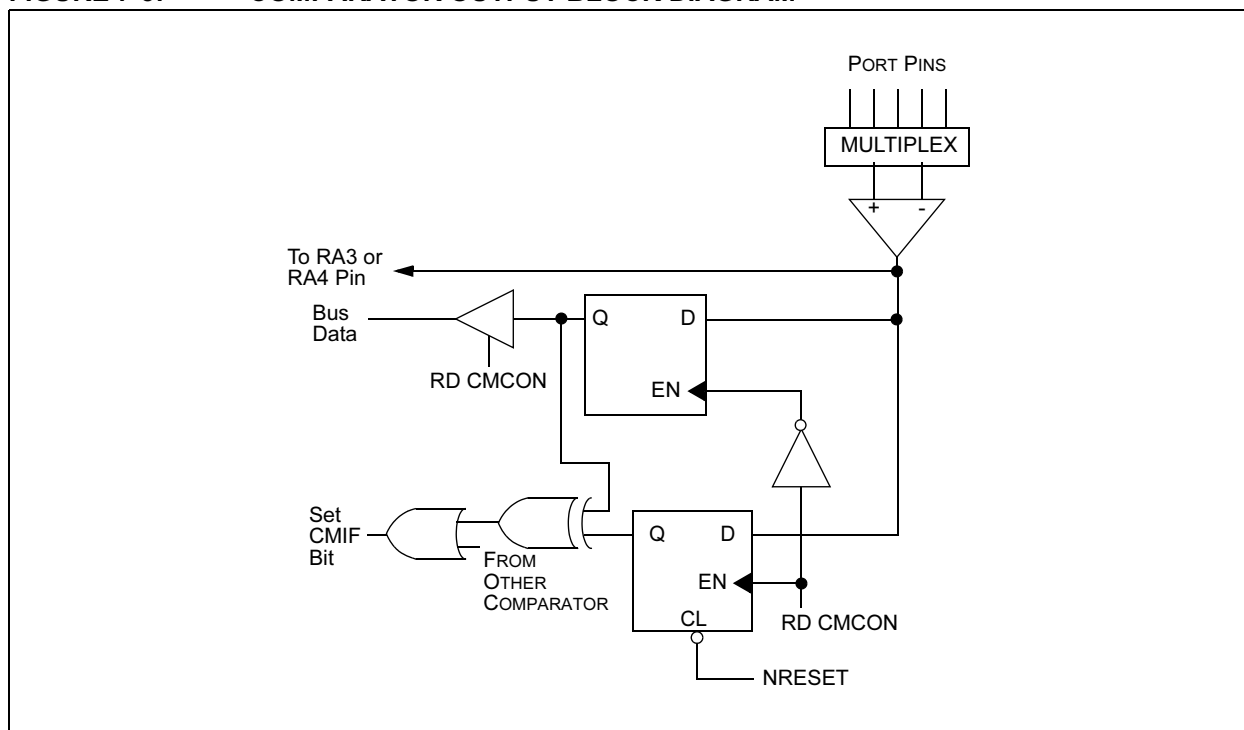
The comparator outputs are read through the CMCON register. These bits are read only. The comparator outputs may also be directly output to the RA3 and RA4 I/O pins. When the CM<2:0> = 110, multiplexors in the output path of the RA3 and RA4 pins will switch and the output of each pin will be the unsynchronized output of the comparator. The uncertainty of each of the comparators is related to the input offset voltage and the response time given in the specifications. Figure 7-3 shows the comparator output block diagram.

The TRISA bits will still function as an output enable/disable for the RA3 and RA4 pins while in this mode.

Note 1: When reading the PORT register, all pins configured as analog inputs will read as a '0'. Pins configured as digital inputs will convert an analog input according to the Schmitt Trigger input specification.

2: Analog levels on any pin that is defined as a digital input may cause the input buffer to consume more current than is specified.

FIGURE 7-3: COMPARATOR OUTPUT BLOCK DIAGRAM



PIC16C62X

TABLE 7-1: REGISTERS ASSOCIATED WITH COMPARATOR MODULE

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Value on All Other RESETS
1Fh	CMCON	C2OUT	C1OUT	—	—	CIS	CM2	CM1	CM0	00-- 0000	00-- 0000
9Fh	VRCON	VREN	VROE	VRR	—	VR3	VR2	VR1	VR0	000- 0000	000- 0000
0Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	—	CMIF	—	—	—	—	—	—	-0-- ----	-0-- ----
8Ch	PIE1	—	CMIE	—	—	—	—	—	—	-0-- ----	-0-- ----
85h	TRISA	—	—	—	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	---1 1111	---1 1111

Legend: x = unknown, u = unchanged, - = unimplemented, read as "0"

PIC16C62X

9.1 Configuration Bits

The configuration bits can be programmed (read as '0') or left unprogrammed (read as '1') to select various device configurations. These bits are mapped in program memory location 2007h.

The user will note that address 2007h is beyond the user program memory space. In fact, it belongs to the special test/configuration memory space (2000h – 3FFFh), which can be accessed only during programming.

REGISTER 9-1: CONFIGURATION WORD (ADDRESS 2007h)

CP1	CP0 (2)	CP1	$\overline{\text{CP0}}^{(2)}$	$\overline{\text{CP1}}$	CP0 (2)		BODEN	CP1	CP0 (2)	$\overline{\text{PWRT}}^{\text{E}}$	WDTE	F0SC1	F0SC0
bit 13													bit 0

bit 13-8, 5-4: **CP<1:0>**: Code protection bit pairs (2)
 Code protection for 2K program memory
 11 = Program memory code protection off
 10 = 0400h-07FFh code protected
 01 = 0200h-07FFh code protected
 00 = 0000h-07FFh code protected

Code protection for 1K program memory
 11 = Program memory code protection off
 10 = Program memory code protection off
 01 = 0200h-03FFh code protected
 00 = 0000h-03FFh code protected

Code protection for 0.5K program memory
 11 = Program memory code protection off
 10 = Program memory code protection off
 01 = Program memory code protection off
 00 = 0000h-01FFh code protected

bit 7: **Unimplemented**: Read as '0'

bit 6: **BODEN**: Brown-out Reset Enable bit (1)
 1 = BOR enabled
 0 = BOR disabled

bit 3: **PWRT^E**: Power-up Timer Enable bit (1, 3)
 1 = PWRT disabled
 0 = PWRT enabled

bit 2: **WDTE**: Watchdog Timer Enable bit
 1 = WDT enabled
 0 = WDT disabled

bit 1-0: **FOSC1:FOSC0**: Oscillator Selection bits
 11 = RC oscillator
 10 = HS oscillator
 01 = XT oscillator
 00 = LP oscillator

- Note 1:** Enabling Brown-out Reset automatically enables Power-up Timer (PWRT) regardless of the value of bit $\overline{\text{PWRT}}^{\text{E}}$. Ensure the Power-up Timer is enabled anytime Brown-out Detect Reset is enabled.
- 2:** All of the CP<1:0> pairs have to be given the same value to enable the code protection scheme listed.
- 3:** Unprogrammed parts default the Power-up Timer disabled.

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	1 = bit is set	0 = bit is cleared x = bit is unknown

TABLE 9-6: SUMMARY OF INTERRUPT REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR Reset	Value on all other RESETS ⁽¹⁾
0Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	—	CMIF	—	—	—	—	—	—	-0-- ----	-0-- ----
8Ch	PIE1	—	CMIE	—	—	—	—	—	—	-0-- ----	-0-- ----

Note 1: Other (non Power-up) Resets include MCLR Reset, Brown-out Reset and Watchdog Timer Reset during normal operation.

9.6 Context Saving During Interrupts

During an interrupt, only the return PC value is saved on the stack. Typically, users may wish to save key registers during an interrupt (e.g., W register and STATUS register). This will have to be implemented in software.

Example 9-3 stores and restores the STATUS and W registers. The user register, W_TEMP, must be defined in both banks and must be defined at the same offset from the bank base address (i.e., W_TEMP is defined at 0x20 in Bank 0 and it must also be defined at 0xA0 in Bank 1). The user register, STATUS_TEMP, must be defined in Bank 0. The Example 9-3:

- Stores the W register
- Stores the STATUS register in Bank 0
- Executes the ISR code
- Restores the STATUS (and bank select bit register)
- Restores the W register

EXAMPLE 9-3: SAVING THE STATUS AND W REGISTERS IN RAM

```

MOVWF  W_TEMP      ;copy W to temp register,
                    ;could be in either bank
SWAPF  STATUS,W     ;swap status to be saved
                    ;into W
BCF    STATUS,RP0    ;change to bank 0 regardless
                    ;of current bank
MOVWF  STATUS_TEMP  ;save status to bank 0
                    ;register
:
:    (ISR)
:
SWAPF  STATUS_TEMP, ;swap STATUS_TEMP register
W      ;into W, sets bank to origi-
      ;nal
      ;state
MOVWF  STATUS       ;move W into STATUS register
SWAPF  W_TEMP,F     ;swap W_TEMP
SWAPF  W_TEMP,W     ;swap W_TEMP into W

```

PIC16C62X

CLRW Clear W

Syntax: [*label*] CLRW

Operands: None

Operation: 00h → (W)
1 → Z

Status Affected: Z

Encoding:

00	0001	0000	0011
----	------	------	------

Description: W register is cleared. Zero bit (Z) is set.

Words: 1

Cycles: 1

Example CLRW

Before Instruction

W = 0x5A

After Instruction

W = 0x00

Z = 1

CLRWDT Clear Watchdog Timer

Syntax: [*label*] CLRWDT

Operands: None

Operation: 00h → WDT
0 → WDT prescaler,
1 → $\overline{TO}$
1 → $\overline{PD}$

Status Affected: $\overline{TO}$, $\overline{PD}$

Encoding:

00	0000	0110	0100
----	------	------	------

Description: CLRWDT instruction resets the Watchdog Timer. It also resets the prescaler of the WDT. STATUS bits $\overline{TO}$ and $\overline{PD}$ are set.

Words: 1

Cycles: 1

Example CLRWDT

Before Instruction

WDT counter = ?

After Instruction

WDT counter = 0x00

WDT prescaler = 0

$\overline{TO}$ = 1

$\overline{PD}$ = 1

COMF Complement f

Syntax: [*label*] COMF f,d

Operands: $0 \leq f \leq 127$
 $d \in [0,1]$

Operation: $(\bar{f}) \rightarrow (\text{dest})$

Status Affected: Z

Encoding:

00	1001	dfff	ffff
----	------	------	------

Description: The contents of register 'f' are complemented. If 'd' is 0, the result is stored in W. If 'd' is 1, the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example COMF REG1,0

Before Instruction

REG1 = 0x13

After Instruction

REG1 = 0x13

W = 0xEC

DECF Decrement f

Syntax: [*label*] DECF f,d

Operands: $0 \leq f \leq 127$
 $d \in [0,1]$

Operation: $(f) - 1 \rightarrow (\text{dest})$

Status Affected: Z

Encoding:

00	0011	dfff	ffff
----	------	------	------

Description: Decrement register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example DECF CNT, 1

Before Instruction

CNT = 0x01

Z = 0

After Instruction

CNT = 0x00

Z = 1

MOVF		Move f		
Syntax:	[<i>label</i>] MOVF f,d			
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$			
Operation:	$(f) \rightarrow (dest)$			
Status Affected:	Z			
Encoding:	00	1000	dfff	ffff
Description:	The contents of register f is moved to a destination dependent upon the status of d. If d = 0, destination is W register. If d = 1, the destination is file register f itself. d = 1 is useful to test a file register since status flag Z is affected.			
Words:	1			
Cycles:	1			
Example	MOVF FSR, 0			
After Instruction				
	W	=	value in FSR	
	register			
	Z	=	1	

MOVWF	Move W to f				
Syntax:	[<i>label</i>] MOVWF f				
Operands:	0 ≤ f ≤ 127				
Operation:	(W) → (f)				
Status Affected:	None				
Encoding:	<table><tr><td>00</td><td>0000</td><td>1fff</td><td>ffff</td></tr></table>	00	0000	1fff	ffff
00	0000	1fff	ffff		
Description:	Move data from W register to register 'f'.				
Words:	1				
Cycles:	1				
Example	MOVWF OPTION				
	Before Instruction				
	OPTION = 0xFF				
	W = 0x4F				
	After Instruction				
	OPTION = 0x4F				
	W = 0x4F				

NOP	No Operation			
Syntax:	[<i>label</i>] NOP			
Operands:	None			
Operation:	No operation			
Status Affected:	None			
Encoding:	00	0000	0xx0	0000
Description:	No operation.			
Words:	1			
Cycles:	1			
Example	NOP			

OPTION	Load Option Register				
Syntax:	[<i>label</i>] OPTION				
Operands:	None				
Operation:	(W) → OPTION				
Status Affected:	None				
Encoding:	<table><tr><td>00</td><td>0000</td><td>0110</td><td>0010</td></tr></table>	00	0000	0110	0010
00	0000	0110	0010		
Description:	The contents of the W register are loaded in the OPTION register. This instruction is supported for code compatibility with PIC16C5X products. Since OPTION is a readable/writable register, the user can directly address it.				
Words:	1				
Cycles:	1				
Example	To maintain upward compatibility with future PICmicro[®] products, do not use this instruction.				

Operands: None

Status Affected: None

Description: Return from Interrupt. Stack is POPed and Top of Stack (TOS) is loaded in the PC. Interrupts are enabled by setting Global Interrupt Enable bit, GIE (INTCON<7>). This is a two-cycle instruction.

Cycles: 2

Example RETFIE

Operands: $0 \leq k \leq 255$

Status Affected: None

Description: The W register is loaded with the eight bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a two-cycle instruction.

Cycles: 2

TABLE

Operands: None

Status Affected: None

Description: Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a two-cycle instruction.

Cycles: 2

Example	RETURN
---------	--------

FIGURE 12-7: PIC16CR62XA VOLTAGE-FREQUENCY GRAPH, $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$

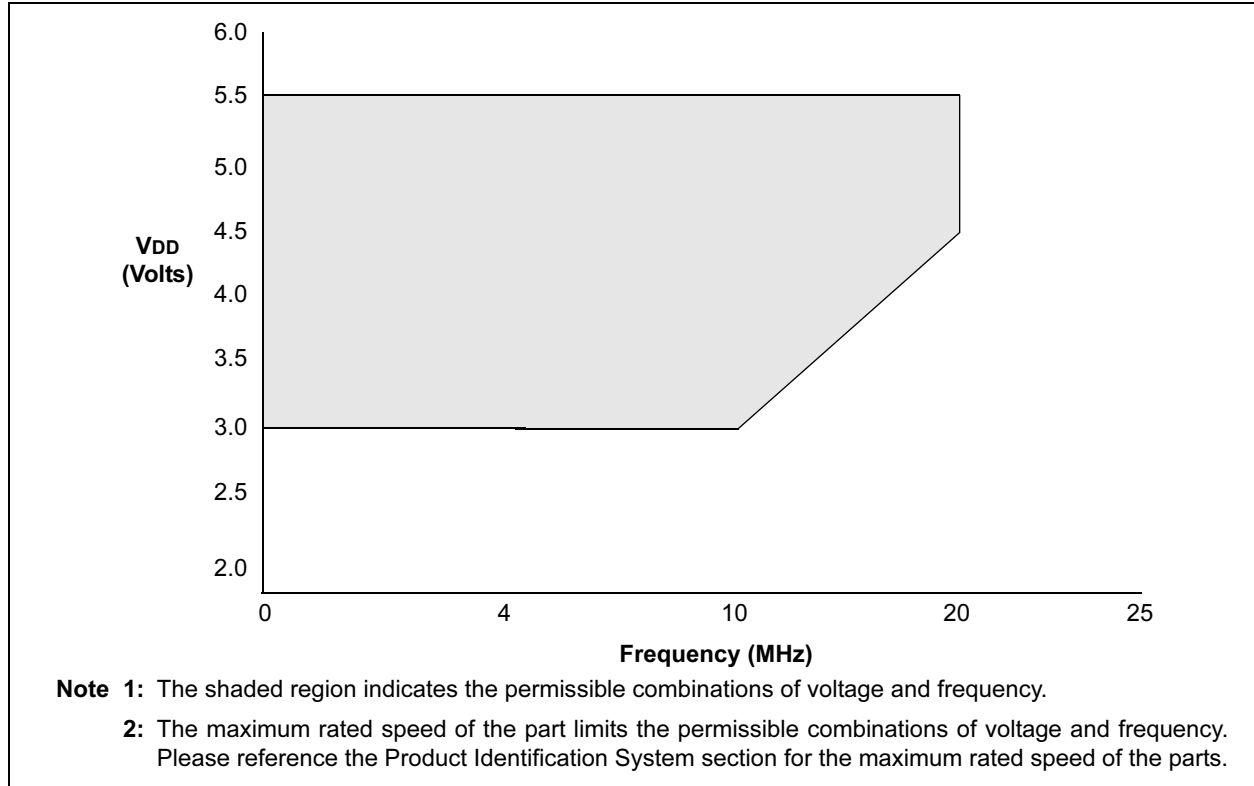
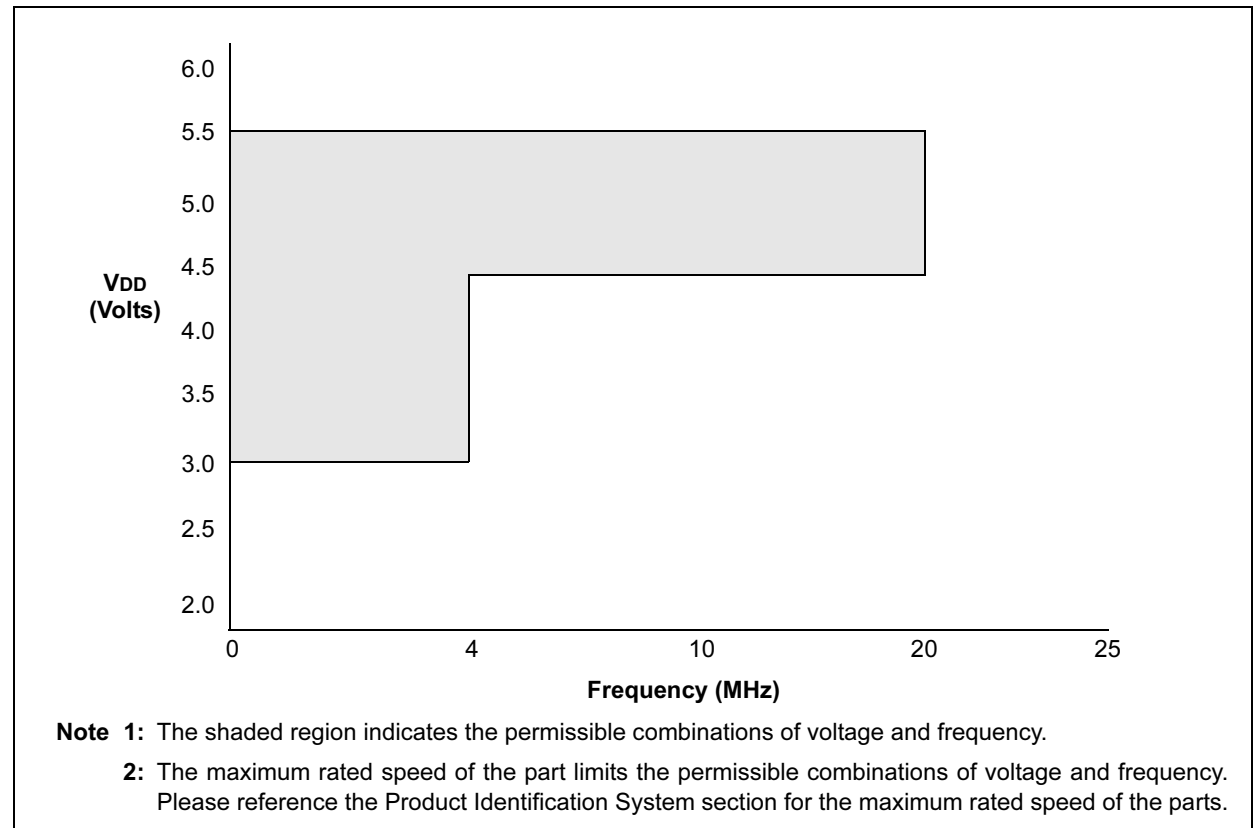


FIGURE 12-8: PIC16CR62XA VOLTAGE-FREQUENCY GRAPH, $-40^{\circ}\text{C} \leq T_A \leq 0^{\circ}\text{C}$, $+70^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$



PIC16C62X

12.2 DC Characteristics: PIC16C62XA-04 (Commercial, Industrial, Extended) PIC16C62XA-20 (Commercial, Industrial, Extended) PIC16LC62XA-04 (Commercial, Industrial, Extended (CONT.))

PIC16C62XA			Standard Operating Conditions (unless otherwise stated)				
			Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial and -40°C ≤ TA ≤ +125°C for extended				
PIC16LC62XA			Standard Operating Conditions (unless otherwise stated)				
			Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial and -40°C ≤ TA ≤ +125°C for extended				
Param. No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D022	ΔI _{WDT}	WDT Current ⁽⁵⁾	—	6.0	10	μA	V _{DD} = 4.0V (125°C)
D022A	ΔI _{BOR}	Brown-out Reset Current ⁽⁵⁾	—	75	125	μA	BOD enabled, V _{DD} = 5.0V
D023	ΔI _{COMP}	Comparator Current for each Comparator ⁽⁵⁾	—	30	60	μA	V _{DD} = 4.0V
D023A	ΔI _{VREF}	VREF Current ⁽⁵⁾	—	80	135	μA	V _{DD} = 4.0V
D022	ΔI _{WDT}	WDT Current ⁽⁵⁾	—	6.0	10	μA	V _{DD} = 4.0V (125°C)
D022A	ΔI _{BOR}	Brown-out Reset Current ⁽⁵⁾	—	75	125	μA	BOD enabled, V _{DD} = 5.0V
D023	ΔI _{COMP}	Comparator Current for each Comparator ⁽⁵⁾	—	30	60	μA	V _{DD} = 4.0V
D023A	ΔI _{VREF}	VREF Current ⁽⁵⁾	—	80	135	μA	V _{DD} = 4.0V
1A	FOSC	LP Oscillator Operating Frequency	0	—	200	kHz	All temperatures
		RC Oscillator Operating Frequency	0	—	4	MHz	All temperatures
		XT Oscillator Operating Frequency	0	—	4	MHz	All temperatures
		HS Oscillator Operating Frequency	0	—	20	MHz	All temperatures
1A	FOSC	LP Oscillator Operating Frequency	0	—	200	kHz	All temperatures
		RC Oscillator Operating Frequency	0	—	4	MHz	All temperatures
		XT Oscillator Operating Frequency	0	—	4	MHz	All temperatures
		HS Oscillator Operating Frequency	0	—	20	MHz	All temperatures

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which V_{DD} can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all I_{DD} measurements in Active Operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tri-stated, pulled to V_{DD},

MCLR = V_{DD}; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to V_{DD} or V_{SS}.

4: For RC osc configuration, current through R_{EXT} is not included. The current through the resistor can be estimated by the formula: I_r = V_{DD}/2R_{EXT} (mA) with R_{EXT} in kΩ.

5: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base I_{DD} or I_{PD} measurement.

6: Commercial temperature range only.

PIC16C62X

PIC16CR62XA-04 PIC16CR62XA-20			Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial and $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial and $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended				
PIC16LCR62XA-04			Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial and $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial and $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended				
Param. No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in Active Operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tri-stated, pulled to VDD,

MCLR = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or VSS.

4: For RC osc configuration, current through REXT is not included. The current through the resistor can be estimated by the formula: $I_r = V_{DD}/2R_{EXT}$ (mA) with REXT in kΩ.

5: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

6: Commercial temperature range only.

PIC16C62X

12.4 DC Characteristics: PIC16C62X/C62XA/CR62XA (Commercial, Industrial, Extended) PIC16LC62X/LC62XA/LCR62XA (Commercial, Industrial, Extended)

PIC16C62X/C62XA/CR62XA			Standard Operating Conditions (unless otherwise stated)				
			Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial and $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial and $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended				
PIC16LC62X/LC62XA/LCR62XA			Standard Operating Conditions (unless otherwise stated)				
			Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial and $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial and $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended				
Param. No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D030 D031 D032 D033	V _{IL}	Input Low Voltage					
		I/O ports					
		with TTL buffer	V _{SS}	—	0.8V 0.15 V _{DD}	V	V _{DD} = 4.5V to 5.5V otherwise
		with Schmitt Trigger input	V _{SS}	—	0.2 V _{DD}	V	
		MCLR, RA4/T0CKI, OSC1 (in RC mode)	V _{SS}	—	0.2 V _{DD}	V	(Note 1)
D030 D031 D032 D033	V _{IL}	OSC1 (in XT and HS)	V _{SS}	—	0.3 V _{DD}	V	
		OSC1 (in LP)	V _{SS}	—	0.6 V _{DD} - 1.0	V	
D030 D031 D032 D033	V _{IL}	Input Low Voltage					
		I/O ports					
		with TTL buffer	V _{SS}	—	0.8V 0.15 V _{DD}	V	V _{DD} = 4.5V to 5.5V otherwise
		with Schmitt Trigger input	V _{SS}	—	0.2 V _{DD}	V	
		MCLR, RA4/T0CKI, OSC1 (in RC mode)	V _{SS}	—	0.2 V _{DD}	V	(Note 1)
D030 D031 D032 D033	V _{IL}	OSC1 (in XT and HS)	V _{SS}	—	0.3 V _{DD}	V	
		OSC1 (in LP)	V _{SS}	—	0.6 V _{DD} - 1.0	V	
D040 D041 D042 D043 D043A	V _{IH}	Input High Voltage					
		I/O ports					
		with TTL buffer	2.0V 0.25 V _{DD} + 0.8V	—	V _{DD} V _{DD}	V	V _{DD} = 4.5V to 5.5V otherwise
		with Schmitt Trigger input	0.8 V _{DD}	—	V _{DD}	V	
		MCLR RA4/T0CKI	0.8 V _{DD}	—	V _{DD}	V	
D043 D043A	V _{IH}	OSC1 (XT, HS and LP)	0.7 V _{DD}	—	V _{DD}	V	
		OSC1 (in RC mode)	0.9 V _{DD}	—	V _{DD}	V	(Note 1)

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

- Note 1:** In RC oscillator configuration, the OSC1 pin is a Schmitt Trigger input. It is not recommended that the PIC16C62X(A) be driven with external clock in RC mode.
- 2:** The leakage current on the MCLR pin is strongly dependent on applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
- 3:** Negative current is defined as coming out of the pin.

FIGURE 12-13: CLKOUT AND I/O TIMING

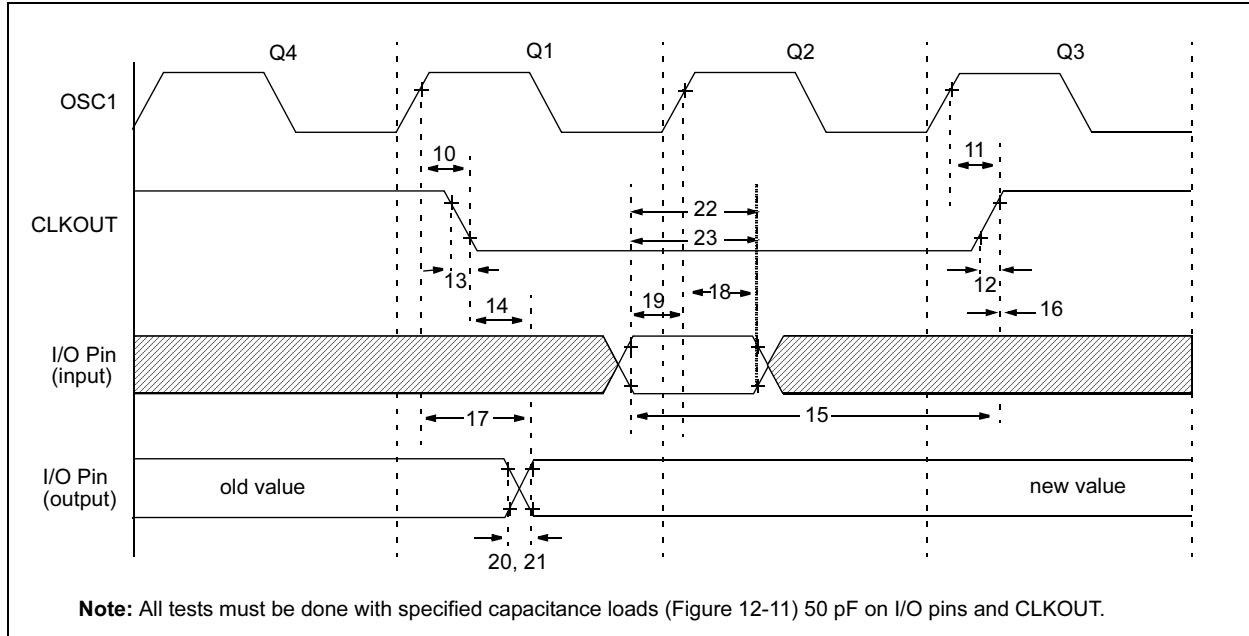


FIGURE 12-14: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

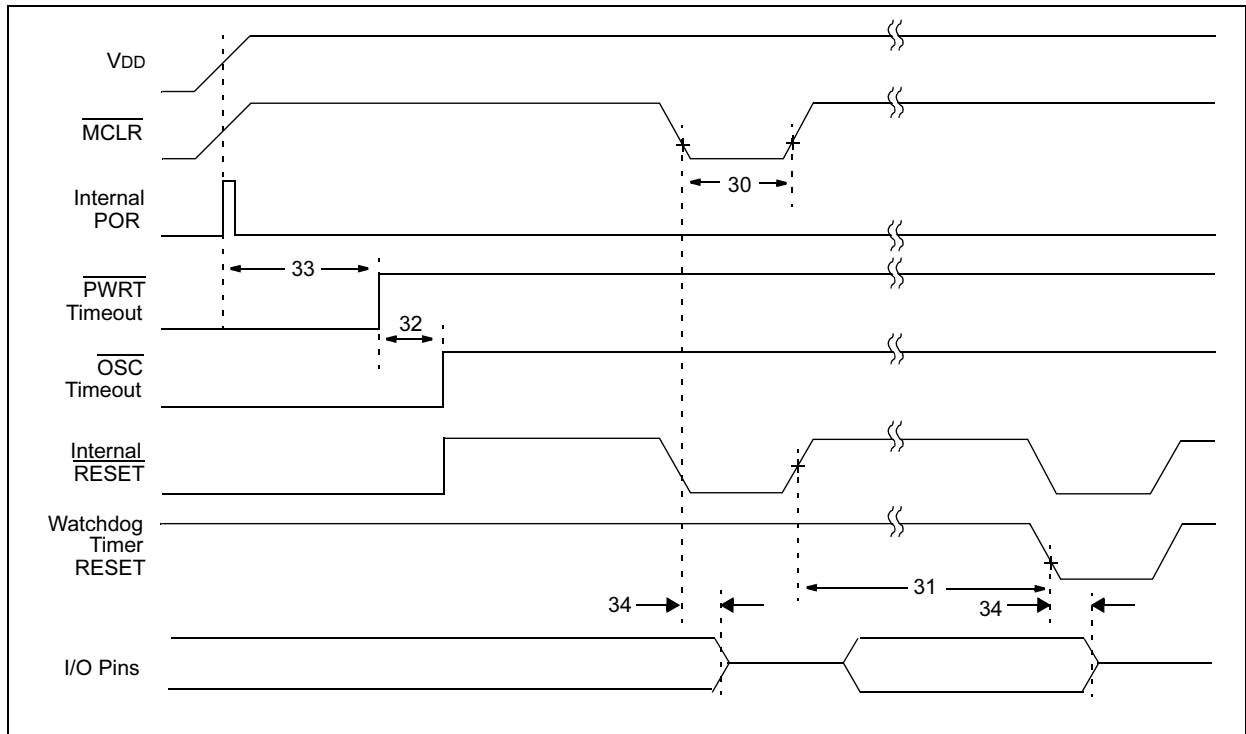


FIGURE 12-15: BROWN-OUT RESET TIMING

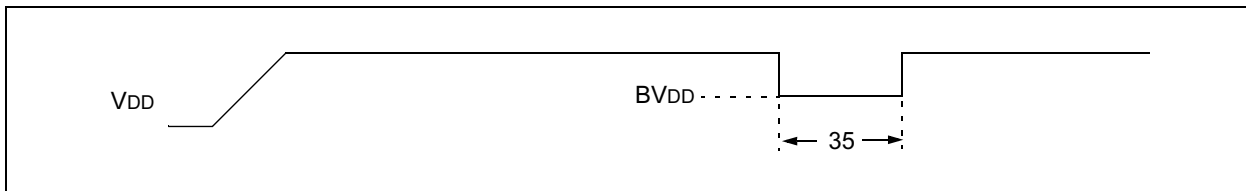


TABLE 12-5: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	Tmcl	MCLR Pulse Width (low)	2000	—	—	ns	-40° to +85°C
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7*	18	33*	ms	VDD = 5.0V, -40° to +85°C
32	Tost	Oscillation Start-up Timer Period	—	1024 TOSC	—	—	TOSC = OSC1 period
33	Tpwrt	Power-up Timer Period	28*	72	132*	ms	VDD = 5.0V, -40° to +85°C
34	TIOZ	I/O hi-impedance from MCLR low	—	—	2.0	μs	
35	TBOR	Brown-out Reset Pulse Width	100*	—	—	μs	3.7V ≤ VDD ≤ 4.3V

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

PIC16C62X

FIGURE 12-16: TIMER0 CLOCK TIMING

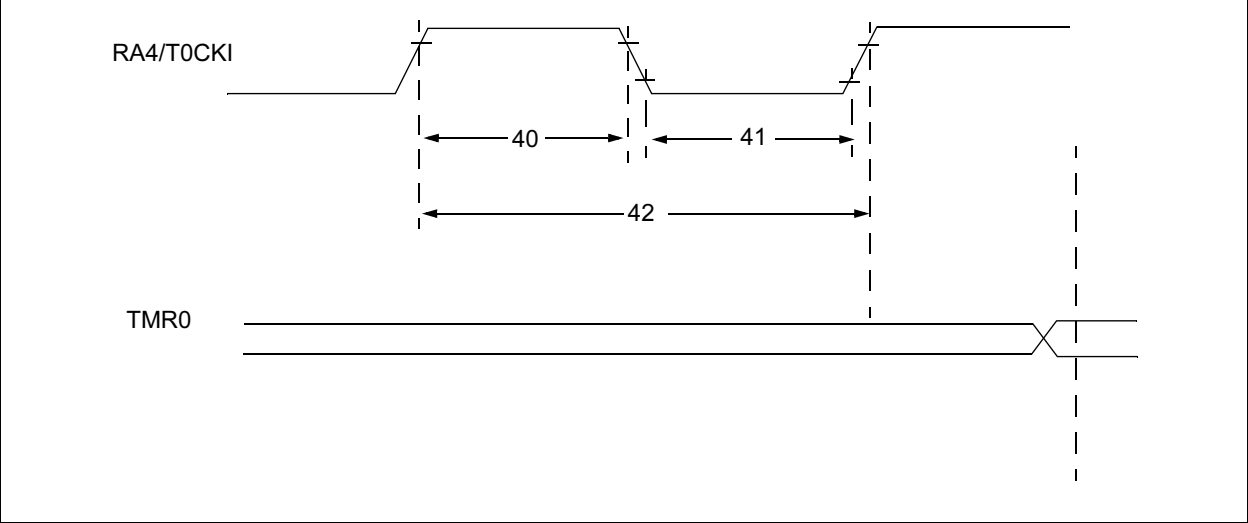


TABLE 12-6: TIMER0 CLOCK REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width	No Prescaler	0.5 TcY + 20*	—	—	ns	
			With Prescaler	10*	—	—	ns	
41	Tt0L	T0CKI Low Pulse Width	No Prescaler	0.5 TcY + 20*	—	—	ns	
			With Prescaler	10*	—	—	ns	
42	Tt0P	T0CKI Period		$\frac{TcY + 40^*}{N}$	—	—	ns	N = prescale value (1, 2, 4, ..., 256)

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 13-5: I_{OH} vs. V_{OH} , $V_{DD} = 3.0V$

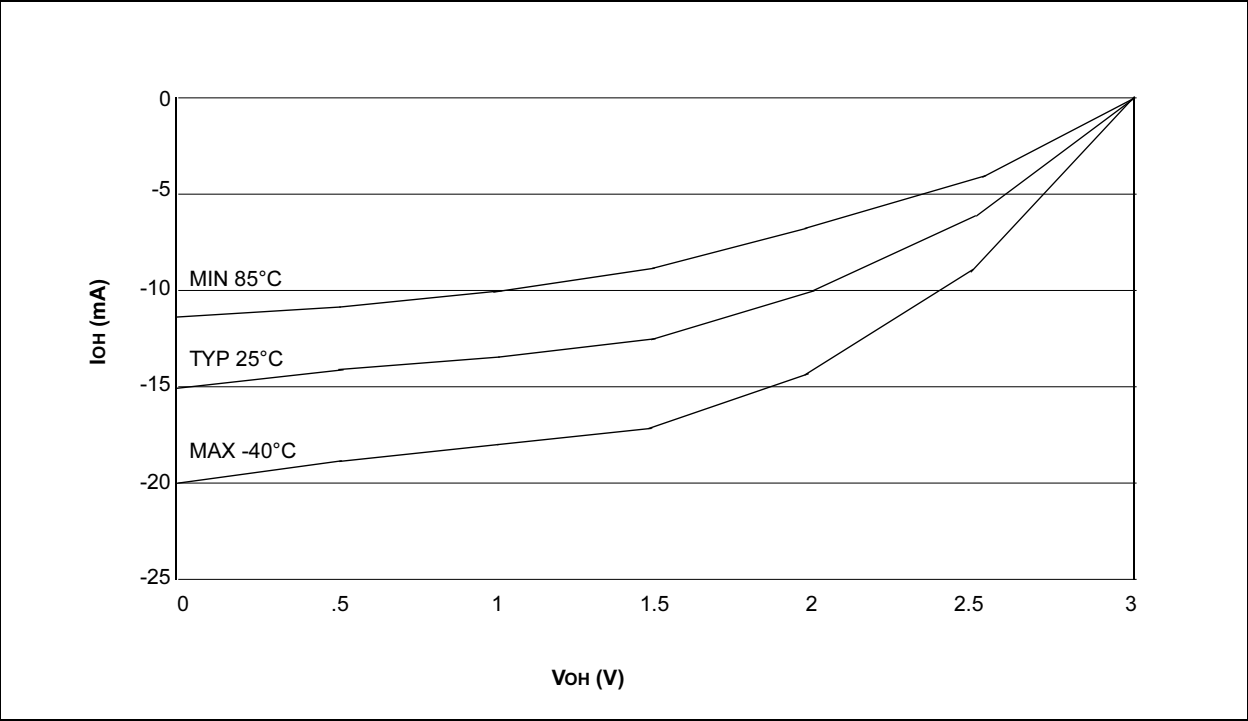
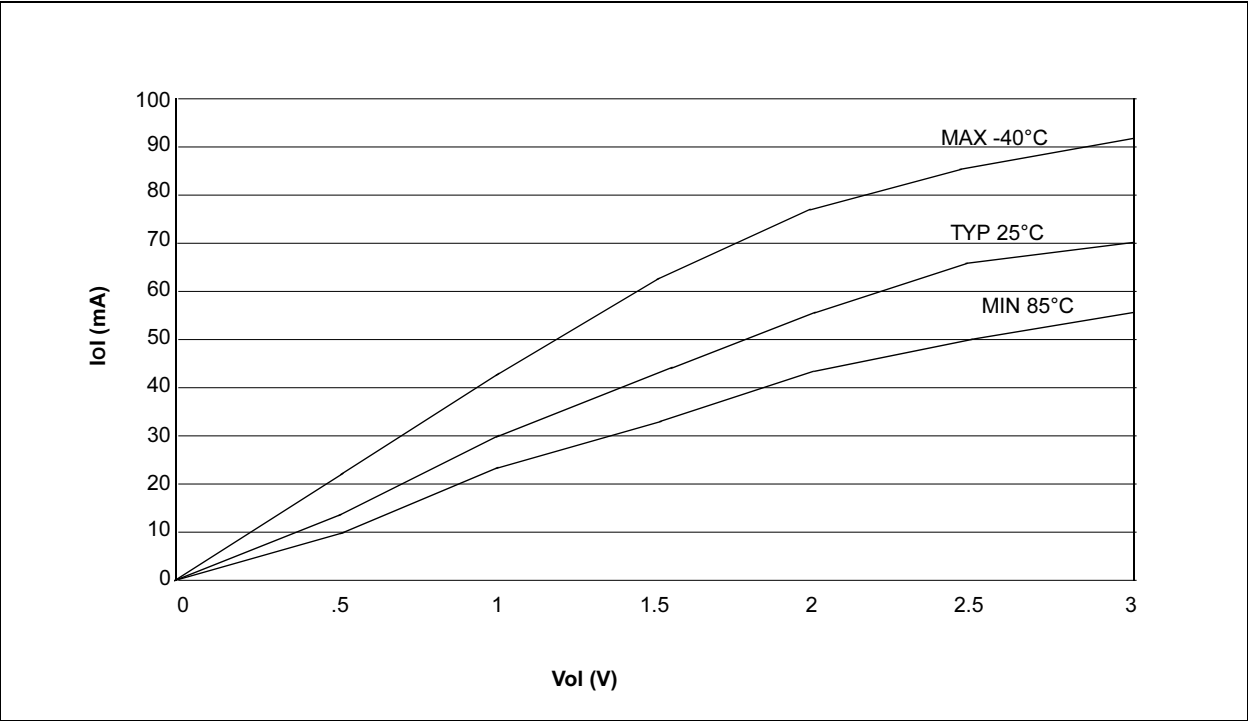
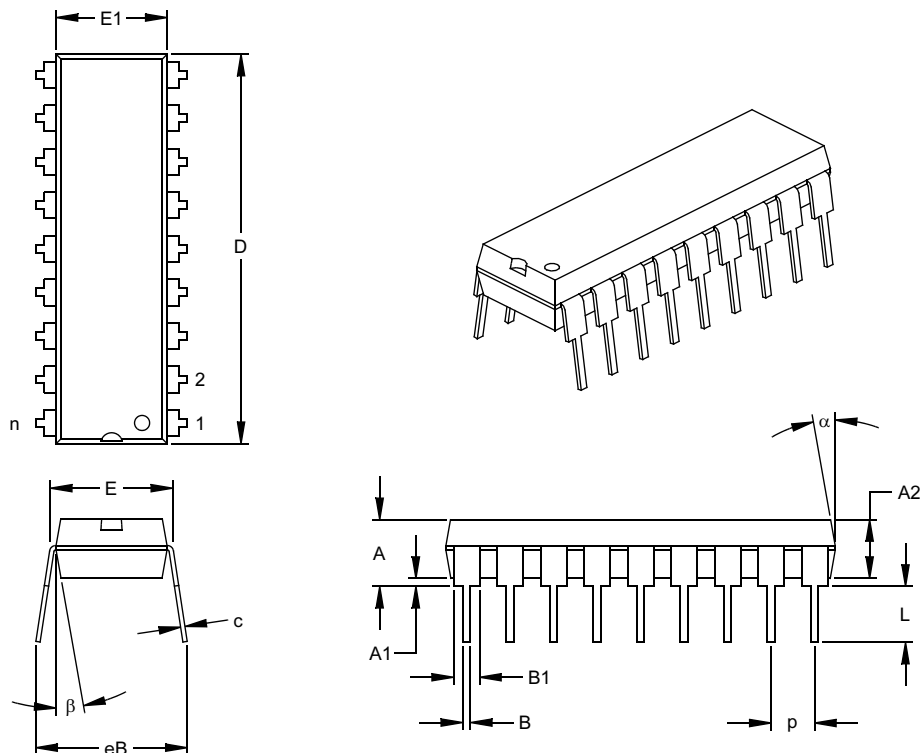


FIGURE 13-6: I_{OL} vs. V_{OL} , $V_{DD} = 5.5V$



PIC16C62X

18-Lead Plastic Dual In-line (P) – 300 mil (PDIP)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		18			18	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.890	.898	.905	22.61	22.80	22.99
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing	§ eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter

§ Significant Characteristic

Notes:

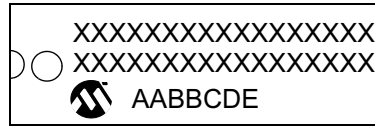
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-001

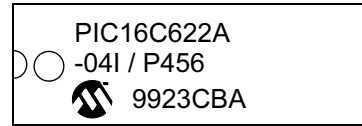
Drawing No. C04-007

14.1 Package Marking Information

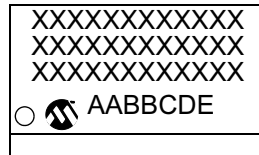
18-Lead PDIP



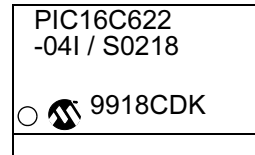
Example



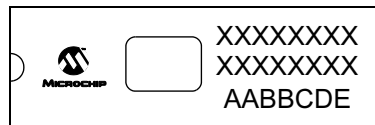
18-Lead SOIC (.300")



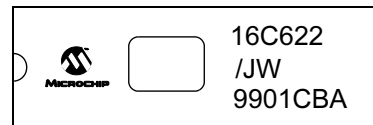
Example



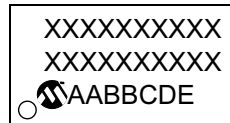
18-Lead Cerdip Windowed



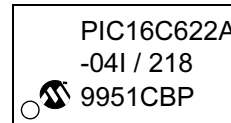
Example



20-Lead SSOP



Example



Legend: XX...X Customer specific information*
 Y Year code (last digit of calendar year)
 YY Year code (last 2 digits of calendar year)
 WW Week code (week of January 1 is week '01')
 NNN Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

* Standard PICmicro device marking consists of Microchip part number, year code, week code, and traceability code. For PICmicro device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

PIC16C62X

N

NOP Instruction 69

O

One-Time-Programmable (OTP) Devices 7

OPTION Instruction 69

OPTION Register 19

Oscillator Configurations 47

Oscillator Start-up Timer (OST) 50

P

Package Marking Information 117

Packaging Information 113

PCL and PCLATH 23

PCON Register 22

PICKit 1 FLASH Starter Kit 79

PICSTART Plus Development Programmer 77

PIE1 Register 21

PIR1 Register 21

Port RB Interrupt 56

PORTA 25

PORTB 28

Power Control/Status Register (PCON) 51

Power-Down Mode (SLEEP) 59

Power-On Reset (POR) 50

Power-up Timer (PWRT) 50

Prescaler 34

PRO MATE II Universal Device Programmer 77

Program Memory Organization 13

Q

Quick-Turnaround-Production (QTP) Devices 7

R

RC Oscillator 48

Reset 49

RETFIE Instruction 70

RETLW Instruction 70

RETURN Instruction 70

RLF Instruction 71

RRF Instruction 71

S

Serialized Quick-Turnaround-Production (SQTP) Devices ... 7

SLEEP Instruction 71

Software Simulator (MPLAB SIM) 76

Software Simulator (MPLAB SIM30) 76

Special Features of the CPU 45

Special Function Registers 17

Stack 23

Status Register 18

SUBLW Instruction 72

SUBWF Instruction 72

SWAPF Instruction 73

T

Timer0

TIMER0 31

TIMER0 (TMR0) Interrupt 31

TIMER0 (TMR0) Module 31

TMR0 with External Clock 33

Timer1

Switching Prescaler Assignment 35

Timing Diagrams and Specifications 104

TMR0 Interrupt 56

TRIS Instruction 73

TRISA 25

TRISB 28

V

Voltage Reference Module 43

VRCON Register 43

W

Watchdog Timer (WDT) 58

WWW, On-Line Support 3

X

XORLW Instruction 73

XORWF Instruction 73