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"**Embedded - Microcontrollers**" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "**Embedded - Microcontrollers**"

Details	
Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	13
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	18-DIP (0.300", 7.62mm)
Supplier Device Package	18-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lc622-04e-p

NOTES:

1.0 GENERAL DESCRIPTION

The PIC16C62X devices are 18 and 20-Pin ROM/EPROM-based members of the versatile PICmicro® family of low cost, high performance, CMOS, fully-static, 8-bit microcontrollers.

All PICmicro microcontrollers employ an advanced RISC architecture. The PIC16C62X devices have enhanced core features, eight-level deep stack, and multiple internal and external interrupt sources. The separate instruction and data buses of the Harvard architecture allow a 14-bit wide instruction word with the separate 8-bit wide data. The two-stage instruction pipeline allows all instructions to execute in a single cycle, except for program branches (which require two cycles). A total of 35 instructions (reduced instruction set) are available. Additionally, a large register set gives some of the architectural innovations used to achieve a very high performance.

PIC16C62X microcontrollers typically achieve a 2:1 code compression and a 4:1 speed improvement over other 8-bit microcontrollers in their class.

The PIC16C620A, PIC16C621A and PIC16CR620A have 96 bytes of RAM. The PIC16C622(A) has 128 bytes of RAM. Each device has 13 I/O pins and an 8-bit timer/counter with an 8-bit programmable prescaler. In addition, the PIC16C62X adds two analog comparators with a programmable on-chip voltage reference module. The comparator module is ideally suited for applications requiring a low cost analog interface (e.g., battery chargers, threshold detectors, white goods controllers, etc).

PIC16C62X devices have special features to reduce external components, thus reducing system cost, enhancing system reliability and reducing power consumption. There are four oscillator options, of which the single pin RC oscillator provides a low cost solution, the LP oscillator minimizes power consumption, XT is a standard crystal, and the HS is for High Speed crystals. The SLEEP (Power-down) mode offers power savings. The user can wake-up the chip from SLEEP through several external and internal interrupts and RESET.

A highly reliable Watchdog Timer with its own on-chip RC oscillator provides protection against software lock- up.

A UV-erasable CERDIP-packaged version is ideal for code development while the cost effective One-Time-Programmable (OTP) version is suitable for production in any volume.

Table 1-1 shows the features of the PIC16C62X mid-range microcontroller families.

A simplified block diagram of the PIC16C62X is shown in Figure 3-1.

The PIC16C62X series fits perfectly in applications ranging from battery chargers to low power remote sensors. The EPROM technology makes customization of application programs (detection levels, pulse generation, timers, etc.) extremely fast and convenient. The small footprint packages make this microcontroller series perfect for all applications with space limitations. Low cost, low power, high performance, ease of use and I/O flexibility make the PIC16C62X very versatile.

1.1 Family and Upward Compatibility

Those users familiar with the PIC16C5X family of microcontrollers will realize that this is an enhanced version of the PIC16C5X architecture. Please refer to Appendix A for a detailed list of enhancements. Code written for the PIC16C5X can be easily ported to PIC16C62X family of devices (Appendix B). The PIC16C62X family fills the niche for users wanting to migrate up from the PIC16C5X family and not needing various peripheral features of other members of the PIC16XX mid-range microcontroller family.

1.2 Development Support

The PIC16C62X family is supported by a full-featured macro assembler, a software simulator, an in-circuit emulator, a low cost development programmer and a full-featured programmer. Third Party "C" compilers are also available.

4.2.2.4 PIE1 Register

This register contains the individual enable bit for the comparator interrupt.

REGISTER 4-4: PIE1 REGISTER (ADDRESS 8CH)

U-0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0
—	CMIE	—	—	—	—	—	—

bit 7   bit 0

bit 7   **Unimplemented:** Read as '0'

bit 6   **CMIE**: Comparator Interrupt Enable bit
1 = Enables the Comparator interrupt
0 = Disables the Comparator interrupt

bit 5-0   **Unimplemented**: Read as '0'

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

4.2.2.5 PIR1 Register

This register contains the individual flag bit for the comparator interrupt.

> **Note:** Interrupt flag bits get set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 4-5: PIR1 REGISTER (ADDRESS 0CH)

U-0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0
—	CMIF	—	—	—	—	—	—

bit 7   bit 0

bit 7   **Unimplemented:** Read as '0'

bit 6   **CMIF**: Comparator Interrupt Flag bit
1 = Comparator input has changed
0 = Comparator input has not changed

bit 5-0   **Unimplemented**: Read as '0'

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

PIC16C62X

5.2   PORTB and TRISB Registers

PORTB is an 8-bit wide, bi-directional port. The corresponding data direction register is TRISB. A '1' in the TRISB register puts the corresponding output driver in a High Impedance mode. A '0' in the TRISB register puts the contents of the output latch on the selected pin(s).

Reading PORTB register reads the status of the pins, whereas writing to it will write to the port latch. All write operations are read-modify-write operations. So a write to a port implies that the port pins are first read, then this value is modified and written to the port data latch.

Each of the PORTB pins has a weak internal pull-up (≈200 μA typical). A single control bit can turn on all the pull-ups. This is done by clearing the RBPU (OPTION<7>) bit. The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on Power-on Reset.

Four of PORTB's pins, RB<7:4>, have an interrupt on change feature. Only pins configured as inputs can cause this interrupt to occur (e.g., any RB<7:4> pin configured as an output is excluded from the interrupt on change comparison). The input pins (of RB<7:4>) are compared with the old value latched on the last read of PORTB. The "mismatch" outputs of RB<7:4> are OR'ed together to generate the RBIF interrupt (flag latched in INTCON<0>).

This interrupt can wake the device from SLEEP. The user, in the interrupt service routine, can clear the interrupt in the following manner:

a)   Any read or write of PORTB. This will end the mismatch condition.

b)   Clear flag bit RBIF.

A mismatch condition will continue to set flag bit RBIF. Reading PORTB will end the mismatch condition and allow flag bit RBIF to be cleared.

This interrupt on mismatch feature, together with software configurable pull-ups on these four pins allow easy interface to a key pad and make it possible for wake-up on key-depression. (See AN552, "Implementing Wake-Up on Key Strokes.)

> **Note:** If a change on the I/O pin should occur when the read operation is being executed (start of the Q2 cycle), then the RBIF interrupt flag may not get set.

The interrupt-on-change feature is recommended for wake-up on key depression operation and operations where PORTB is only used for the interrupt on change feature. Polling of PORTB is not recommended while using the interrupt-on-change feature.

FIGURE 5-5:   BLOCK DIAGRAM OF RB<7:4> PINS

Note 1: TRISB = 1 enables weak pull-up if RBPU = '0' (OPTION<7>).

FIGURE 5-6:   BLOCK DIAGRAM OF RB<3:0> PINS

Note 1: TRISB = 1 enables weak pull-up if RBPU = '0' (OPTION<7>).

6.0   TIMER0 MODULE

The Timer0 module timer/counter has the following features:

- 8-bit timer/counter
- Readable and writable
- 8-bit software programmable prescaler
- Internal or external clock select
- Interrupt on overflow from FFh to 00h
- Edge select for external clock

Figure 6-1 is a simplified block diagram of the Timer0 module.

Timer mode is selected by clearing the T0CS bit (OPTION<5>). In Timer mode, the TMR0 will increment every instruction cycle (without prescaler). If Timer0 is written, the increment is inhibited for the following two cycles (Figure 6-2 and Figure 6-3). The user can work around this by writing an adjusted value to TMR0.

Counter mode is selected by setting the T0CS bit. In this mode, Timer0 will increment either on every rising or falling edge of pin RA4/T0CKI. The incrementing edge is determined by the source edge (T0SE) control bit (OPTION<4>). Clearing the T0SE bit selects the rising edge. Restrictions on the external clock input are discussed in detail in Section 6.2.

The prescaler is shared between the Timer0 module and the Watchdog Timer. The prescaler assignment is controlled in software by the control bit PSA (OPTION<3>). Clearing the PSA bit will assign the prescaler to Timer0. The prescaler is not readable or writable. When the prescaler is assigned to the Timer0 module, prescale value of 1:2, 1:4, ..., 1:256 are selectable. Section 6.3 details the operation of the prescaler.

6.1   TIMER0 Interrupt

Timer0 interrupt is generated when the TMR0 register timer/counter overflows from FFh to 00h. This overflow sets the T0IF bit. The interrupt can be masked by clearing the T0IE bit (INTCON<5>). The T0IF bit (INTCON<2>) must be cleared in software by the Timer0 module interrupt service routine before re-enabling this interrupt. The Timer0 interrupt cannot wake the processor from SLEEP, since the timer is shut off during SLEEP. See Figure 6-4 for Timer0 interrupt timing.
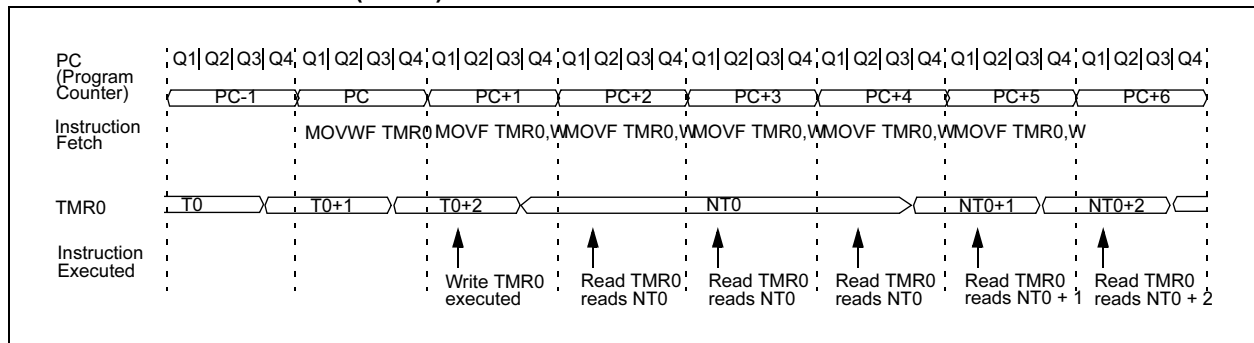
FIGURE 6-1:   **TIMER0 BLOCK DIAGRAM**

    Note 1:   Bits T0SE, T0CS, PS2, PS1, PS0 and PSA are located in the OPTION register.
          2:   The prescaler is shared with Watchdog Timer (Figure 6-6).
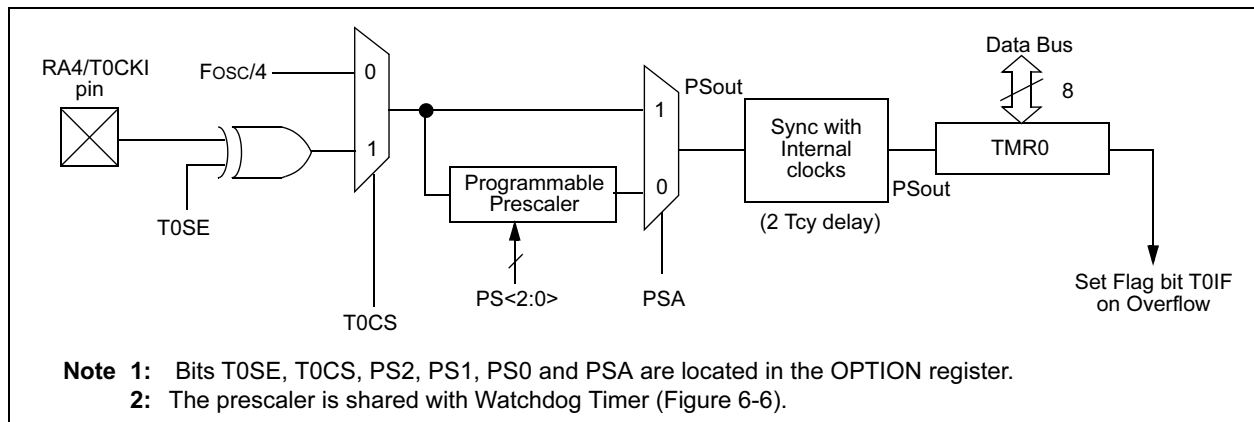
FIGURE 6-2:   **TIMER0 (TMR0) TIMING: INTERNAL CLOCK/NO PRESCALER**

PIC16C62X

6.3   Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module, or as a postscaler for the Watchdog Timer, respectively (Figure 6-6). For simplicity, this counter is being referred to as "prescaler" throughout this data sheet. Note that there is only one prescaler available which is mutually exclusive between the Timer0 module and the Watchdog Timer. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the Watchdog Timer and vice-versa.

The PSA and PS<2:0> bits (OPTION<3:0>) determine the prescaler assignment and prescale ratio.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., `CLRF 1`, `MOVWF 1`, `BSF 1,x`....etc.) will clear the prescaler. When assigned to WDT, a `CLRWDT` instruction will clear the prescaler along with the Watchdog Timer. The prescaler is not readable or writable.

FIGURE 6-6:   **BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER**

Note: T0SE, T0CS, PSA, PS<2:0> are bits in the OPTION register.
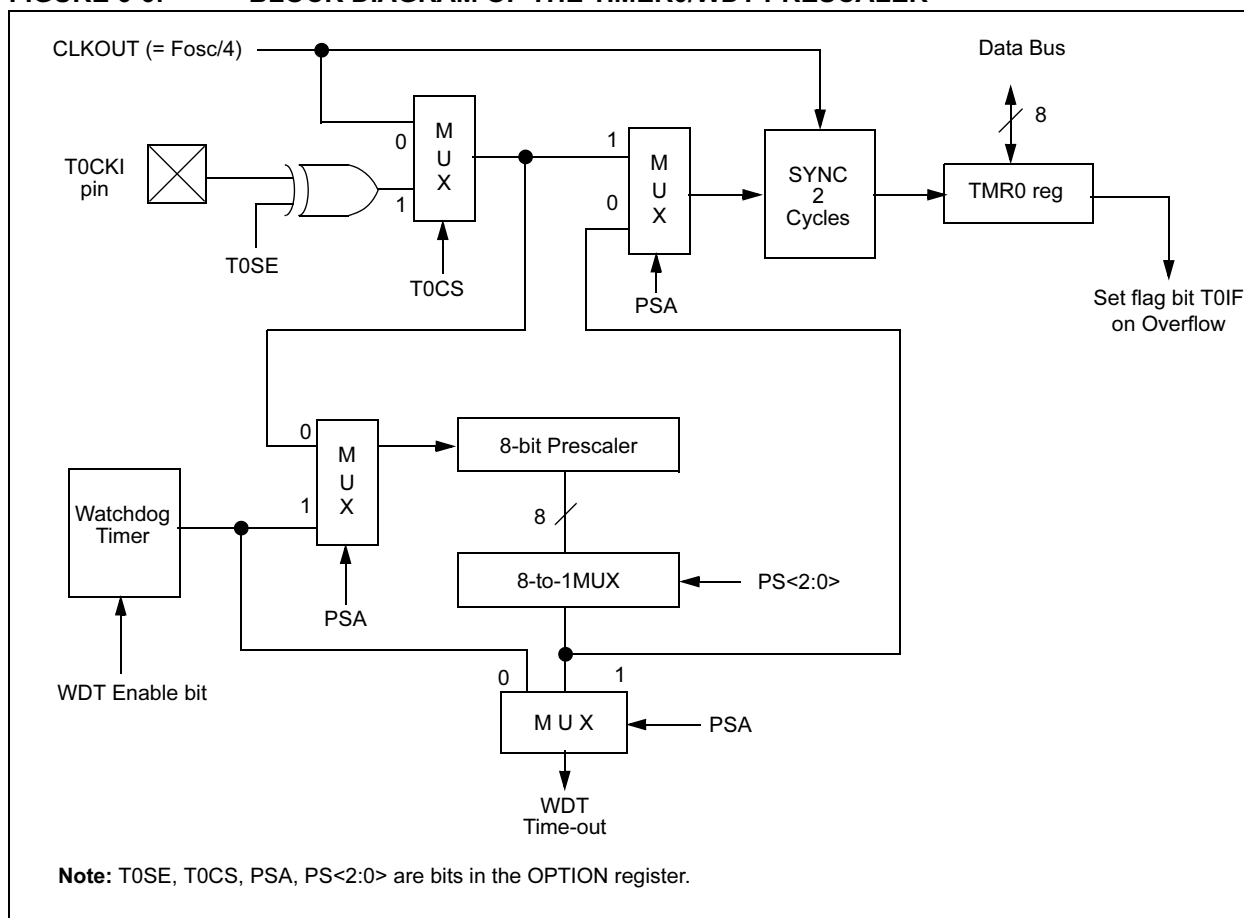
7.6 Comparator Interrupts

The comparator interrupt flag is set whenever there is a change in the output value of either comparator. Software will need to maintain information about the status of the output bits, as read from CMCON<7:6>, to determine the actual change that has occurred. The CMIF bit, PIR1<6>, is the comparator interrupt flag. The CMIF bit must be RESET by clearing '0'. Since it is also possible to write a '1' to this register, a simulated interrupt may be initiated.

The CMIE bit (PIE1<6>) and the PEIE bit (INTCON<6>) must be set to enable the interrupt. In addition, the GIE bit must also be set. If any of these bits are clear, the interrupt is not enabled, though the CMIF bit will still be set if an interrupt condition occurs.

> **Note:** If a change in the CMCON register (C1OUT or C2OUT) should occur when a read operation is being executed (start of the Q2 cycle), then the CMIF (PIR1<6>) interrupt flag may not get set.

The user, in the interrupt service routine, can clear the interrupt in the following manner:

a) Any read or write of CMCON. This will end the mismatch condition.

b) Clear flag bit CMIF.

A mismatch condition will continue to set flag bit CMIF. Reading CMCON will end the mismatch condition and allow flag bit CMIF to be cleared.

7.7 Comparator Operation During SLEEP

When a comparator is active and the device is placed in SLEEP mode, the comparator remains active and the interrupt is functional if enabled. This interrupt will wake up the device from SLEEP mode when enabled. While the comparator is powered-up, higher SLEEP currents than shown in the power-down current specification will occur. Each comparator that is operational will consume additional current as shown in the comparator specifications. To minimize power consumption while in SLEEP mode, turn off the comparators, CM<2:0> = 111, before entering SLEEP. If the device wakes up from SLEEP, the contents of the CMCON register are not affected.
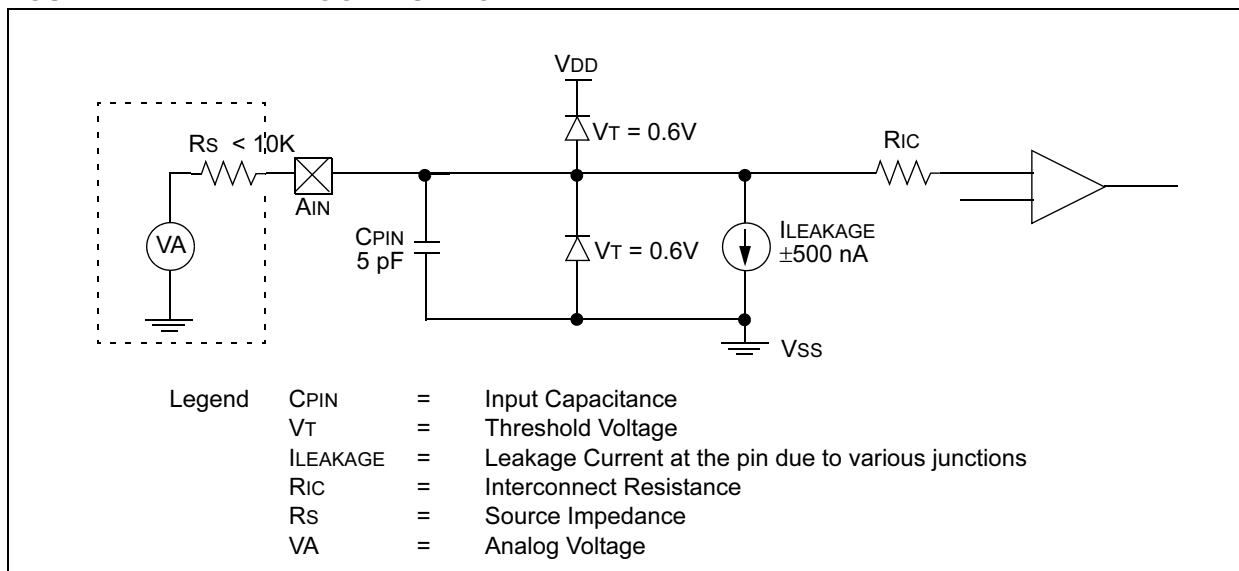
7.8 Effects of a RESET

A device RESET forces the CMCON register to its RESET state. This forces the comparator module to be in the comparator RESET mode, CM<2:0> = 000. This ensures that all potential inputs are analog inputs. Device current is minimized when analog inputs are present at RESET time. The comparators will be powered-down during the RESET interval.

7.9 Analog Input Connection Considerations

A simplified circuit for an analog input is shown in Figure 7-4. Since the analog pins are connected to a digital output, they have reverse biased diodes to VDD and VSS. The analog input therefore, must be between VSS and VDD. If the input voltage deviates from this range by more than 0.6V in either direction, one of the diodes is forward biased and a latchup may occur. A maximum source impedance of 10 kΩ is recommended for the analog sources. Any external component connected to an analog input pin, such as a capacitor or a Zener diode, should have very little leakage current.

FIGURE 7-4:   ANALOG INPUT MODEL

Legend	CPIN	=	Input Capacitance
	VT	=	Threshold Voltage
	ILEAKAGE	=	Leakage Current at the pin due to various junctions
	RIC	=	Interconnect Resistance
	RS	=	Source Impedance
	VA	=	Analog Voltage

9.0   SPECIAL FEATURES OF THE CPU

Special circuits to deal with the needs of real-time applications are what sets a microcontroller apart from other processors. The PIC16C62X family has a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection.

These are:

1. OSC selection
2. RESET
   Power-on Reset (POR)
   Power-up Timer (PWRT)
   Oscillator Start-up Timer (OST)
   Brown-out Reset (BOR)
3. Interrupts
4. Watchdog Timer (WDT)
5. SLEEP
6. Code protection
7. ID Locations
8. In-Circuit Serial Programming™

The PIC16C62X devices have a Watchdog Timer which is controlled by configuration bits. It runs off its own RC oscillator for added reliability. There are two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in RESET until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay of 72 ms (nominal) on power-up only, designed to keep the part in RESET while the power supply stabilizes. There is also circuitry to RESET the device if a brown-out occurs, which provides at least a 72 ms RESET. With these three functions on-chip, most applications need no external RESET circuitry.

The SLEEP mode is designed to offer a very low current Power-down mode. The user can wake-up from SLEEP through external RESET, Watchdog Timer wake-up or through an interrupt. Several oscillator options are also made available to allow the part to fit the application. The RC oscillator option saves system cost, while the LP crystal option saves power. A set of configuration bits are used to select various options.

9.3 RESET

The PIC16C62X differentiates between various kinds of RESET:

a) Power-on Reset (POR)

b) MCLR Reset during normal operation

c) MCLR Reset during SLEEP

d) WDT Reset (normal operation)

e) WDT wake-up (SLEEP)

f) Brown-out Reset (BOR)

Some registers are not affected in any RESET condition Their status is unknown on POR and unchanged in any other RESET. Most other registers are reset to a "RESET state" on Power-on Reset, MCLR Reset, WDT Reset and MCLR Reset during SLEEP. They are not affected by a WDT wake-up, since this is viewed as the resumption of normal operation. TO and PD bits are set or cleared differently in different RESET situations as indicated in Table 9-2. These bits are used in software to determine the nature of the RESET. See Table 9-5 for a full description of RESET states of all registers.

A simplified block diagram of the on-chip RESET circuit is shown in Figure 9-6.

The MCLR Reset path has a noise filter to detect and ignore small pulses. See Table 12-5 for pulse width specification.

**FIGURE 9-6:** SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT

Note 1: This is a separate oscillator from the RC oscillator of the CLKIN pin.
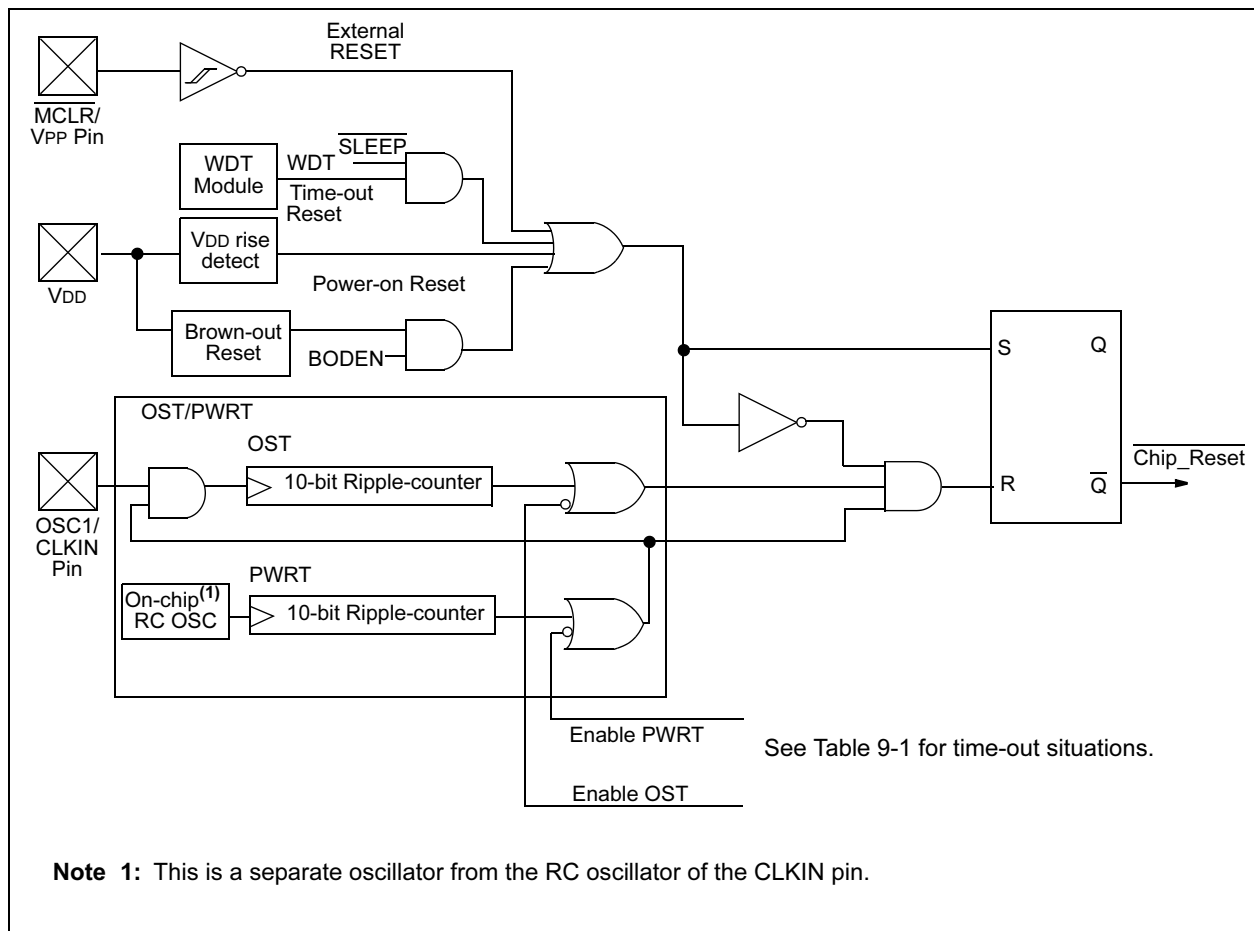
PIC16C62X

FIGURE 9-11: **EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW V$_{DD}$ POWER-UP)**

V$_{DD}$ V$_{DD}$

R   D

R1

$\overline{MCLR}$

C   **PIC16C62X**
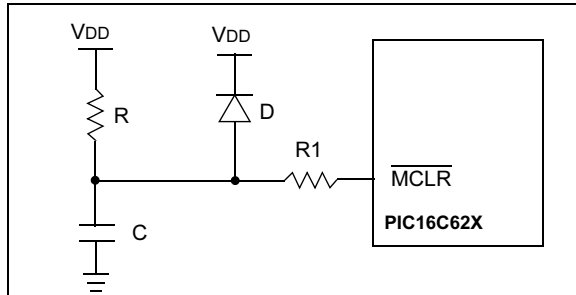
Note 1: External Power-on Reset circuit is required only if V$_{DD}$ power-up slope is too slow. The diode D helps discharge the capacitor quickly when V$_{DD}$ powers down.

2: < 40 kΩ is recommended to make sure that voltage drop across R does not violate the device's electrical specification.

3: R1 = 100Ω to 1 kΩ will limit any current flowing into $\overline{MCLR}$ from external capacitor C in the event of $\overline{MCLR}$/V$_{PP}$ pin breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).

FIGURE 9-12: **EXTERNAL BROWN-OUT PROTECTION CIRCUIT 1**

V$_{DD}$

V$_{DD}$

33k

10k

$\overline{MCLR}$

40k   **PIC16C62X**
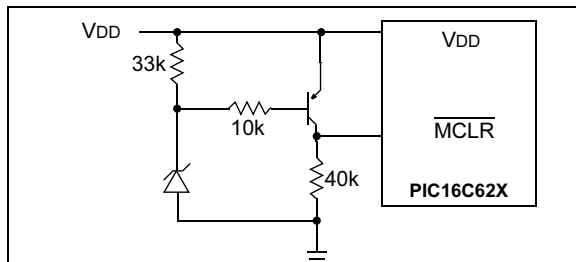
Note 1: This circuit will activate RESET when V$_{DD}$ goes below (Vz + 0.7V) where Vz = Zener voltage.

2: Internal Brown-out Reset circuitry should be disabled when using this circuit.

FIGURE 9-13: **EXTERNAL BROWN-OUT PROTECTION CIRCUIT 2**

V$_{DD}$ V$_{DD}$

R1

Q1

$\overline{MCLR}$

R2   40k   **PIC16C62X**
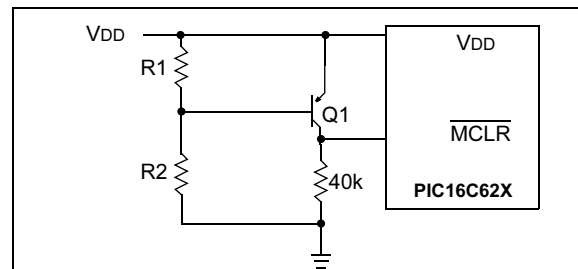
Note 1: This brown-out circuit is less expensive, albeit less accurate. Transistor Q1 turns off when V$_{DD}$ is below a certain level such that:

$$V_{DD} \times \frac{R1}{R1 + R2} = 0.7V$$

2: Internal Brown-out Reset should be disabled when using this circuit.

3: Resistors should be adjusted for the characteristics of the transistor.

FIGURE 9-14: **EXTERNAL BROWN-OUT PROTECTION CIRCUIT 3**

V$_{DD}$

MCP809   bypass capacitor   V$_{DD}$

Vss

V$_{DD}$

$\overline{RST}$ $\overline{MCLR}$

PIC16C62X
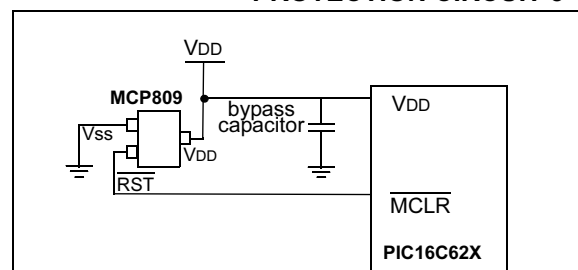
This brown-out protection circuit employs Microchip Technology's MCP809 microcontroller supervisor. The MCP8XX and MCP1XX families of supervisors provide push-pull and open collector outputs with both high and low active RESET pins. There are 7 different trip point selections to accommodate 5V and 3V systems.

9.7 Watchdog Timer (WDT)

The Watchdog Timer is a free running on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the RC oscillator of the CLKIN pin. That means that the WDT will run, even if the clock on the OSC1 and OSC2 pins of the device has been stopped, for example, by execution of a SLEEP instruction. During normal operation, a WDT time-out generates a device RESET. If the device is in SLEEP mode, a WDT time-out causes the device to wake-up and continue with normal operation. The WDT can be permanently disabled by programming the configuration bit WDTE as clear (Section 9.1).

9.7.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms, (with no prescaler). The time-out periods vary with temperature, VDD and process variations from part to part (see DC specs). If longer time-out periods are desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT under software control by writing to the OPTION register. Thus, time-out periods up to 2.3 seconds can be realized.

The CLRWDT and SLEEP instructions clear the WDT and the postscaler, if assigned to the WDT, and prevent it from timing out and generating a device RESET.

The $\overline{TO}$ bit in the STATUS register will be cleared upon a Watchdog Timer time-out.

9.7.2 WDT PROGRAMMING CONSIDERATIONS

It should also be taken in account that under worst case conditions (VDD = Min., Temperature = Max., max. WDT prescaler) it may take several seconds before a WDT time-out occurs.

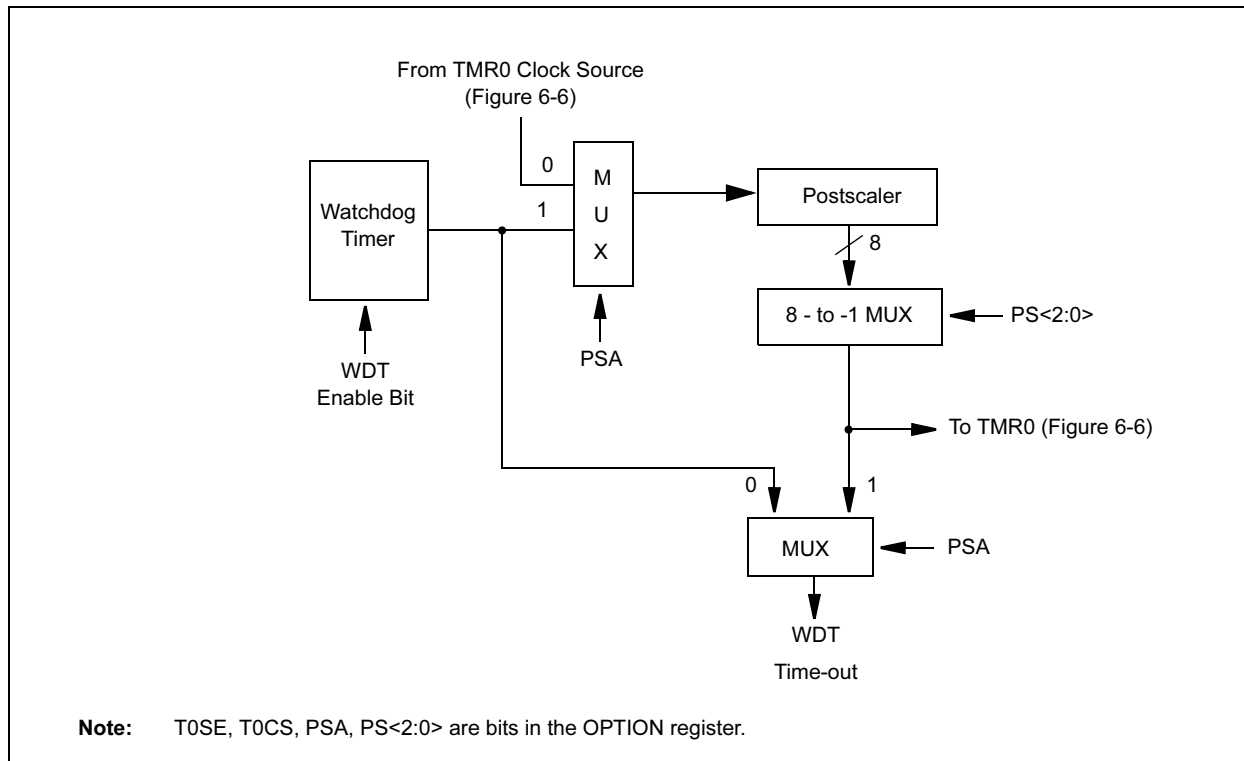**FIGURE 9-17: WATCHDOG TIMER BLOCK DIAGRAM**

Note: T0SE, T0CS, PSA, PS<2:0> are bits in the OPTION register.

TABLE 9-7: SUMMARY OF WATCHDOG TIMER REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR Reset	Value on all other RESETS
2007h	Config. bits	—	BODEN	CP1	CP0	PWRTE	WDTE	FOSC1	FOSC0	—	—
81h	OPTION	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111

Legend: Shaded cells are not used by the Watchdog Timer.

Note: — = Unimplemented location, read as "0"
      + = Reserved for future use

10.0   INSTRUCTION SET SUMMARY

Each PIC16C62X instruction is a 14-bit word divided into an OPCODE which specifies the instruction type and one or more operands which further specify the operation of the instruction. The PIC16C62X instruction set summary in Table 10-2 lists **byte-oriented**, **bit-oriented,** and **literal and control** operations. Table 10-1 shows the opcode field descriptions.

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator specifies which file register is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is zero, the result is placed in the W register. If 'd' is one, the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator which selects the number of the bit affected by the operation, while 'f' represents the number of the file in which the bit is located.

For **literal and control** operations, 'k' represents an eight or eleven bit constant or literal value.

TABLE 10-1:   OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1) The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0: store result in W, d = 1: store result in file register f. Default is d = 1
label	Label name
TOS	Top of Stack
PC	Program Counter
PCLATH	Program Counter High Latch
GIE	Global Interrupt Enable bit
WDT	Watchdog Timer/Counter
TO	Time-out bit
PD	Power-down bit
dest	Destination either the W register or the specified register file location
[ ]	Options
( )	Contents
→	Assigned to
< >	Register bit field
∈	In the set of
italics	User defined term (font is courier)

The instruction set is highly orthogonal and is grouped into three basic categories:

- **Byte-oriented** operations
- **Bit-oriented** operations
- **Literal and control** operations

All instructions are executed within one single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles with the second cycle executed as a NOP. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 μs. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time is 2 μs.

Table 10-1 lists the instructions recognized by the MPASM™ assembler.

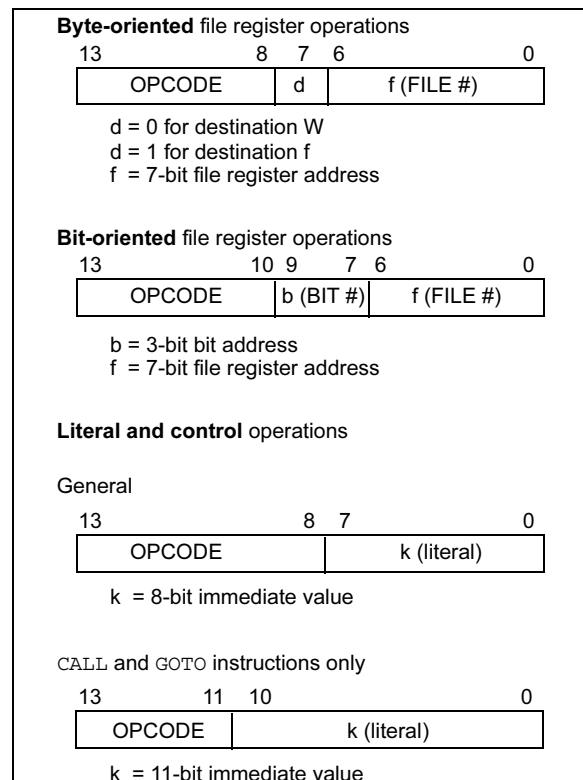Figure 10-1 shows the three general formats that the instructions can have.

> **Note:** To maintain upward compatibility with future PICmicro® products, <u>do not use</u> the OPTION and TRIS instructions.

All examples use the following format to represent a hexadecimal number:

0xhh

where h signifies a hexadecimal digit.

FIGURE 10-1:   GENERAL FORMAT FOR INSTRUCTIONS

Byte-oriented file register operations

13		8	7	6		0
OPCODE			d	f (FILE #)		

d = 0 for destination W
d = 1 for destination f
f = 7-bit file register address

Bit-oriented file register operations

13		10	9	7	6		0
OPCODE			b (BIT #)		f (FILE #)		

b = 3-bit bit address
f = 7-bit file register address

Literal and control operations

General

13		8	7		0
OPCODE			k (literal)		

k = 8-bit immediate value

CALL and GOTO instructions only

13		11	10		0
OPCODE			k (literal)		

k = 11-bit immediate value

MOVF   **Move f**

Syntax:	[*label*] MOVF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	(f) $\rightarrow$ (dest)
Status Affected:	Z

Encoding:

00	1000	dfff	ffff

Description:	The contents of register f is moved to a destination dependent upon the status of d. If d = 0, destination is W register. If d = 1, the destination is file register f itself. d = 1 is useful to test a file register since status flag Z is affected.
Words:	1
Cycles:	1
Example	MOVF FSR, 0

After Instruction
     W   =   value in FSR register
     Z   =   1

MOVWF   **Move W to f**

Syntax:	[*label*] MOVWF f
Operands:	$0 \leq f \leq 127$
Operation:	(W) $\rightarrow$ (f)
Status Affected:	None

Encoding:

00	0000	1fff	ffff

Description:	Move data from W register to register 'f'.
Words:	1
Cycles:	1
Example	MOVWF OPTION

Before Instruction
     OPTION =   0xFF
     W   =   0x4F
After Instruction
     OPTION =   0x4F
     W   =   0x4F

NOP   **No Operation**

Syntax:	[*label*] NOP
Operands:	None
Operation:	No operation
Status Affected:	None

Encoding:

00	0000	0xx0	0000

Description:	No operation.
Words:	1
Cycles:	1
Example	NOP

OPTION   **Load Option Register**

Syntax:	[*label*] OPTION
Operands:	None
Operation:	(W) $\rightarrow$ OPTION
Status Affected:	None

Encoding:

00	0000	0110	0010

Description:	The contents of the W register are loaded in the OPTION register. This instruction is supported for code compatibility with PIC16C5X products. Since OPTION is a readable/writable register, the user can directly address it.
Words:	1
Cycles:	1
Example	

To maintain upward compatibility with future PICmicro® products, do not use this instruction.

PIC16C62X

FIGURE 12-5: **PIC16LC620A/LC621A/LC622A VOLTAGE-FREQUENCY GRAPH,**
-40°C ≤ TA ≤ 0°C

Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

     2: The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.
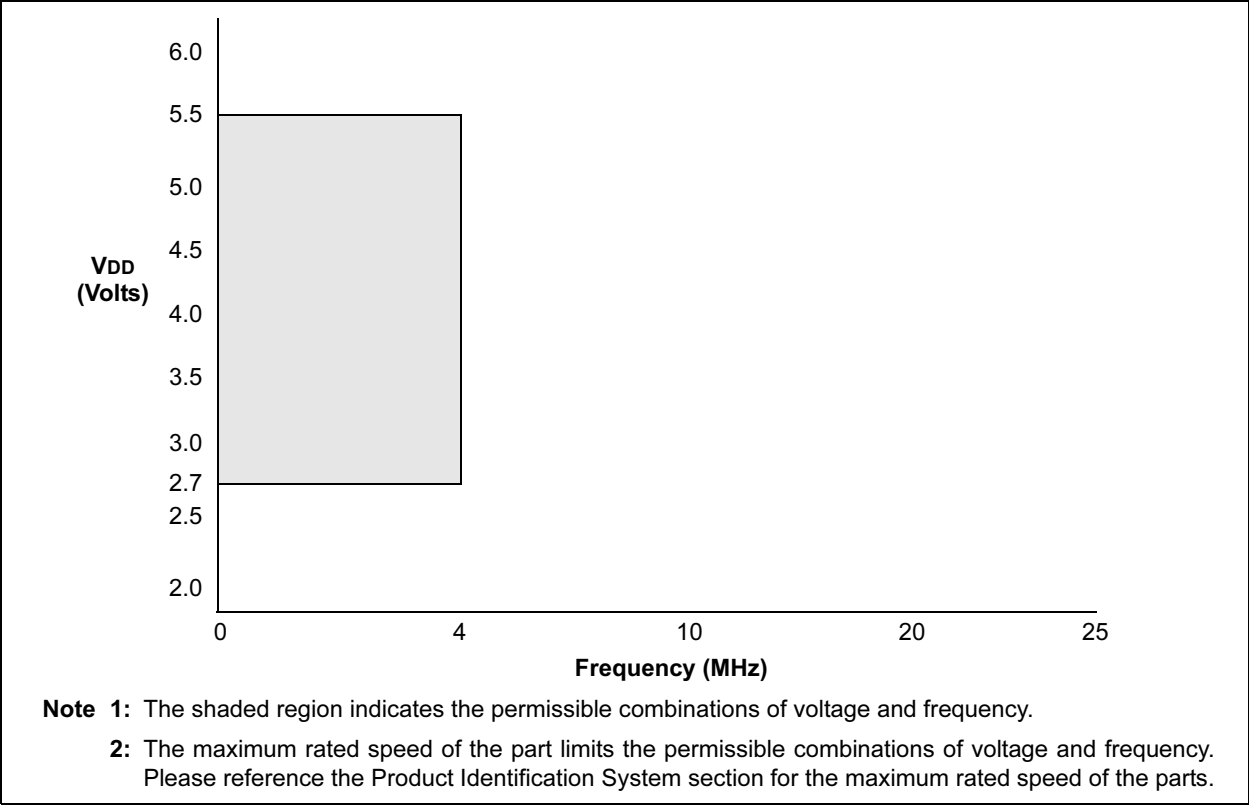
FIGURE 12-6: **PIC16LC620A/LC621A/LC622A VOLTAGE-FREQUENCY GRAPH,**
0°C ≤ TA ≤ +125°C

Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

     2: The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.
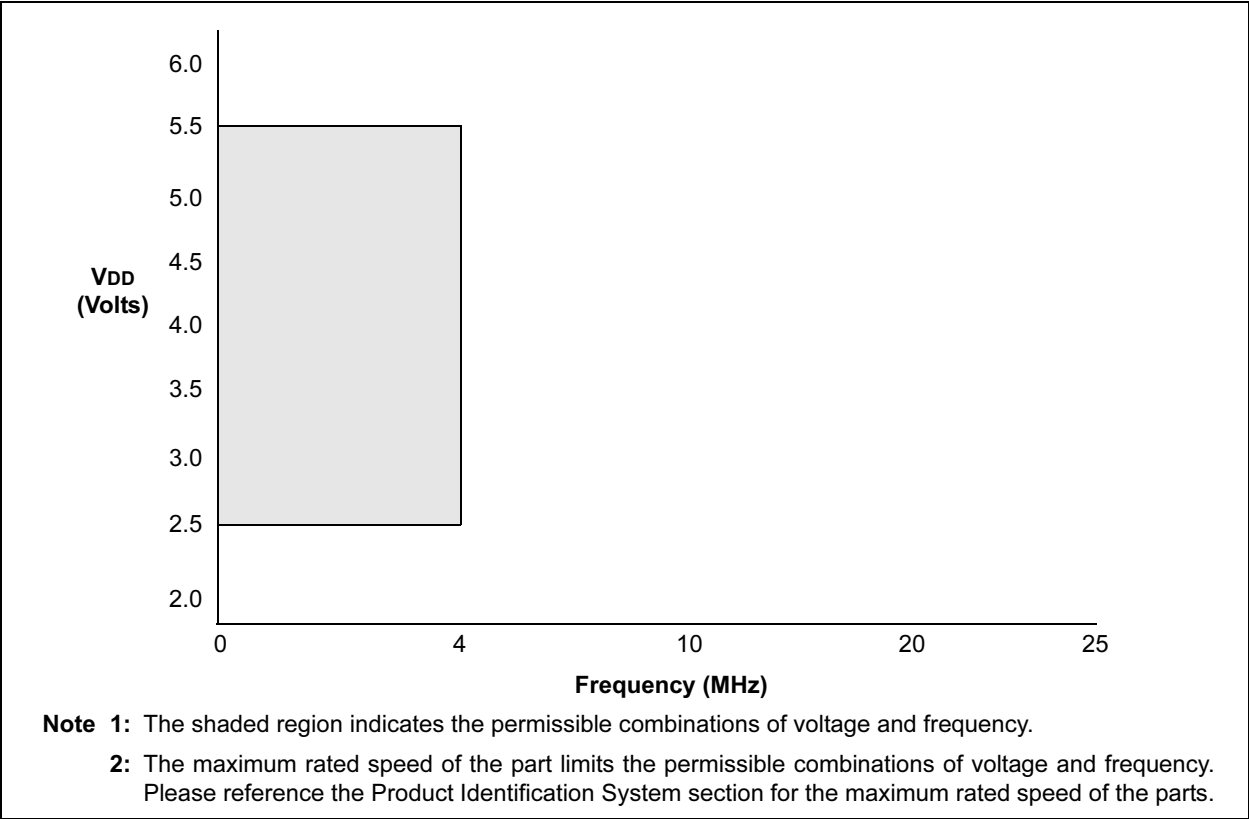
PIC16C62X

FIGURE 12-9: **PIC16LCR62XA VOLTAGE-FREQUENCY GRAPH, -40°C ≤ TA ≤ +125°C**

Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

2: The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.
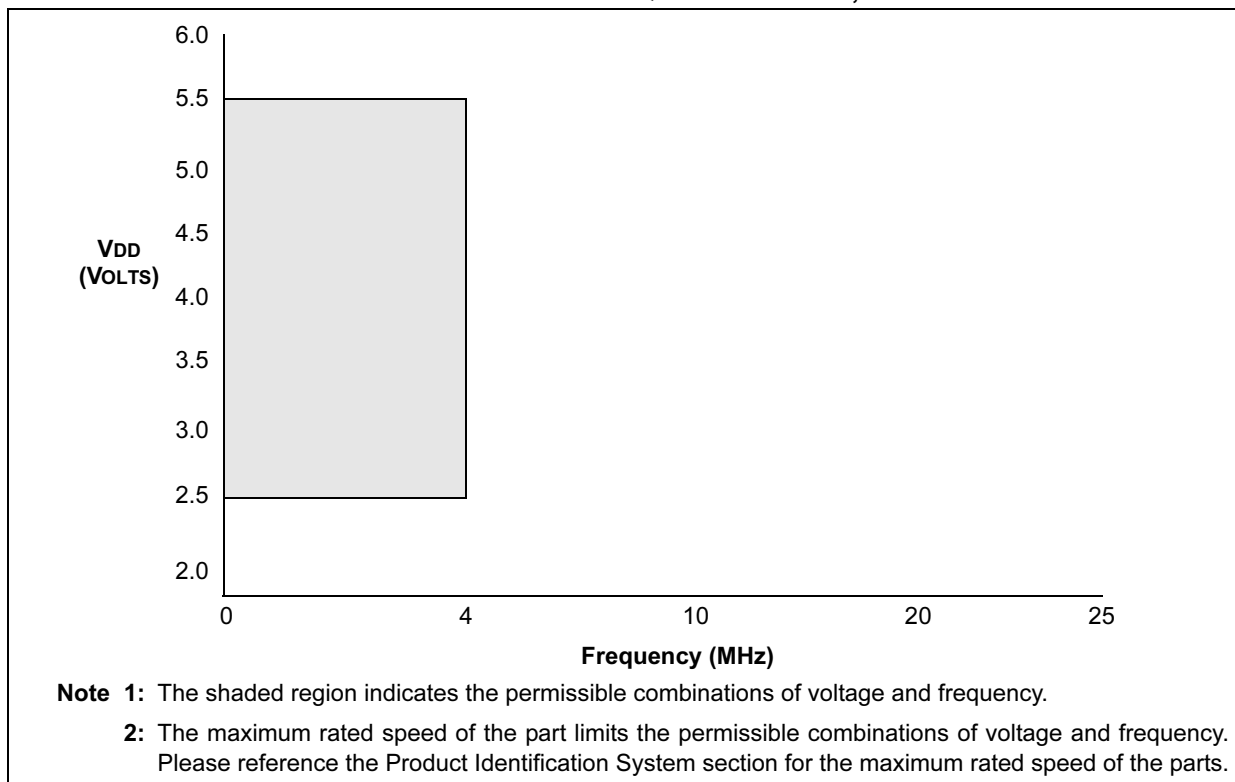
PIC16C62X

12.4   DC Characteristics: PIC16C62X/C62XA/CR62XA (Commercial, Industrial, Extended)
PIC16LC62X/LC62XA/LCR62XA (Commercial, Industrial, Extended)

PIC16C62X/C62XA/CR62XA	Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial and -40°C ≤ TA ≤ +125°C for extended
PIC16LC62X/LC62XA/LCR62XA	Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial and -40°C ≤ TA ≤ +125°C for extended

Param. No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	V$_{IL}$	**Input Low Voltage**					
		I/O ports					
D030		with TTL buffer	Vss	—	0.8V 0.15 V$_{DD}$	V	V$_{DD}$ = 4.5V to 5.5V otherwise
D031		with Schmitt Trigger input	Vss	—	0.2 V$_{DD}$	V	
D032		$\overline{MCLR}$, RA4/T0CKI,OSC1 (in RC mode)	Vss	—	0.2 V$_{DD}$	V	**(Note 1)**
D033		OSC1 (in XT and HS)	Vss	—	0.3 V$_{DD}$	V	
		OSC1 (in LP)	Vss	—	0.6 V$_{DD}$-1.0	V	
	V$_{IL}$	**Input Low Voltage**					
		I/O ports					
D030		with TTL buffer	Vss	—	0.8V 0.15 V$_{DD}$	V	V$_{DD}$ = 4.5V to 5.5V otherwise
D031		with Schmitt Trigger input	Vss	—	0.2 V$_{DD}$	V	
D032		$\overline{MCLR}$, RA4/T0CKI,OSC1 (in RC mode)	Vss	—	0.2 V$_{DD}$	V	**(Note 1)**
D033		OSC1 (in XT and HS)	Vss	—	0.3 V$_{DD}$	V	
		OSC1 (in LP)	Vss	—	0.6 V$_{DD}$-1.0	V	
	V$_{IH}$	Input High Voltage					
		I/O ports					
D040		with TTL buffer	2.0V 0.25 V$_{DD}$ + 0.8V	—	V$_{DD}$ V$_{DD}$	V	V$_{DD}$ = 4.5V to 5.5V otherwise
D041		with Schmitt Trigger input	0.8 V$_{DD}$	—	V$_{DD}$		
D042		$\overline{MCLR}$ RA4/T0CKI	0.8 V$_{DD}$	—	V$_{DD}$	V	
D043		OSC1 (XT, HS and LP)	0.7 V$_{DD}$	—	V$_{DD}$	V	
D043A		OSC1 (in RC mode)	0.9 V$_{DD}$				**(Note 1)**

*   These parameters are characterized but not tested.

†   Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1 pin is a Schmitt Trigger input. It is not recommended that the PIC16C62X(A) be driven with external clock in RC mode.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

PIC16C62X

12.5 DC CHARACTERISTICS: PIC16C620A/C621A/C622A-40[7] (Commercial)
PIC16CR620A-40[7] (Commercial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated)					
			Operating temperature 0°C ≤ TA ≤ +70°C for commercial					
Param No.	Sym	Characteristic	Min	Typ†	Max	Unit	Conditions	
	VIL	**Input Low Voltage**						
		I/O ports						
D030		with TTL buffer	VSS	—	0.8V 0.15VDD	V	VDD = 4.5V to 5.5V, otherwise	
D031		with Schmitt Trigger input	VSS		0.2VDD	V		
D032		MCLR, RA4/T0CKI, OSC1 (in RC mode)	VSS	—	0.2VDD	V	**(Note 1)**	
D033		OSC1 (in XT and HS)	VSS	—	0.3VDD	V		
		OSC1 (in LP)	VSS	—	0.6VDD - 1.0	V		
	VIH	**Input High Voltage**						
		I/O ports						
D040		with TTL buffer	2.0V 0.25 VDD + 0.8	—	VDD VDD	V	VDD = 4.5V to 5.5V, otherwise	
D041		with Schmitt Trigger input	0.8 VDD		VDD			
D042		MCLR RA4/T0CKI	0.8 VDD	—	VDD	V		
D043		OSC1 (XT, HS and LP)	0.7 VDD	—	VDD	V		
D043A		OSC1 (in RC mode)	0.9 VDD				**(Note 1)**	
D070	IPURB	**PORTB Weak Pull-up Current**	50	200	400	µA	VDD = 5.0V, VPIN = VSS	
	IIL	**Input Leakage Current**[2, 3]						
		I/O ports (except PORTA)			±1.0	µA	VSS ≤ VPIN ≤ VDD, pin at hi-impedance	
D060		PORTA	—	—	±0.5	µA	VSS ≤ VPIN ≤ VDD, pin at hi-impedance	
D061		RA4/T0CKI	—	—	±1.0	µA	VSS ≤ VPIN ≤ VDD	
D063		OSC1, MCLR	—	—	±5.0	µA	VSS ≤ VPIN ≤ VDD, XT, HS and LP OSC configuration	
	VOL	**Output Low Voltage**						
D080		I/O ports	—	—	0.6	V	IOL = 8.5 mA, VDD = 4.5V, -40° to +85°C	
			—	—	0.6	V	IOL = 7.0 mA, VDD = 4.5V, +125°C	
D083		OSC2/CLKOUT (RC only)	—	—	0.6	V	IOL = 1.6 mA, VDD = 4.5V, -40° to +85°C	
			—	—	0.6	V	IOL = 1.2 mA, VDD = 4.5V, +125°C	
	VOH	**Output High Voltage**[3]						
D090		I/O ports (except RA4)	VDD-0.7	—	—	V	IOH = -3.0 mA, VDD = 4.5V, -40° to +85°C	
			VDD-0.7	—	—	V	IOH = -2.5 mA, VDD = 4.5V, +125°C	
D092		OSC2/CLKOUT (RC only)	VDD-0.7	—	—	V	IOH = -1.3 mA, VDD = 4.5V, -40° to +85°C	
			VDD-0.7	—	—	V	IOH = -1.0 mA, VDD = 4.5V, +125°C	
*D150	VOD	**Open Drain High Voltage**			8.5	V	RA4 pin	
		Capacitive Loading Specs on Output Pins						
D100	COSC2	OSC2 pin			15	pF	In XT, HS and LP modes when external clock used to drive OSC1.	
D101	CIO	All I/O pins/OSC2 (in RC mode)			50	pF		

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in Active Operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD, MCLR = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or VSS.

4: For RC OSC configuration, current through REXT is not included. The current through the resistor can be estimated by the formula Ir = VDD/2REXT (mA) with REXT in kΩ.

5: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

6: Commercial temperature range only.

7: See Section 12.1 and Section 12.3 for 16C62X and 16CR62X devices for operation between 20 MHz and 40 MHz for valid modified characteristics.

18-Lead Plastic Small Outline (SO) – Wide, 300 mil (SOIC)
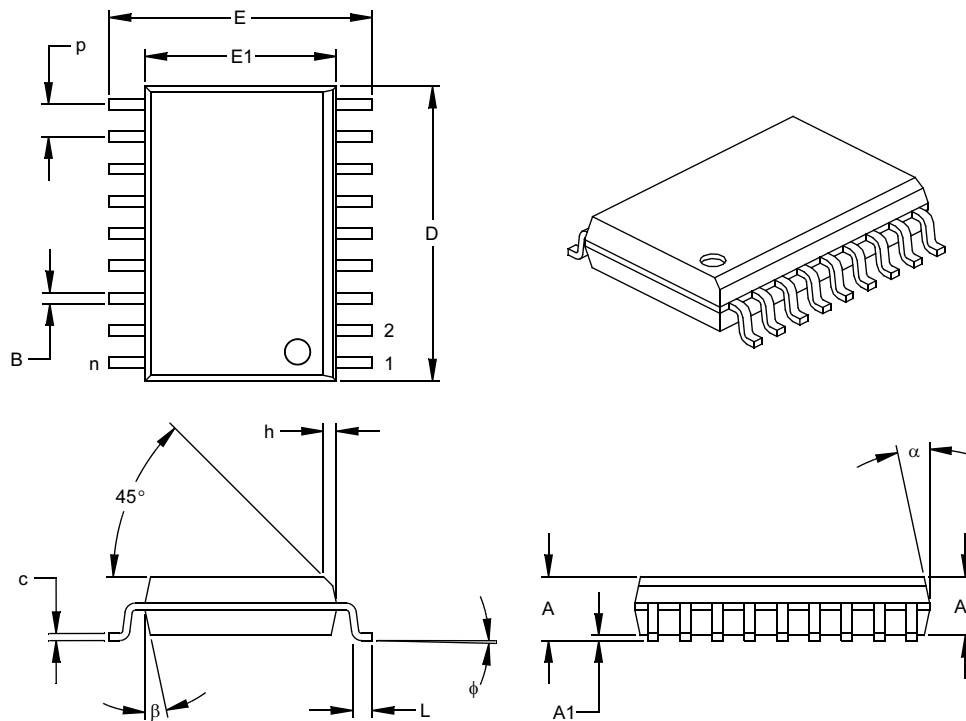
	Units	INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		18			18	
Pitch	p		.050			1.27	
Overall Height	A	.093	.099	.104	2.36	2.50	2.64
Molded Package Thickness	A2	.088	.091	.094	2.24	2.31	2.39
Standoff §	A1	.004	.008	.012	0.10	0.20	0.30
Overall Width	E	.394	.407	.420	10.01	10.34	10.67
Molded Package Width	E1	.291	.295	.299	7.39	7.49	7.59
Overall Length	D	.446	.454	.462	11.33	11.53	11.73
Chamfer Distance	h	.010	.020	.029	0.25	0.50	0.74
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.009	.011	.012	0.23	0.27	0.30
Lead Width	B	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
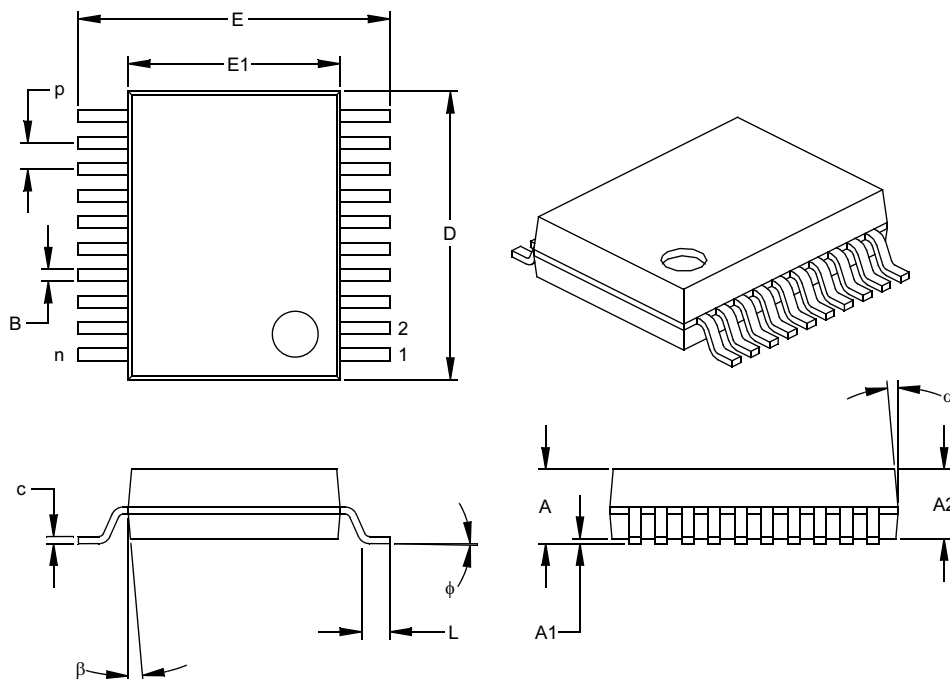§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed
.010" (0.254mm) per side.
JEDEC Equivalent: MS-013
Drawing No. C04-051

PIC16C62X

20-Lead Plastic Shrink Small Outline (SS) – 209 mil, 5.30 mm (SSOP)

Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		20			20	
Pitch	p		.026			0.65	
Overall Height	A	.068	.073	.078	1.73	1.85	1.98
Molded Package Thickness	A2	.064	.068	.072	1.63	1.73	1.83
Standoff §	A1	.002	.006	.010	0.05	0.15	0.25
Overall Width	E	.299	.309	.322	7.59	7.85	8.18
Molded Package Width	E1	.201	.207	.212	5.11	5.25	5.38
Overall Length	D	.278	.284	.289	7.06	7.20	7.34
Foot Length	L	.022	.030	.037	0.56	0.75	0.94
Lead Thickness	c	.004	.007	.010	0.10	0.18	0.25
Foot Angle	φ	0	4	8	0.00	101.60	203.20
Lead Width	B	.010	.013	.015	0.25	0.32	0.38
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed
.010" (0.254mm) per side.
JEDEC Equivalent: MO-150
Drawing No. C04-072

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