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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	13
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	18-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lc622-04e-so

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NOTES:

3.0   ARCHITECTURAL OVERVIEW

The high performance of the PIC16C62X family can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC16C62X uses a Harvard architecture, in which, program and data are accessed from separate memories using separate busses. This improves bandwidth over traditional von Neumann architecture, where program and data are fetched from the same memory. Separating program and data memory further allows instructions to be sized differently than 8-bit wide data word. Instruction opcodes are 14-bits wide making it possible to have all single word instructions. A 14-bit wide program memory access bus fetches a 14-bit instruction in a single cycle. A two-stage pipeline overlaps fetch and execution of instructions. Consequently, all instructions (35) execute in a single cycle (200 ns @ 20 MHz) except for program branches.

The PIC16C620(A) and PIC16CR620A address 512 x 14 on-chip program memory. The PIC16C621(A) addresses 1K x 14 program memory. The PIC16C622(A) addresses 2K x 14 program memory. All program memory is internal.

The PIC16C62X can directly or indirectly address its register files or data memory. All special function registers including the program counter are mapped in the data memory. The PIC16C62X has an orthogonal (symmetrical) instruction set that makes it possible to carry out any operation on any register using any Addressing mode. This symmetrical nature and lack of 'special optimal situations' make programming with the PIC16C62X simple yet efficient. In addition, the learning curve is reduced significantly.

The PIC16C62X devices contain an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between data in the working register and any register file.

The ALU is 8-bits wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. In two-operand instructions, typically one operand is the working register (W register). The other operand is a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC), and Zero (Z) bits in the STATUS register. The C and DC bits operate as a Borrow and Digit Borrow out bit, respectively, bit in subtraction. See the SUBLW and SUBWF instructions for examples.

A simplified block diagram is shown in Figure 3-1, with a description of the device pins in Table 3-1.

4.0   MEMORY ORGANIZATION

4.1   Program Memory Organization

The PIC16C62X has a 13-bit program counter capable of addressing an 8K x 14 program memory space. Only the first 512 x 14 (0000h - 01FFh) for the PIC16C620(A) and PIC16CR620, 1K x 14 (0000h - 03FFh) for the PIC16C621(A) and 2K x 14 (0000h - 07FFh) for the PIC16C622(A) are physically implemented. Accessing a location above these boundaries will cause a wrap-around within the first 512 x 14 space (PIC16C(R)620(A)) or 1K x 14 space (PIC16C621(A)) or 2K x 14 space (PIC16C622(A)). The RESET vector is at 0000h and the interrupt vector is at 0004h (Figure 4-1, Figure 4-2, Figure 4-3).

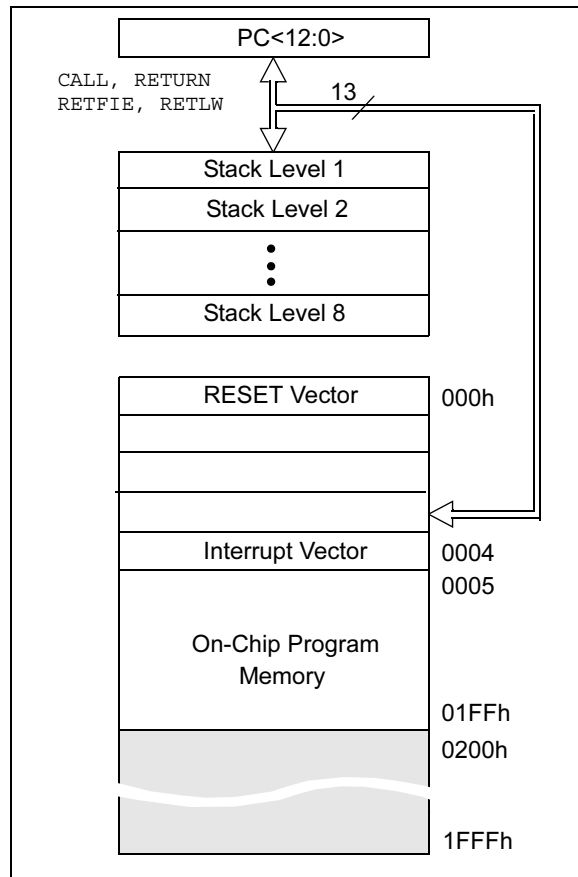**FIGURE 4-1:   PROGRAM MEMORY MAP AND STACK FOR THE PIC16C620/PIC16C620A/ PIC16CR620A**

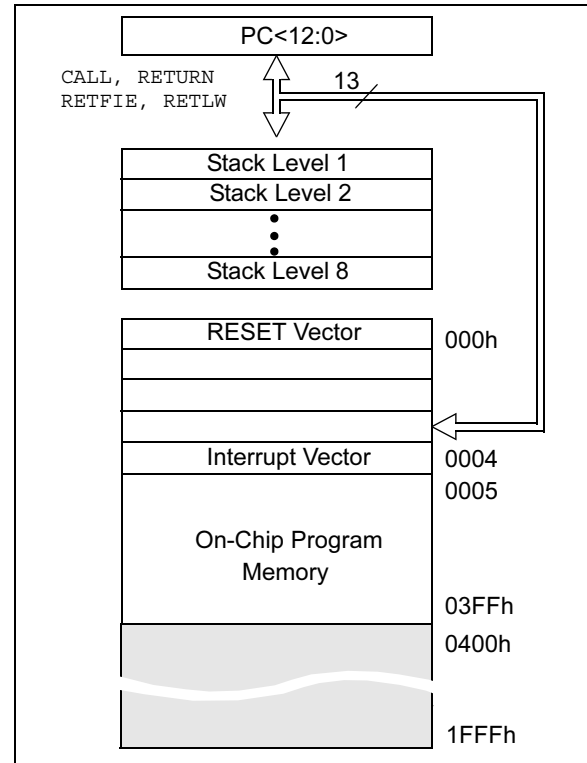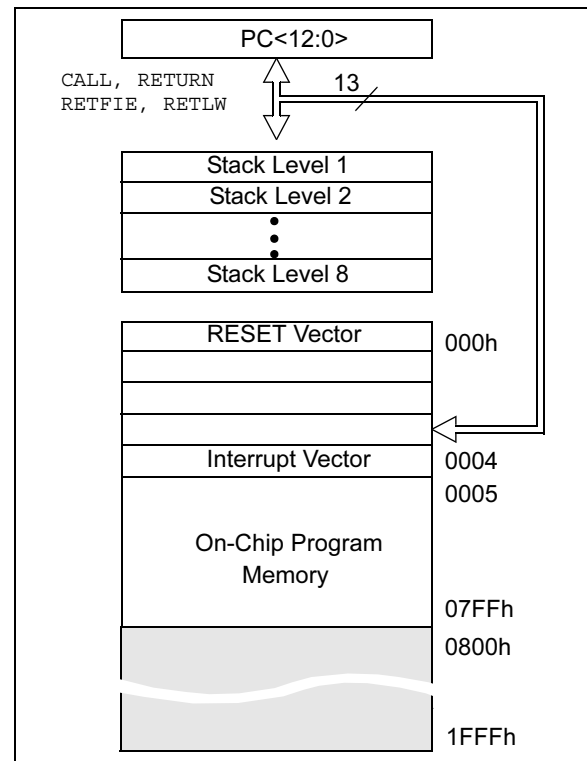**FIGURE 4-2:   PROGRAM MEMORY MAP AND STACK FOR THE PIC16C621/PIC16C621A**

FIGURE 4-3:   PROGRAM MEMORY MAP AND STACK FOR THE PIC16C622/PIC16C622A

4.3 PCL and PCLATH

The program counter (PC) is 13-bits wide. The low byte comes from the PCL register, which is a readable and writable register. The high byte (PC<12:8>) is not directly readable or writable and comes from PCLATH. On any RESET, the PC is cleared. Figure 4-8 shows the two situations for the loading of the PC. The upper example in the figure shows how the PC is loaded on a write to PCL (PCLATH<4:0> → PCH). The lower example in the figure shows how the PC is loaded during a `CALL` or `GOTO` instruction (PCLATH<4:3> → PCH).

FIGURE 4-8: LOADING OF PC IN DIFFERENT SITUATIONS
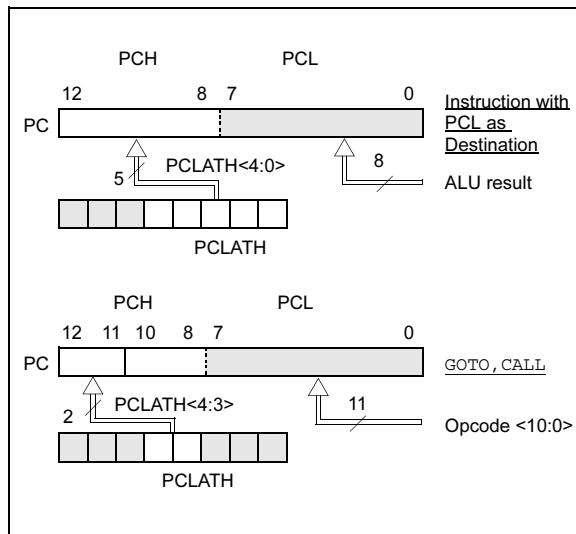
4.3.1 COMPUTED GOTO

A computed GOTO is accomplished by adding an offset to the program counter (`ADDWF PCL`). When doing a table read using a computed GOTO method, care should be exercised if the table location crosses a PCL memory boundary (each 256 byte block). Refer to the application note, *"Implementing a Table Read"* (AN556).

4.3.2 STACK

The PIC16C62X family has an 8-level deep x 13-bit wide hardware stack (Figure 4-2 and Figure 4-3). The stack space is not part of either program or data space and the stack pointer is not readable or writable. The PC is PUSHed onto the stack when a `CALL` instruction is executed or an interrupt causes a branch. The stack is POPed in the event of a `RETURN`, `RETLW` or a `RETFIE` instruction execution. PCLATH is not affected by a `PUSH` or `POP` operation.

The stack operates as a circular buffer. This means that after the stack has been PUSHed eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on).

> **Note 1:** There are no STATUS bits to indicate stack overflow or stack underflow conditions.
>
> **2:** There are no instructions/mnemonics called `PUSH` or `POP`. These are actions that occur from the execution of the `CALL`, `RETURN`, `RETLW` and `RETFIE` instructions, or the vectoring to an interrupt address.

6.2   Using Timer0 with External Clock

When an external clock input is used for Timer0, it must meet certain requirements. The external clock requirement is due to internal phase clock (TOSC) synchronization. Also, there is a delay in the actual incrementing of Timer0 after synchronization.
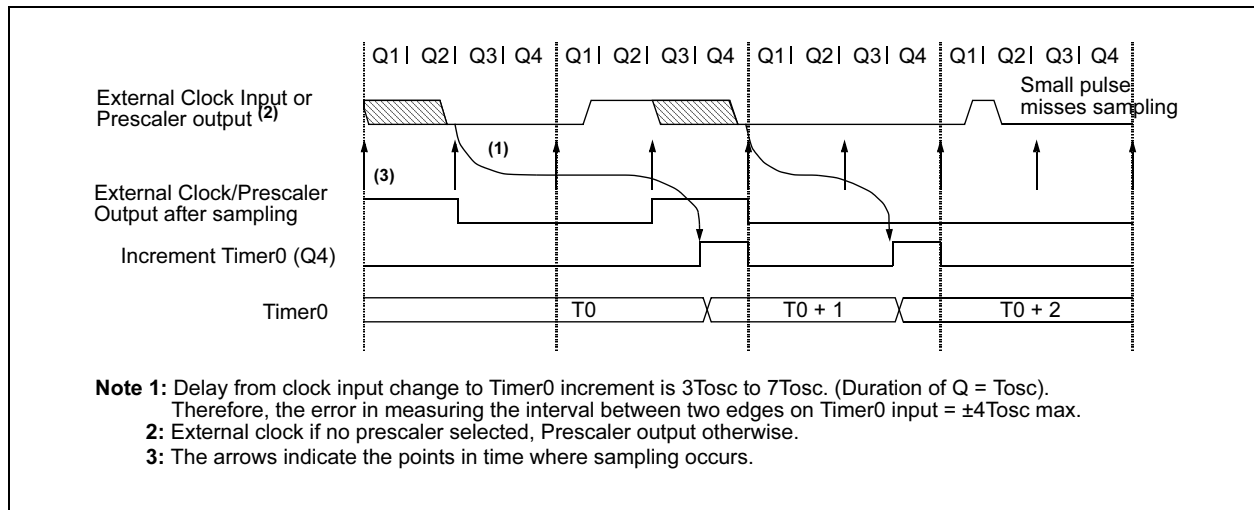
6.2.1   EXTERNAL CLOCK SYNCHRONIZATION

When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks (Figure 6-5). Therefore, it is necessary for T0CKI to be high for at least 2TOSC (and a small RC delay of 20 ns) and low for at least 2TOSC (and a small RC delay of 20 ns). Refer to the electrical specification of the desired device.

When a prescaler is used, the external clock input is divided by the asynchronous ripple-counter type prescaler, so that the prescaler output is symmetrical. For the external clock to meet the sampling requirement, the ripple-counter must be taken into account. Therefore, it is necessary for T0CKI to have a period of at least 4TOSC (and a small RC delay of 40 ns) divided by the prescaler value. The only requirement on T0CKI high and low time is that they do not violate the minimum pulse width requirement of 10 ns. Refer to parameters 40, 41 and 42 in the electrical specification of the desired device.

6.2.2   TIMER0 INCREMENT DELAY

Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the TMR0 is actually incremented. Figure 6-5 shows the delay from the external clock edge to the timer incrementing.

FIGURE 6-5:   TIMER0 TIMING WITH EXTERNAL CLOCK

Note 1: Delay from clock input change to Timer0 increment is 3Tosc to 7Tosc. (Duration of Q = Tosc).
Therefore, the error in measuring the interval between two edges on Timer0 input = ±4Tosc max.
2: External clock if no prescaler selected, Prescaler output otherwise.
3: The arrows indicate the points in time where sampling occurs.

7.0   COMPARATOR MODULE

The comparator module contains two analog comparators. The inputs to the comparators are multiplexed with the RA0 through RA3 pins. The On-Chip Voltage Reference (Section 8.0) can also be an input to the comparators.

The CMCON register, shown in Register 7-1, controls the comparator input and output multiplexers. A block diagram of the comparator is shown in Figure 7-1.

REGISTER 7-1:   CMCON REGISTER (ADDRESS 1Fh)

R-0	R-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
C2OUT	C1OUT	—	—	CIS	CM2	CM1	CM0

bit 7   bit 0

bit 7   **C2OUT**: Comparator 2 output
1 = C2 VIN+ > C2 VIN-
0 = C2 VIN+ < C2 VIN-

bit 6   **C1OUT**: Comparator 1 output
1 = C1 VIN+ > C1 VIN-
0 = C1 VIN+ < C1 VIN-

bit 5-4   **Unimplemented:** Read as '0'

bit 3   **CIS**: Comparator Input Switch
When CM<2:0>: = 001:
1 = C1 VIN- connects to RA3
0 = C1 VIN- connects to RA0
When CM<2:0> = 010:
1 = C1 VIN- connects to RA3
       C2 VIN- connects to RA2
0 = C1 VIN- connects to RA0
       C2 VIN- connects to RA1

bit 2-0   **CM<2:0>**: Comparator mode.

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

8.0 VOLTAGE REFERENCE MODULE

The Voltage Reference is a 16-tap resistor ladder network that provides a selectable voltage reference. The resistor ladder is segmented to provide two ranges of VREF values and has a power-down function to conserve power when the reference is not being used. The VRCON register controls the operation of the reference as shown in Register 8-1. The block diagram is given in Figure 8-1.

8.1 Configuring the Voltage Reference

The Voltage Reference can output 16 distinct voltage levels for each range. The equations used to calculate the output of the Voltage Reference are as follows:

if VRR = 1: VREF = (VR<3:0>/24) x VDD

if VRR = 0: VREF = (VDD x 1/4) + (VR<3:0>/32) x VDD

The setting time of the Voltage Reference must be considered when changing the VREF output (Table 12-1). Example 8-1 shows an example of how to configure the Voltage Reference for an output voltage of 1.25V with VDD = 5.0V.

**REGISTER 8-1: VRCON REGISTER(ADDRESS 9Fh)**

R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
VREN	VROE	VRR	—	VR3	VR2	VR1	VR0

bit 7   bit 0

bit 7 **VREN:** VREF Enable
1 = VREF circuit powered on
0 = VREF circuit powered down, no IDD drain

bit 6 **VROE:** VREF Output Enable
1 = VREF is output on RA2 pin
0 = VREF is disconnected from RA2 pin

bit 5 **VRR:** VREF Range selection
1 = Low Range
0 = High Range

bit 4 **Unimplemented:** Read as '0'

bit 3-0 **VR<3:0>**: VREF value selection $0 \leq$ VR [3:0] ≤ 15
when VRR = 1: VREF = (VR<3:0>/ 24) * VDD
when VRR = 0: VREF = 1/4 * VDD + (VR<3:0>/ 32) * VDD

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

FIGURE 8-1: VOLTAGE REFERENCE BLOCK DIAGRAM

Note: R is defined in Table 12-2.
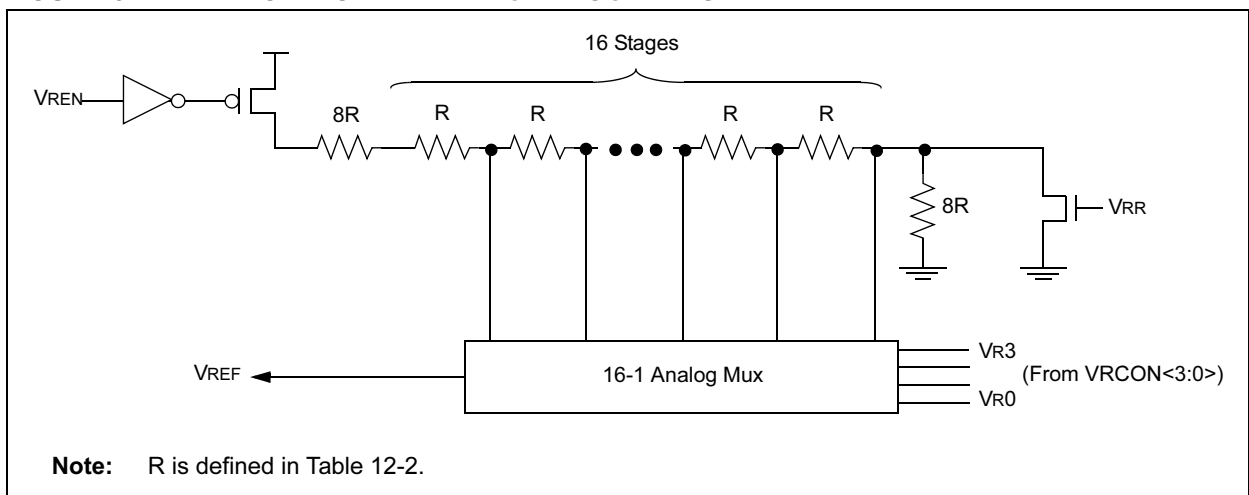
PIC16C62X

9.4 Power-on Reset (POR), Power-up Timer (PWRT), Oscillator Start-up Timer (OST) and Brown-out Reset (BOR)

9.4.1 POWER-ON RESET (POR)

The on-chip POR circuit holds the chip in RESET until V_{DD} has reached a high enough level for proper operation. To take advantage of the POR, just tie the $\overline{MCLR}$ pin through a resistor to V_{DD}. This will eliminate external RC components usually needed to create Power-on Reset. A maximum rise time for V_{DD} is required. See Electrical Specifications for details.

The POR circuit does not produce an internal RESET when V_{DD} declines.

When the device starts normal operation (exits the RESET condition), device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in RESET until the operating conditions are met.

For additional information, refer to Application Note AN607, "Power-up Trouble Shooting".

9.4.2 POWER-UP TIMER (PWRT)

The Power-up Timer provides a fixed 72 ms (nominal) time-out on power-up only, from POR or Brown-out Reset. The Power-up Timer operates on an internal RC oscillator. The chip is kept in RESET as long as PWRT is active. The PWRT delay allows the V_{DD} to rise to an acceptable level. A configuration bit, $\overline{PWRTE}$ can disable (if set) or enable (if cleared or programmed) the Power-up Timer. The Power-up Timer should always be enabled when Brown-out Reset is enabled.

The Power-up Time delay will vary from chip-to-chip and due to V_{DD}, temperature and process variation. See DC parameters for details.

9.4.3 OSCILLATOR START-UP TIMER (OST)

The Oscillator Start-Up Timer (OST) provides a 1024 oscillator cycle (from OSC1 input) delay after the PWRT delay is over. This ensures that the crystal oscillator or resonator has started and stabilized.

The OST time-out is invoked only for XT, LP and HS modes and only on Power-on Reset or wake-up from SLEEP.

9.4.4 BROWN-OUT RESET (BOR)

The PIC16C62X members have on-chip Brown-out Reset circuitry. A configuration bit, BODEN, can disable (if clear/programmed) or enable (if set) the Brown-out Reset circuitry. If V_{DD} falls below 4.0V refer to V_{BOR} parameter D005 (V_{BOR}) for greater than parameter (T_{BOR}) in Table 12-5. The brown-out situation will RESET the chip. A RESET won't occur if V_{DD} falls below 4.0V for less than parameter (T_{BOR}).

On any RESET (Power-on, Brown-out, Watchdog, etc.) the chip will remain in RESET until V_{DD} rises above BV_{DD}. The Power-up Timer will now be invoked and will keep the chip in RESET an additional 72 ms.

If V_{DD} drops below BV_{DD} while the Power-up Timer is running, the chip will go back into a Brown-out Reset and the Power-up Timer will be re-initialized. Once V_{DD} rises above BV_{DD}, the Power-Up Timer will execute a 72 ms RESET. The Power-up Timer should always be enabled when Brown-out Reset is enabled. Figure 9-7 shows typical Brown-out situations.

FIGURE 9-7: BROWN-OUT SITUATIONS
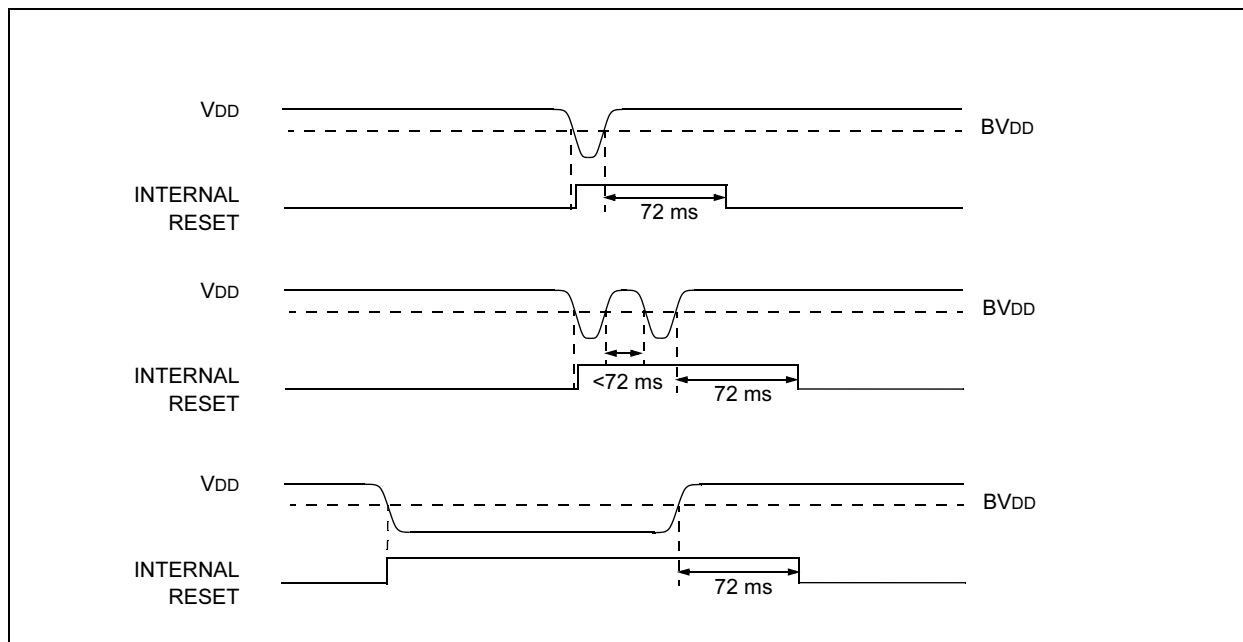
TABLE 9-4:   INITIALIZATION CONDITION FOR SPECIAL REGISTERS

Condition	Program Counter	STATUS Register	PCON Register
Power-on Reset	000h	`0001 1xxx`	`---- --0x`
$\overline{\text{MCLR}}$ Reset during normal operation	000h	`000u uuuu`	`---- --uu`
$\overline{\text{MCLR}}$ Reset during SLEEP	000h	`0001 0uuu`	`---- --uu`
WDT Reset	000h	`0000 uuuu`	`---- --uu`
WDT Wake-up	PC + 1	`uuu0 0uuu`	`---- --uu`
Brown-out Reset	000h	`000x xuuu`	`---- --u0`
Interrupt Wake-up from SLEEP	PC + 1[1]	`uuu1 0uuu`	`---- --uu`

Legend: `u` = unchanged, `x` = unknown, `-` = unimplemented bit, reads as '0'.

Note 1: When the wake-up is due to an interrupt and global enable bit, GIE is set, the PC is loaded with the interrupt vector (0004h) after execution of PC+1.

TABLE 9-5:   INITIALIZATION CONDITION FOR REGISTERS

Register	Address	Power-on Reset	• MCLR Reset during normal operation • MCLR Reset during SLEEP • WDT Reset • Brown-out Reset [1]	• Wake-up from SLEEP through interrupt • Wake-up from SLEEP through WDT time-out
W	—	`xxxx xxxx`	`uuuu uuuu`	`uuuu uuuu`
INDF	00h	—	—	—
TMR0	01h	`xxxx xxxx`	`uuuu uuuu`	`uuuu uuuu`
PCL	02h	`0000 0000`	`0000 0000`	`PC + 1`[3]
STATUS	03h	`0001 1xxx`	`000q quuu`[4]	`uuuq quuu`[4]
FSR	04h	`xxxx xxxx`	`uuuu uuuu`	`uuuu uuuu`
PORTA	05h	`---x xxxx`	`---u uuuu`	`---u uuuu`
PORTB	06h	`xxxx xxxx`	`uuuu uuuu`	`uuuu uuuu`
CMCON	1Fh	`00-- 0000`	`00-- 0000`	`uu-- uuuu`
PCLATH	0Ah	`---0 0000`	`---0 0000`	`---u uuuu`
INTCON	0Bh	`0000 000x`	`0000 000u`	`uuuu uqqq`[2]
PIR1	0Ch	`-0-- ----`	`-0-- ----`	`-q-- ----`[2,5]
OPTION	81h	`1111 1111`	`1111 1111`	`uuuu uuuu`
TRISA	85h	`---1 1111`	`---1 1111`	`---u uuuu`
TRISB	86h	`1111 1111`	`1111 1111`	`uuuu uuuu`
PIE1	8Ch	`-0-- ----`	`-0-- ----`	`-u-- ----`
PCON	8Eh	`---- --0x`	`---- --uq`[1,6]	`---- --uu`
VRCON	9Fh	`000- 0000`	`000- 0000`	`uuu- uuuu`

Legend: `u` = unchanged, `x` = unknown, `-` = unimplemented bit, reads as '0',`q` = value depends on condition.

Note 1: If VDD goes too low, Power-on Reset will be activated and registers will be affected differently.
2: One or more bits in INTCON, PIR1 and/or PIR2 will be affected (to cause wake-up).
3: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).
4: See Table 9-4 for RESET value for specific condition.
5: If wake-up was due to comparator input changing, then bit 6 = 1. All other interrupts generating a wake-up will cause bit 6 = u.
6: If RESET was due to brown-out, then bit 0 = 0. All other RESETS will cause bit 0 = u.

RLF   **Rotate Left f through Carry**

Syntax: [*label*]   RLF   f,d

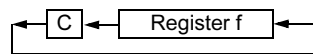Operands: $0 \leq f \leq 127$
$d \in [0,1]$

Operation: See description below

Status Affected: C

Encoding:

00	1101	dfff	ffff

Description: The contents of register 'f' are rotated one bit to the left through the Carry Flag. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example   RLF   REG1,0

Before Instruction
```
REG1    =    1110 0110
C       =    0
```
After Instruction
```
REG1    =    1110 0110
W       =    1100 1100
C       =    1
```

RRF   **Rotate Right f through Carry**

Syntax: [*label*]   RRF   f,d
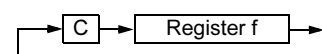
Operands: $0 \leq f \leq 127$
$d \in [0,1]$

Operation: See description below

Status Affected: C

Encoding:

00	1100	dfff	ffff

Description: The contents of register 'f' are rotated one bit to the right through the Carry Flag. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'.

Words: 1

Cycles: 1

Example   RRF   REG1, 0

Before Instruction
```
REG1    =    1110 0110
C       =    0
```
After Instruction
```
REG1    =    1110 0110
W       =    0111 0011
C       =    0
```

SLEEP

Syntax: [*label*   SLEEP]

Operands: None

Operation: 00h $\rightarrow$ WDT,
$0 \rightarrow$ WDT prescaler,
$1 \rightarrow \overline{TO}$,
$0 \rightarrow \overline{PD}$

Status Affected: $\overline{TO}$, $\overline{PD}$

Encoding:

00	0000	0110	0011

Description: The power-down STATUS bit, $\overline{PD}$ is cleared. Time-out STATUS bit, $\overline{TO}$ is set. Watchdog Timer and its prescaler are cleared.
The processor is put into SLEEP mode with the oscillator stopped. See Section 9.8 for more details.

Words: 1

Cycles: 1

Example: SLEEP

NOTES:

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FIGURE 12-1:   **PIC16C62X VOLTAGE-FREQUENCY GRAPH, -40°C ≤ TA ≤ +125°C**

Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

2: The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.
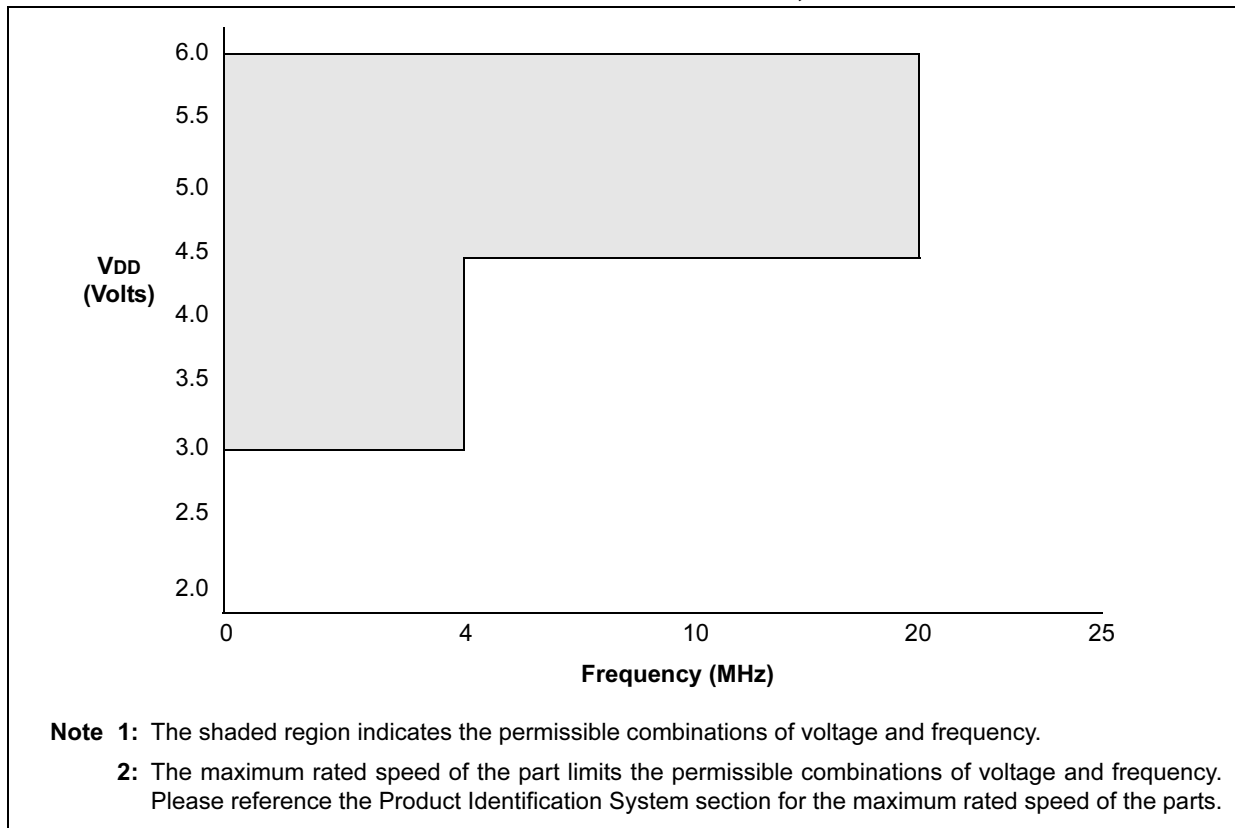
FIGURE 12-2:   **PIC16LC62X VOLTAGE-FREQUENCY GRAPH, -40°C ≤ TA ≤ +125°C**

Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

2: The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.
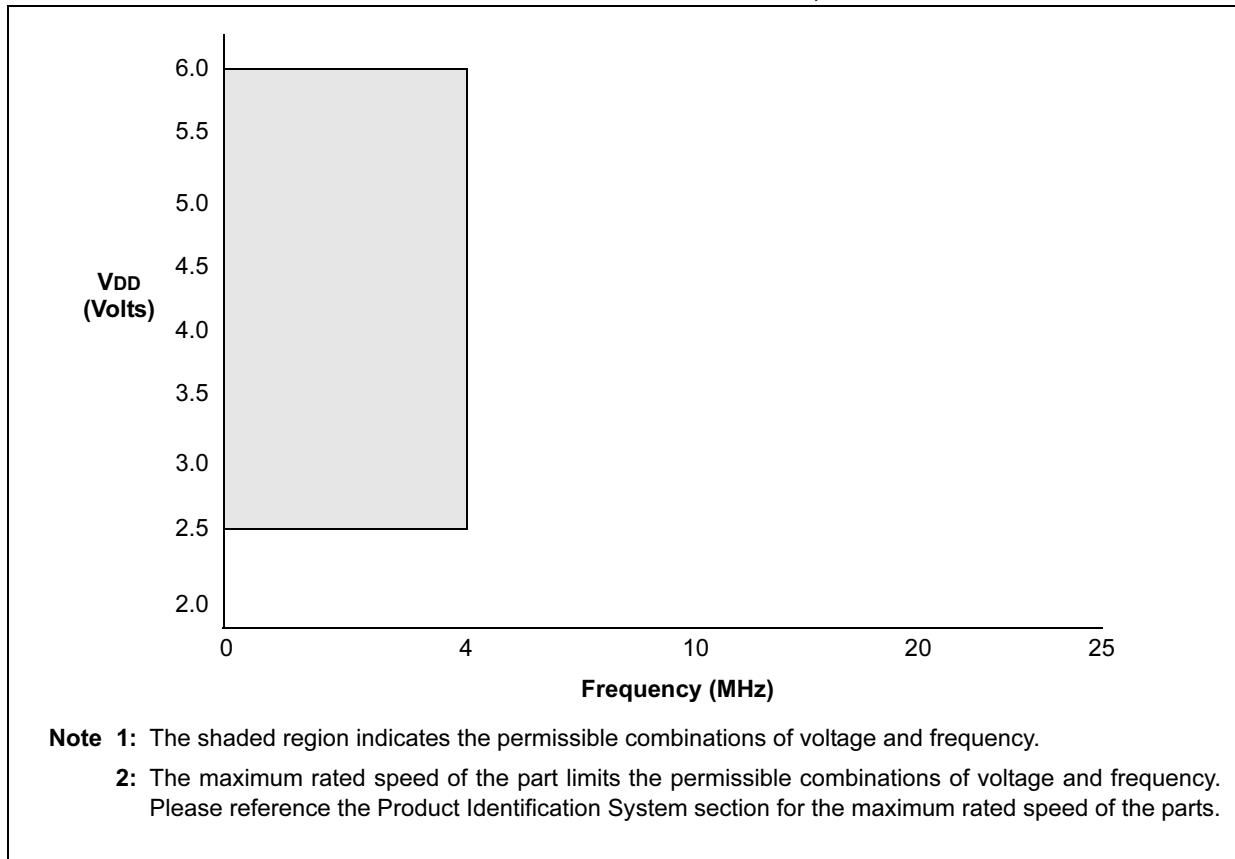
PIC16C62X

FIGURE 12-5: **PIC16LC620A/LC621A/LC622A VOLTAGE-FREQUENCY GRAPH,**
-40°C ≤ TA ≤ 0°C

Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

2: The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.
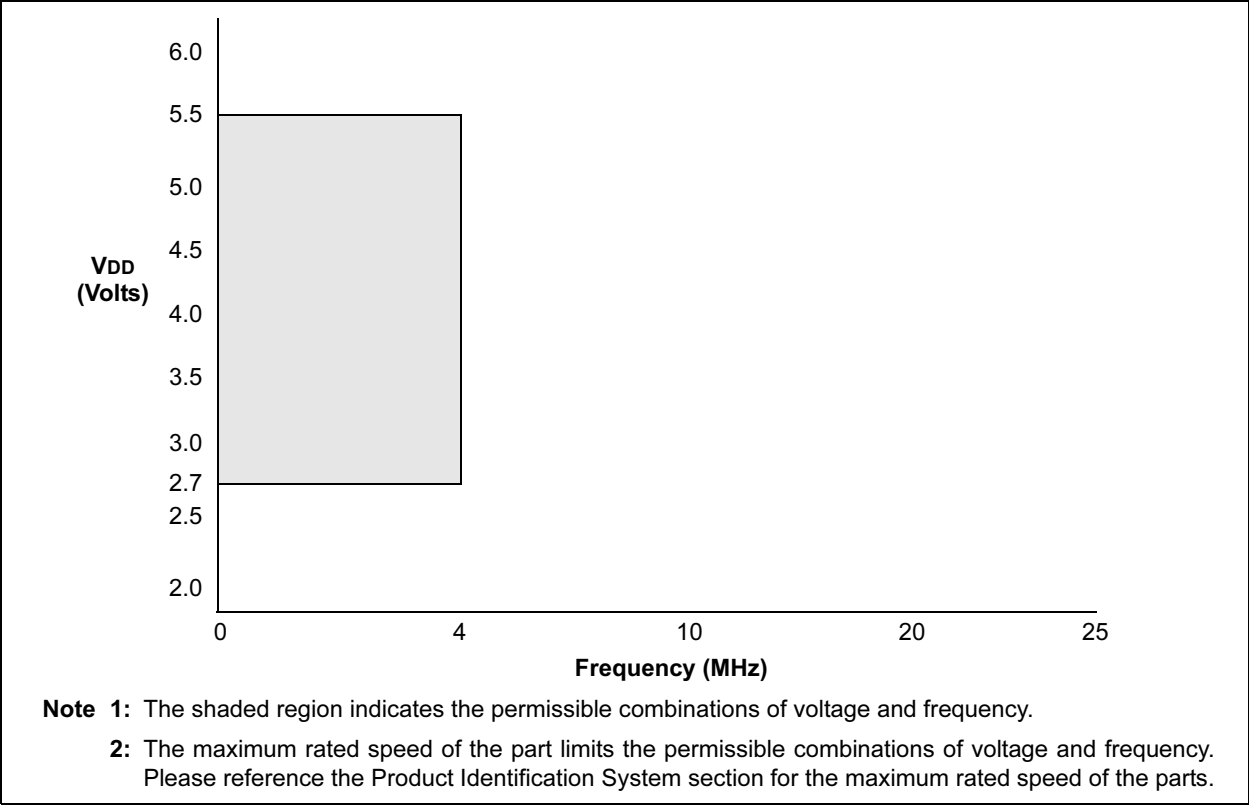
FIGURE 12-6: **PIC16LC620A/LC621A/LC622A VOLTAGE-FREQUENCY GRAPH,**
0°C ≤ TA ≤ +125°C

Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

2: The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.
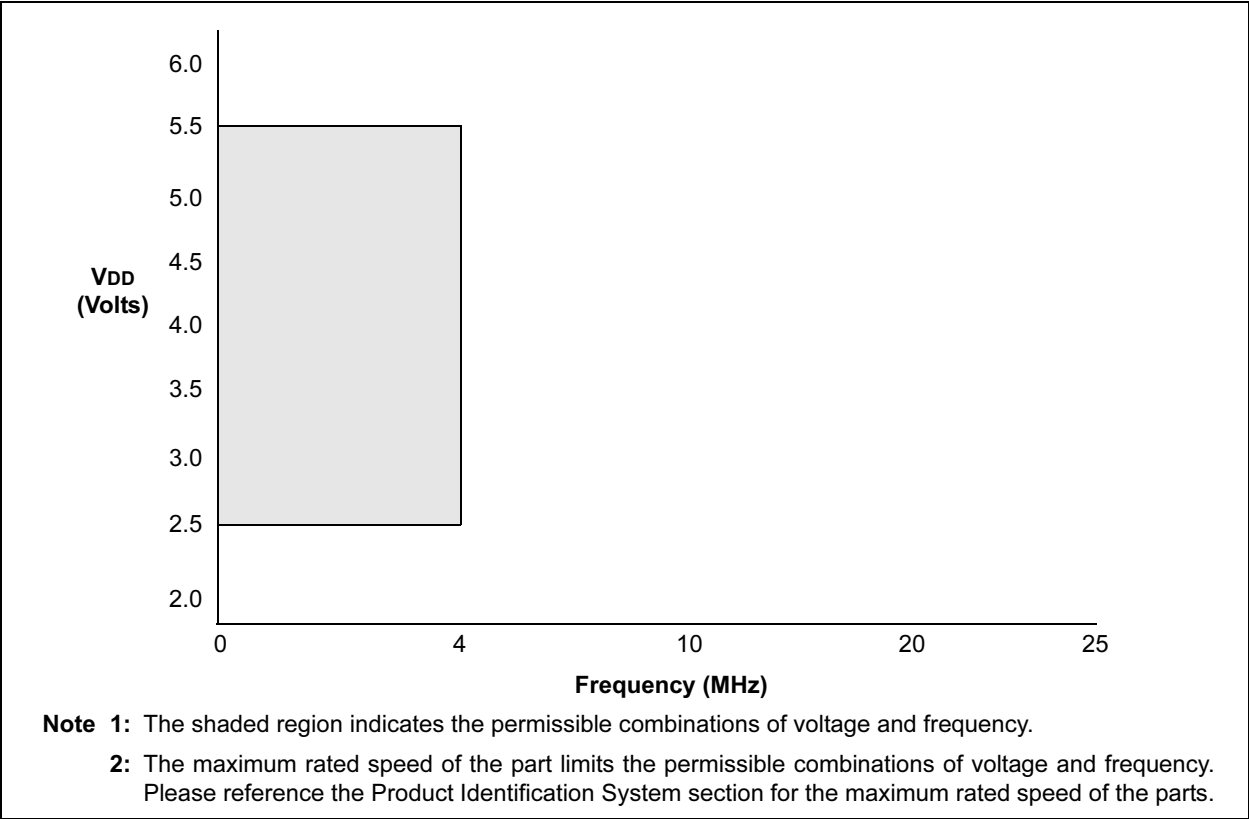
12.2 DC Characteristics: PIC16C62XA-04 (Commercial, Industrial, Extended)
PIC16C62XA-20 (Commercial, Industrial, Extended)
PIC16LC62XA-04 (Commercial, Industrial, Extended) (CONT.)

PIC16C62XA							**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial and -40°C ≤ TA ≤ +125°C for extended
PIC16LC62XA							**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial and -40°C ≤ TA ≤ +125°C for extended
Param. No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D010	IDD	Supply Current[2, 4]	—	1.2	2.0	mA	F_{OSC} = 4 MHz, V_{DD} = 5.5V, WDT disabled, XT mode, **(Note 4)***
			—	0.4	1.2	mA	F_{OSC} = 4 MHz, V_{DD} = 3.0V, WDT disabled, XT mode, **(Note 4)***
			—	1.0	2.0	mA	F_{OSC} = 10 MHz, V_{DD} = 3.0V, WDT disabled, HS mode, **(Note 6)**
			—	4.0	6.0	mA	F_{OSC} = 20 MHz, V_{DD} = 4.5V, WDT disabled, HS mode
			—	4.0	7.0	mA	F_{OSC} = 20 MHz, V_{DD} = 5.5V, WDT disabled*, HS mode
			—	35	70	μA	F_{OSC} = 32 kHz, V_{DD} = 3.0V, WDT disabled, LP mode
D010	IDD	Supply Current[2]	—	1.2	2.0	mA	F_{OSC} = 4 MHz, V_{DD} = 5.5V, WDT disabled, XT mode, **(Note 4)***
			—	—	1.1	mA	F_{OSC} = 4 MHz, V_{DD} = 2.5V, WDT disabled, XT mode, **(Note 4)**
			—	35	70	μA	F_{OSC} = 32 kHz, V_{DD} = 2.5V, WDT disabled, LP mode
D020	IPD	Power-down Current[3]	—	—	2.2	μA	V_{DD} = 3.0V
			—	—	5.0	μA	V_{DD} = 4.5V*
			—	—	9.0	μA	V_{DD} = 5.5V
			—	—	15	μA	V_{DD} = 5.5V Extended Temp.
D020	IPD	Power-down Current[3]	—	—	2.0	μA	V_{DD} = 2.5V
			—	—	2.2	μA	V_{DD} = 3.0V*
			—	—	9.0	μA	V_{DD} = 5.5V
			—	—	15	μA	V_{DD} = 5.5V Extended Temp.

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which V_{DD} can be lowered without losing RAM data.

  2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
  The test conditions for all IDD measurements in Active Operation mode are:
  OSC1 = external square wave, from rail to rail; all I/O pins tri-stated, pulled to V_{DD},
  MCLR = V_{DD}; WDT enabled/disabled as specified.

  3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to V_{DD} or V_{SS}.

  4: For RC osc configuration, current through REXT is not included. The current through the resistor can be estimated by the formula: Ir = V_{DD}/2REXT (mA) with REXT in kΩ.

  5: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

  6: Commercial temperature range only.

PIC16C62X

12.5 DC CHARACTERISTICS: PIC16C620A/C621A/C622A-40[7] (Commercial) PIC16CR620A-40[7] (Commercial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated)					
			Operating temperature $0°C \leq TA \leq +70°C$ for commercial					
Param No.	Sym	Characteristic	Min	Typ†	Max	Unit	Conditions	
	VIL	**Input Low Voltage**						
		I/O ports						
D030		with TTL buffer	Vss	—	0.8V 0.15VDD	V	VDD = 4.5V to 5.5V, otherwise	
D031		with Schmitt Trigger input	Vss		0.2VDD	V		
D032		MCLR, RA4/T0CKI, OSC1 (in RC mode)	Vss	—	0.2VDD	V	**(Note 1)**	
D033		OSC1 (in XT and HS)	Vss	—	0.3VDD	V		
		OSC1 (in LP)	Vss	—	0.6VDD - 1.0	V		
	VIH	**Input High Voltage**						
		I/O ports						
D040		with TTL buffer	2.0V 0.25 VDD + 0.8	—	VDD VDD	V	VDD = 4.5V to 5.5V, otherwise	
D041		with Schmitt Trigger input	0.8 VDD		VDD			
D042		MCLR RA4/T0CKI	0.8 VDD	—	VDD	V		
D043		OSC1 (XT, HS and LP)	0.7 VDD	—	VDD	V		
D043A		OSC1 (in RC mode)	0.9 VDD				**(Note 1)**	
D070	IPURB	**PORTB Weak Pull-up Current**	50	200	400	µA	VDD = 5.0V, VPIN = Vss	
	IIL	**Input Leakage Current**[2, 3]						
		I/O ports (except PORTA)			±1.0	µA	Vss ≤ VPIN ≤ VDD, pin at hi-impedance	
D060		PORTA	—	—	±0.5	µA	Vss ≤ VPIN ≤ VDD, pin at hi-impedance	
D061		RA4/T0CKI	—	—	±1.0	µA	Vss ≤ VPIN ≤ VDD	
D063		OSC1, MCLR	—	—	±5.0	µA	Vss ≤ VPIN ≤ VDD, XT, HS and LP OSC configuration	
	VOL	**Output Low Voltage**						
D080		I/O ports	—	—	0.6	V	IOL = 8.5 mA, VDD = 4.5V, -40° to +85°C	
			—	—	0.6	V	IOL = 7.0 mA, VDD = 4.5V, +125°C	
D083		OSC2/CLKOUT (RC only)	—	—	0.6	V	IOL = 1.6 mA, VDD = 4.5V, -40° to +85°C	
			—	—	0.6	V	IOL = 1.2 mA, VDD = 4.5V, +125°C	
	VOH	**Output High Voltage**[3]						
D090		I/O ports (except RA4)	VDD-0.7	—	—	V	IOH = -3.0 mA, VDD = 4.5V, -40° to +85°C	
			VDD-0.7	—	—	V	IOH = -2.5 mA, VDD = 4.5V, +125°C	
D092		OSC2/CLKOUT (RC only)	VDD-0.7	—	—	V	IOH = -1.3 mA, VDD = 4.5V, -40° to +85°C	
			VDD-0.7	—	—	V	IOH = -1.0 mA, VDD = 4.5V, +125°C	
*D150	VOD	**Open Drain High Voltage**			8.5	V	RA4 pin	
		Capacitive Loading Specs on Output Pins						
D100	COSC2	OSC2 pin			15	pF	In XT, HS and LP modes when external clock used to drive OSC1.	
D101	CIO	All I/O pins/OSC2 (in RC mode)			50	pF		

* These parameters are characterized but not tested.
† Data in "Typ" column is at 5.0V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in Active Operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD, MCLR = VDD; WDT enabled/disabled as specified.
3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or Vss.
4: For RC OSC configuration, current through REXT is not included. The current through the resistor can be estimated by the formula Ir = VDD/2REXT (mA) with REXT in kΩ.
5: The ∆ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.
6: Commercial temperature range only.
7: See Section 12.1 and Section 12.3 for 16C62X and 16CR62X devices for operation between 20 MHz and 40 MHz for valid modified characteristics.

TABLE 12-4: CLKOUT AND I/O TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
10*	TosH2ckL	OSC1↑ to CLKOUT↓[1]	— —	75 —	200 400	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
11*	TosH2ckH	OSC1↑ to CLKOUT↑[1]	— —	75 —	200 400	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
12*	TckR	CLKOUT rise time[1]	— —	35 —	100 200	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
13*	TckF	CLKOUT fall time[1]	— —	35 —	100 200	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
14*	TckL2ioV	CLKOUT ↓ to Port out valid[1]	—	—	20	ns	
15*	TioV2ckH	Port in valid before CLKOUT ↑[1]	T_{OSC} +200 ns T_{OSC} +400 ns	— —	— —	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
16*	TckH2ioI	Port in hold after CLKOUT ↑[1]	0	—	—	ns	
17*	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid	— —	50	150 300	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
18*	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	100 200	— —	— —	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
19*	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	0	—	—	ns	
20*	TioR	Port output rise time	— —	10 —	40 80	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
21*	TioF	Port output fall time	— —	10 —	40 80	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
22*	Tinp	RB0/INT pin high or low time	25 40	— —	— —	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
23	Trbp	RB<7:4> change interrupt high or low time	T_{CY}	—	—	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x T_{OSC}.
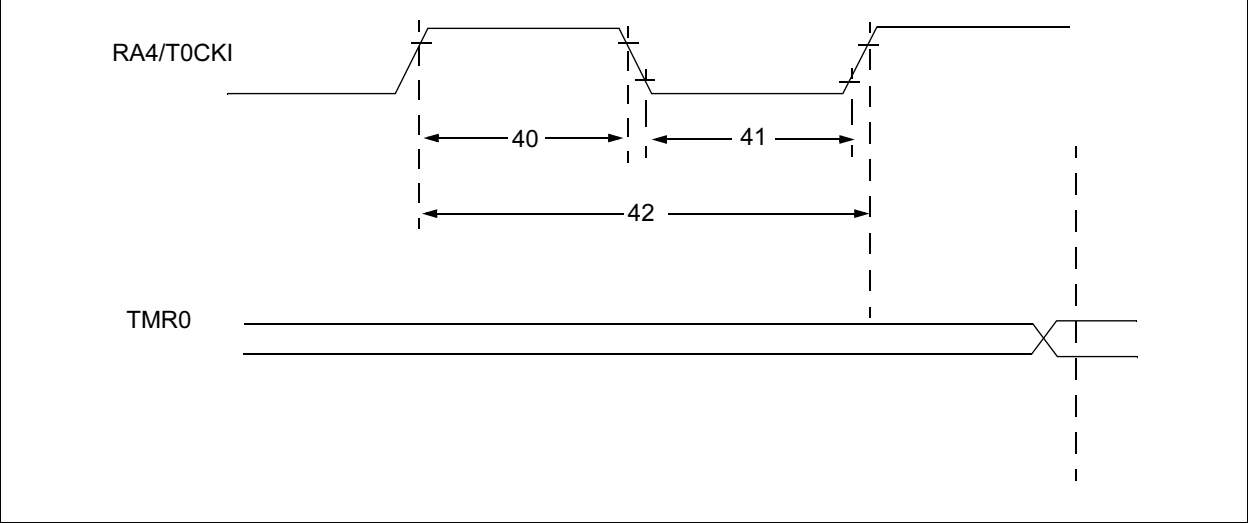
PIC16C62X

FIGURE 12-16: **TIMER0 CLOCK TIMING**

TABLE 12-6: **TIMER0 CLOCK REQUIREMENTS**

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width	No Prescaler	0.5 TCY + 20*	—	—	ns	
			With Prescaler	10*	—	—	ns	
41	Tt0L	T0CKI Low Pulse Width	No Prescaler	0.5 TCY + 20*	—	—	ns	
			With Prescaler	10*	—	—	ns	
42	Tt0P	T0CKI Period		$\frac{TCY + 40*}{N}$	—	—	ns	N = prescale value (1, 2, 4, ..., 256)

*   These parameters are characterized but not tested.

†   Data in "Typ" column is at 5.0V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 13-5: IOH VS. VOH, VDD = 3.0V)
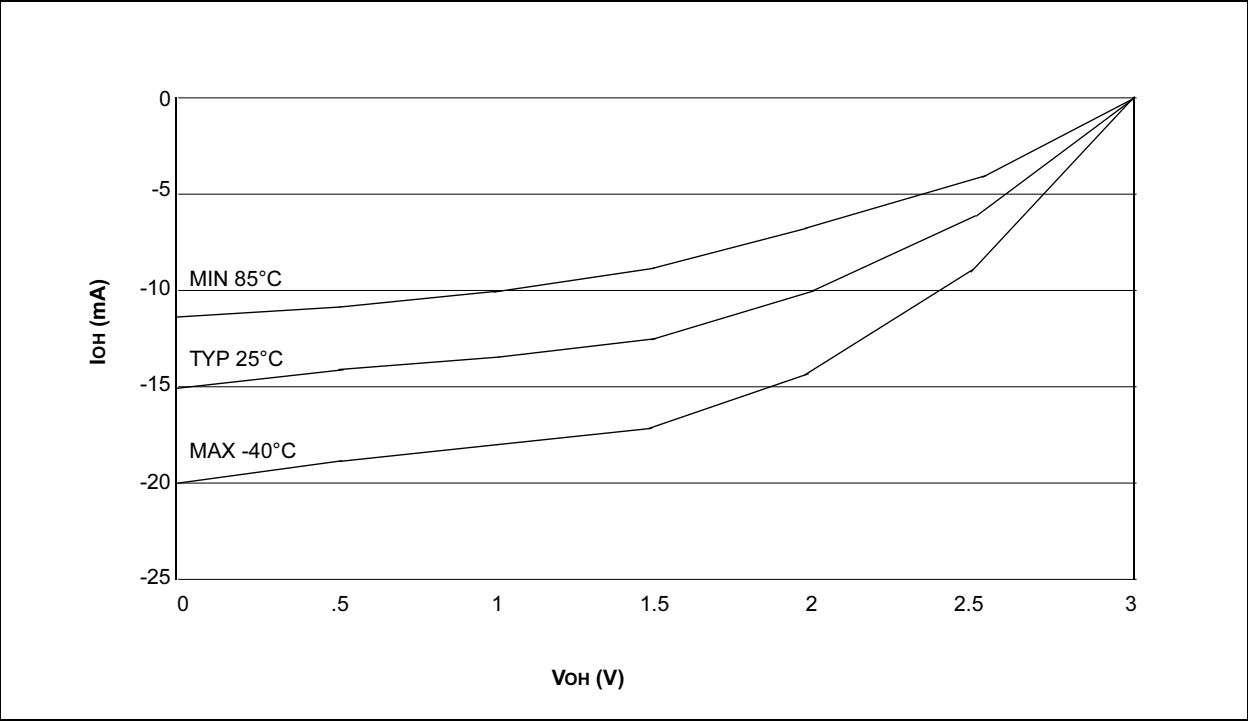
FIGURE 13-6: IOI VS. VOL, VDD = 5.5V)
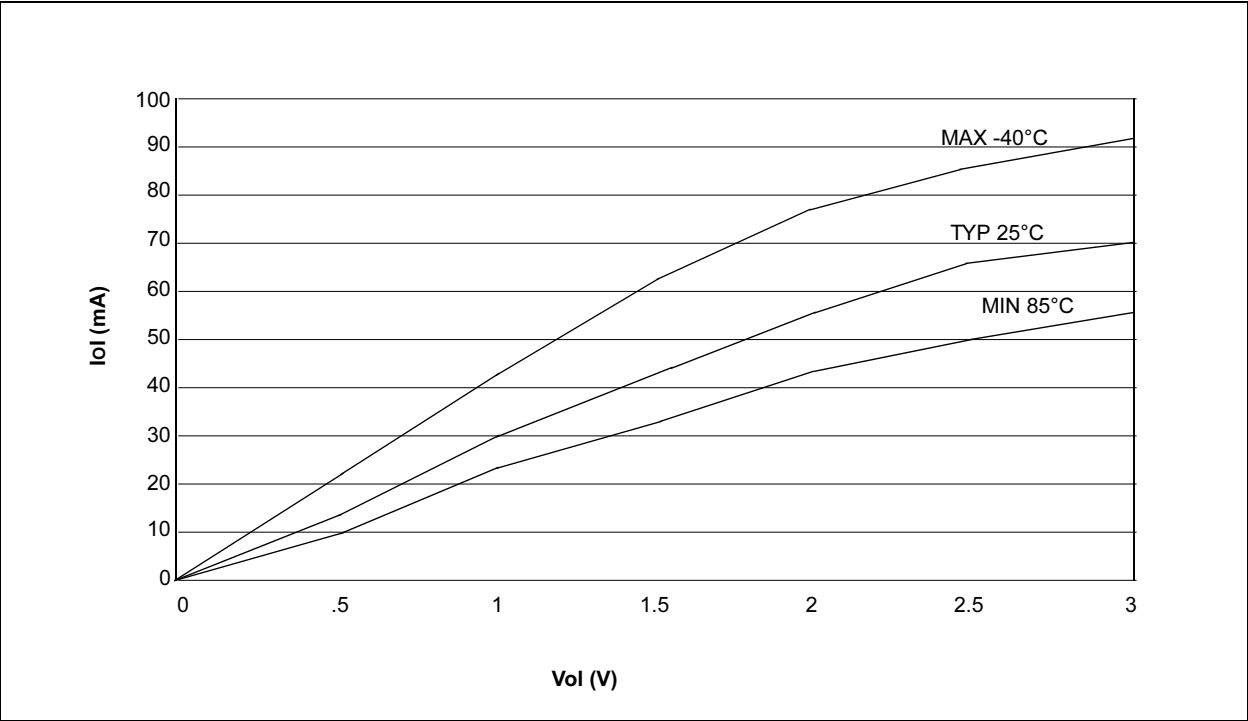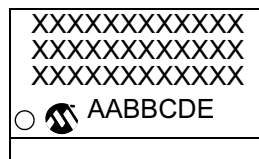
14.1   Package Marking Information

18-Lead PDIP
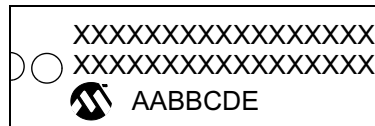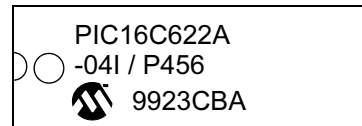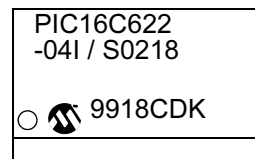
```
XXXXXXXXXXXXXXXXX
XXXXXXXXXXXXXXXXX
    [M] AABBCDE
```

Example

```
PIC16C622A
-04I / P456
    [M] 9923CBA
```

18-Lead SOIC (.300")

```
XXXXXXXXXXX
XXXXXXXXXXX
XXXXXXXXXXX
   [M] AABBCDE
```

Example

```
PIC16C622
-04I / S0218

   [M] 9918CDK
```

18-Lead CERDIP Windowed

```
[M]          XXXXXXX
MICROCHIP    XXXXXXX
             AABBCDE
```

Example

```
[M]          16C622
MICROCHIP    /JW
             9901CBA
```

20-Lead SSOP

```
XXXXXXXXX
XXXXXXXXX
[M]AABBCDE
```

Example

```
PIC16C622A
-04I / 218
[M] 9951CBP
```
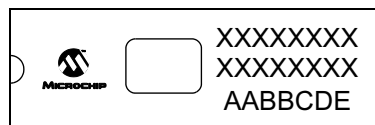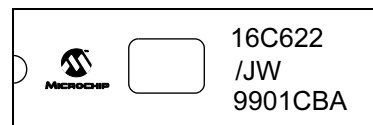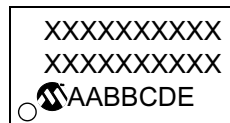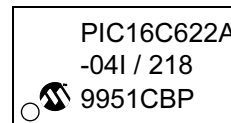
Legend:	XX...X	Customer specific information*
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code

Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

*   Standard PICmicro device marking consists of Microchip part number, year code, week code, and traceability code. For PICmicro device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.