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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	13
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lc622-04i-ss

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

NOTES:

		PIC16C620 ⁽³⁾	PIC16C620A ⁽¹⁾⁽⁴⁾	PIC16CR620A ⁽²⁾	PIC16C621 ⁽³⁾	PIC16C621A ⁽¹⁾⁽⁴⁾	PIC16C622 ⁽³⁾	PIC16C622A ⁽¹⁾⁽⁴⁾
Clock	Maximum Frequency of Operation (MHz)	20	40	20	20	40	20	40
Memory	EPROM Program Memory (x14 words)	512	512	512	1K	1K	2K	2K
	Data Memory (bytes)	80	96	96	80	96	128	128
Peripherals	Timer Module(s)	TMR0	TMR0	TMRO	TMR0	TMR0	TMR0	TMR0
	Comparators(s)	2	2	2	2	2	2	2
	Internal Reference Voltage	Yes						
Features	Interrupt Sources	4	4	4	4	4	4	4
	I/O Pins	13	13	13	13	13	13	13
	Voltage Range (Volts)	2.5-6.0	2.7-5.5	2.5-5.5	2.5-6.0	2.7-5.5	2.5-6.0	2.7-5.5
	Brown-out Reset	Yes						
	Packages	18-pin DIP, SOIC; 20-pin SSOP						

TABLE 1-1: PIC16C62X FAMILY OF DEVICES

All PICmicro[®] Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability. All PIC16C62X Family devices use serial programming with clock pin RB6 and data pin RB7.

Note 1: If you change from this device to another device, please verify oscillator characteristics in your application.

2: For ROM parts, operation from 2.0V - 2.5V will require the PIC16LCR62XA parts.

3: For OTP parts, operation from 2.5V - 3.0V will require the PIC16LC62X part.

4: For OTP parts, operation from 2.7V - 3.0V will require the PIC16LC62XA part.

FIGURE 3-1: BLOCK DIAGRAM



4.2 Data Memory Organization

The data memory (Figure 4-4, Figure 4-5, Figure 4-6 and Figure 4-7) is partitioned into two banks, which contain the General Purpose Registers and the Special Function Registers. Bank 0 is selected when the RP0 bit is cleared. Bank 1 is selected when the RP0 bit (STATUS <5>) is set. The Special Function Registers are located in the first 32 locations of each bank. Register locations 20-7Fh (Bank0) on the PIC16C620A/CR620A/621A and 20-7Fh (Bank0) and A0-BFh (Bank1) on the PIC16C622 and PIC16C622A are General Purpose Registers implemented as static RAM. Some Special Purpose Registers are mapped in Bank 1.

Addresses F0h-FFh of bank1 are implemented as common ram and mapped back to addresses 70h-7Fh in bank0 on the PIC16C620A/621A/622A/CR620A.

4.2.1 GENERAL PURPOSE REGISTER FILE

The register file is organized as 80 x 8 in the PIC16C620/621, 96 x 8 in the PIC16C620A/621A/CR620A and 128 x 8 in the PIC16C622(A). Each is accessed either directly or indirectly through the File Select Register FSR (Section 4.4).

4.2.2.4 PIE1 Register

This register contains the individual enable bit for the comparator interrupt.

REGISTER 4-4:	: PIE1 REGISTER (ADDRESS 8CH)									
	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0		
		CMIE	—	_	—	_				
	bit 7							bit 0		
bit 7	Unimpleme	nted: Read	d as '0'							
bit 6	CMIE: Com	parator Inte	errupt Enable	e bit						
	1 = Enables 0 = Disables	the Compa the Comp	arator interru arator interr	upt upt						
bit 5-0	Unimpleme	nted: Read	d as '0'							
	Legend:									
	R = Readab	le bit	W = W	ritable bit	U = Unim	plemented	bit, read as '	0'		
	- n = Value a	at POR	'1' = Bi	it is set	'0' = Bit i	s cleared	x = Bit is u	nknown		

4.2.2.5 PIR1 Register

This register contains the individual flag bit for the comparator interrupt.

Note:	Interrupt flag bits get set when an interrupt							
	condition occurs, regardless of the state of							
	its corresponding enable bit or the global							
	enable bit, GIE (INTCON<7>). User							
	software should ensure the appropriate							
	interrupt flag bits are clear prior to enabling							
	an interrupt.							

REGISTER 4-5: PIR1 REGISTER (ADDRESS 0CH)

_I\ 4 -J.	FIRT REGISTER (ADDRESS UCH)												
	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0					
	CMIF												
	bit 7							bit 0					
bit 7	Unimplem	ented: Rea	d as '0'										
bit 6	CMIF: Com	nparator Inte	errupt Flag b	it									
	1 = Comparator input has changed												
	0 = Comparator input has not changed												
bit 5-0	Unimplem	ented: Rea	d as '0'										
	Legend:												
	R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'												
	- n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown												

5.2 PORTB and TRISB Registers

PORTB is an 8-bit wide, bi-directional port. The corresponding data direction register is TRISB. A '1' in the TRISB register puts the corresponding output driver in a High Impedance mode. A '0' in the TRISB register puts the contents of the output latch on the selected pin(s).

Reading PORTB register reads the status of the pins, whereas writing to it will write to the port latch. All write operations are read-modify-write operations. So a write to a port implies that the port pins are first read, then this value is modified and written to the port data latch.

Each of the PORTB pins has a weak internal pull-up ($\approx 200 \ \mu A \ typical$). A single control bit can turn on all the pull-ups. This is done by clearing the RBPU (OPTION<7>) bit. The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on Power-on Reset.

Four of PORTB's pins, RB<7:4>, have an interrupt on change feature. Only pins configured as inputs can cause this interrupt to occur (e.g., any RB<7:4> pin configured as an output is excluded from the interrupt on change comparison). The input pins (of RB<7:4>) are compared with the old value latched on the last read of PORTB. The "mismatch" outputs of RB<7:4> are OR'ed together to generate the RBIF interrupt (flag latched in INTCON<0>).

FIGURE 5-5: BLOCK DIAGRAM OF RB<7:4> PINS



This interrupt can wake the device from SLEEP. The user, in the interrupt service routine, can clear the interrupt in the following manner:

- a) Any read or write of PORTB. This will end the mismatch condition.
- b) Clear flag bit RBIF.

A mismatch condition will continue to set flag bit RBIF. Reading PORTB will end the mismatch condition and allow flag bit RBIF to be cleared.

This interrupt on mismatch feature, together with software configurable pull-ups on these four pins allow easy interface to a key pad and make it possible for wake-up on key-depression. (See AN552, "Implementing Wake-Up on Key Strokes.)

Note:	If a change on the I/O pin should occur								
	when the read operation is being executed								
	(start of the Q2 cycle), then the RBIF inter-								
	rupt flag may not get set.								

The interrupt-on-change feature is recommended for wake-up on key depression operation and operations where PORTB is only used for the interrupt on change feature. Polling of PORTB is not recommended while using the interrupt-on-change feature.





6.3 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module, or as a postscaler for the Watchdog Timer, respectively (Figure 6-6). For simplicity, this counter is being referred to as "prescaler" throughout this data sheet. Note that there is only one prescaler available which is mutually exclusive between the Timer0 module and the Watchdog Timer. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the Watchdog Timer and vice-versa.

The PSA and PS<2:0> bits (OPTION<3:0>) determine the prescaler assignment and prescale ratio.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., CLRF 1, MOVWF 1, BSF 1, x....etc.) will clear the prescaler. When assigned to WDT, a CLRWDT instruction will clear the prescaler along with the Watchdog Timer. The prescaler is not readable or writable.



FIGURE 6-6: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER

TABLE 7-1 :	REGISTERS ASSOCIATED WITH COMPARATOR MODULE
--------------------	----------------------------------------------------

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Value on All Other RESETS
1Fh	CMCON	C2OUT	C10UT			CIS	CM2	CM1	CM0	00 0000	00 0000
9Fh	VRCON	VREN	VROE	VRR	_	VR3	VR2	VR1	VR0	000- 0000	000- 0000
0Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1		CMIF		_	_			_	-0	-0
8Ch	PIE1	_	CMIE	_	_	_	_	_	_	-0	-0
85h	TRISA		_	_	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	1 1111	1 1111

Legend: x = unknown, u = unchanged, - = unimplemented, read as "0"

-

EXAMPLE 8-1: VOLTAGE REFERENCE CONFIGURATION

MOVLW	0x02	; 4 Inputs Muxed
MOVWF	CMCON	; to 2 comps.
BSF	STATUS, RPO	; go to Bank 1
MOVLW	0x0F	; RA3-RA0 are
MOVWF	TRISA	; inputs
MOVLW	0xA6	; enable VREF
MOVWF	VRCON	; low range
		; set VR<3:0>=6
BCF	STATUS, RPO	; go to Bank O
CALL	DELAY10	; 10µs delay

8.2 Voltage Reference Accuracy/Error

The full range of VSS to VDD cannot be realized due to the construction of the module. The transistors on the top and bottom of the resistor ladder network (Figure 8-1) keep VREF from approaching VSS or VDD. The voltage reference is VDD derived and therefore, the VREF output changes with fluctuations in VDD. The tested absolute accuracy of the voltage reference can be found in Table 12-2.

8.3 Operation During SLEEP

When the device wakes up from SLEEP through an interrupt or a Watchdog Timer time-out, the contents of the VRCON register are not affected. To minimize current consumption in SLEEP mode, the voltage reference should be disabled.

8.4 Effects of a RESET

A device RESET disables the voltage reference by clearing bit VREN (VRCON<7>). This reset also disconnects the reference from the RA2 pin by clearing bit VROE (VRCON<6>) and selects the high voltage range by clearing bit VRR (VRCON<5>). The VREF value select bits, VRCON<3:0>, are also cleared.

8.5 Connection Considerations

The voltage reference module operates independently of the comparator module. The output of the reference generator may be connected to the RA2 pin if the TRISA<2> bit is set and the VROE bit, VRCON<6>, is set. Enabling the voltage reference output onto the RA2 pin with an input signal present will increase current consumption. Connecting RA2 as a digital output with VREF enabled will also increase current consumption.

The RA2 pin can be used as a simple D/A output with limited drive capability. Due to the limited drive capability, a buffer must be used in conjunction with the voltage reference output for external connections to VREF. Figure 8-2 shows an example buffering technique.

FIGURE 8-2: VOLTAGE REFERENCE OUTPUT BUFFER EXAMPLE

TABLE 8-1: REGISTERS ASSOCIATED WITH VOLTAGE REFERENCE

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value On POR	Value On All Other RESETS
9Fh	VRCON	VREN	VROE	VRR		VR3	VR2	VR1	VR0	000- 0000	000- 0000
1Fh	CMCON	C2OUT	C10UT	_	-	CIS	CM2	CM1	CM0	00 0000	00 0000
85h	TRISA	_	_	_	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	1 1111	1 1111

Note: - = Unimplemented, read as "0"

9.0 SPECIAL FEATURES OF THE CPU

Special circuits to deal with the needs of real-time applications are what sets a microcontroller apart from other processors. The PIC16C62X family has a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection.

These are:

- 1. OSC selection
- 2. RESET Power-on Reset (POR) Power-up Timer (PWRT) Oscillator Start-up Timer (OST) Brown-out Reset (BOR)
- 3. Interrupts
- 4. Watchdog Timer (WDT)
- 5. SLEEP
- 6. Code protection
- 7. ID Locations
- 8. In-Circuit Serial Programming™

The PIC16C62X devices have a Watchdog Timer which is controlled by configuration bits. It runs off its own RC oscillator for added reliability. There are two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in RESET until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay of 72 ms (nominal) on power-up only, designed to keep the part in RESET while the power supply stabilizes. There is also circuitry to RESET the device if a brown-out occurs, which provides at least a 72 ms RESET. With these three functions on-chip, most applications need no external RESET circuitry.

The SLEEP mode is designed to offer a very low current Power-down mode. The user can wake-up from SLEEP through external RESET, Watchdog Timer wake-up or through an interrupt. Several oscillator options are also made available to allow the part to fit the application. The RC oscillator option saves system cost, while the LP crystal option saves power. A set of configuration bits are used to select various options.

9.2.3 EXTERNAL CRYSTAL OSCILLATOR CIRCUIT

Either a prepackaged oscillator can be used or a simple oscillator circuit with TTL gates can be built. Prepackaged oscillators provide a wide operating range and better stability. A well-designed crystal oscillator will provide good performance with TTL gates. Two types of crystal oscillator circuits can be used; one with series resonance or one with parallel resonance.

Figure 9-3 shows implementation of a parallel resonant oscillator circuit. The circuit is designed to use the fundamental frequency of the crystal. The 74AS04 inverter performs the 180° phase shift that a parallel oscillator requires. The 4.7 k Ω resistor provides the negative feedback for stability. The 10 k Ω potentiometers bias the 74AS04 in the linear region. This could be used for external oscillator designs.

FIGURE 9-3: EXTERNAL PARALLEL RESONANT CRYSTAL OSCILLATOR CIRCUIT



Figure 9-4 shows a series resonant oscillator circuit. This circuit is also designed to use the fundamental frequency of the crystal. The inverter performs a 180° phase shift in a series resonant oscillator circuit. The 330 k Ω resistors provide the negative feedback to bias the inverters in their linear region.

FIGURE 9-4: EXTERNAL SERIES RESONANT CRYSTAL OSCILLATOR CIRCUIT



9.2.4 RC OSCILLATOR

For timing insensitive applications the "RC" device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (REXT) and capacitor (CEXT) values, and the operating temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low CEXT values. The user also needs to take into account variation due to tolerance of external R and C components used. Figure 9-5 shows how the R/C combination is connected to the PIC16C62X. For REXT values below 2.2 k Ω , the oscillator operation may become unstable or stop completely. For very high REXT values (e.g., 1 M Ω), the oscillator becomes sensitive to noise, humidity and leakage. Thus, we recommend to keep REXT between 3 k Ω and 100 k Ω .

Although the oscillator will operate with no external capacitor (CEXT = 0 pF), we recommend using values above 20 pF for noise and stability reasons. With no or small external capacitance, the oscillation frequency can vary dramatically due to changes in external capacitances, such as PCB trace capacitance or package lead frame capacitance.

See Section 13.0 for RC frequency variation from part to part due to normal process variation. The variation is larger for larger R (since leakage current variation will affect RC frequency more for large R) and for smaller C (since variation of input capacitance will affect RC frequency more).

See Section 13.0 for variation of oscillator frequency due to VDD for given REXT/CEXT values, as well as frequency variation due to operating temperature for given R, C and VDD values.

The oscillator frequency, divided by 4, is available on the OSC2/CLKOUT pin, and can be used for test purposes or to synchronize other logic (Figure 3-2 for waveform).

FIGURE 9-5: RC OSCILLATOR MODE



BTFSS	Bit Test f, Skip if Set	CALL	Call Subroutine
Syntax:	[<i>label</i>]BTFSS f,b	Syntax:	[<i>label</i>] CALL k
Operands:	$0 \leq f \leq 127$	Operands:	$0 \leq k \leq 2047$
Operation:	0 ≤ b < 7 skip if (f) = 1 None	Operation:	(PC)+ 1→ TOS, k → PC<10:0>, (PCLATH<4:3>) → PC<12:11>
Encoding:	01 11bb bfff ffff	Status Affected:	None
Description:	If hit 'h' in register 'f' is '1' then the	Encoding:	10 Okkk kkkk kkkk
	next instruction is skipped. If bit 'b' is '1', then the next instruc- tion fetched during the current instruction execution, is discarded and a NOP is executed instead, making this a two-cycle instruction.	Description:	Call Subroutine. First, return address (PC+1) is pushed onto the stack. The eleven bit immedi- ate address is loaded into PC bits <10:0>. The upper bits of the PC are loaded from PCLATH. CALL is
Words:	1	\A/a vala -	a two-cycle instruction.
Cycles:	1(2)	vvoras:	1
Example	HERE BTFSS FLAG,1	Cycles:	Z
	TRUE • DE •	Example	HERE CALL THER E
	Before Instruction PC = address HERE After Instruction if FLAG<1> = 0, PC = address FALSE if FLAG<1> = 1,		PC = Address HERE After Instruction PC = Address THERE TOS = Address HERE+1
	IC- address TRUE	CLRF	Clear f
		Syntax:	[<i>label</i>] CLRF f
		Operands:	$0 \le f \le 127$
		Operation:	$\begin{array}{l} 00h \rightarrow (f) \\ 1 \rightarrow Z \end{array}$
		Status Affected:	Z
		Encoding:	00 0001 1fff ffff
		Description:	The contents of register 'f' are cleared and the Z bit is set.
		Words:	1
		Cycles:	1
		Example	CLRF FLAG_REG
			Before Instruction FLAG_REG = 0x5A After Instruction FLAG_REG = 0x00 Z = 1

PIC16C62X

RETFIE	Return fr	rom Inte	rrupt					
Syntax:	[label] RETFIE							
Operands:	None							
Operation:	$TOS \rightarrow PC$, 1 $\rightarrow GIE$							
Status Affected:	None							
Encoding:	00	0000	0000	1001				
Description:	Return fro POPed a loaded in enabled b Interrupt (INTCON instructio	om Intern nd Top o the PC. by setting Enable b I<7>). Th n.	rupt. Stac f Stack (T Interrupts g Global bit, GIE iis is a two	k is OS) is s are o-cycle				
Words:	1							
Cycles:	2							
Example	RETFIE							
	After Inte	rrupt PC = GIE =	TOS 1					

RETLW	Return with Literal in W						
Syntax:	[<i>label</i>] RETLW k						
Operands:	$0 \leq k \leq 255$						
Operation:	$k \rightarrow (W);$ TOS $\rightarrow PC$						
Status Affected:	None						
Encoding:	11 01xx kkkk kkkk						
Description:	The W register is loaded with the eight bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a two-cycle instruction.						
Words:	1						
Cycles:	2						
Example	CALL TABLE;W contains table						
TABLE	;offset value ;W now has table value • ADDWF PC ;W = offset RETLW k1 ;Begin table RETLW k2 ;						
	• RETLW kn ; End of table Before Instruction W = 0x07 After Instruction W = value of k8						
RETURN	Return from Subroutine						
Syntax:	[label] RETURN						
Operands:	None						
Operation:	$TOS \rightarrow PC$						
Status Affected:	None						
Encoding:	00 0000 0000 1000						
Description:	Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a two-cycle instruction.						
Words:	1						
Cycles:	2						
Example	RETURN						
	After Interrupt PC = TOS						

11.14 PICDEM 1 PICmicro Demonstration Board

The PICDEM 1 demonstration board demonstrates the capabilities of the PIC16C5X (PIC16C54 to PIC16C58A), PIC16C61, PIC16C62X, PIC16C71, PIC16C8X, PIC17C42, PIC17C43 and PIC17C44. All necessary hardware and software is included to run basic demo programs. The sample microcontrollers provided with the PICDEM 1 demonstration board can be programmed with a PRO MATE II device programmer, or a PICSTART Plus development programmer. The PICDEM 1 demonstration board can be connected to the MPLAB ICE in-circuit emulator for testing. A prototype area extends the circuitry for additional application components. Features include analog input, push button switches and eight LEDs.

11.15 PICDEM.net Internet/Ethernet Demonstration Board

The PICDEM.net demonstration board is an Internet/ Ethernet demonstration board using the PIC18F452 microcontroller and TCP/IP firmware. The board supports any 40-pin DIP device that conforms to the standard pinout used by the PIC16F877 or PIC18C452. This kit features a user friendly TCP/IP stack, web server with HTML, a 24L256 Serial EEPROM for Xmodem download to web pages into Serial EEPROM, ICSP/MPLAB ICD 2 interface connector, an Ethernet interface, RS-232 interface, and a 16 x 2 LCD display. Also included is the book and CD-ROM *"TCP/IP Lean, Web Servers for Embedded Systems,"* by Jeremy Bentham

11.16 PICDEM 2 Plus Demonstration Board

The PICDEM 2 Plus demonstration board supports many 18-, 28-, and 40-pin microcontrollers, including PIC16F87X and PIC18FXX2 devices. All the necessary hardware and software is included to run the demonstration programs. The sample microcontrollers provided with the PICDEM 2 demonstration board can be programmed with a PRO MATE II device programmer, PICSTART Plus development programmer, or MPLAB ICD 2 with a Universal Programmer Adapter. The MPLAB ICD 2 and MPLAB ICE in-circuit emulators may also be used with the PICDEM 2 demonstration board to test firmware. A prototype area extends the circuitry for additional application components. Some of the features include an RS-232 interface, a 2 x 16 LCD display, a piezo speaker, an on-board temperature sensor, four LEDs, and sample PIC18F452 and PIC16F877 FLASH microcontrollers.

11.17 PICDEM 3 PIC16C92X Demonstration Board

The PICDEM 3 demonstration board supports the PIC16C923 and PIC16C924 in the PLCC package. All the necessary hardware and software is included to run the demonstration programs.

11.18 PICDEM 4 8/14/18-Pin Demonstration Board

The PICDEM 4 can be used to demonstrate the capabilities of the 8-, 14-, and 18-pin PIC16XXXX and PIC18XXXX MCUs, including the PIC16F818/819, PIC16F87/88, PIC16F62XA and the PIC18F1320 family of microcontrollers. PICDEM 4 is intended to showcase the many features of these low pin count parts, including LIN and Motor Control using ECCP. Special provisions are made for low power operation with the supercapacitor circuit, and jumpers allow onboard hardware to be disabled to eliminate current draw in this mode. Included on the demo board are provisions for Crystal, RC or Canned Oscillator modes, a five volt regulator for use with a nine volt wall adapter or battery, DB-9 RS-232 interface, ICD connector for programming via ICSP and development with MPLAB ICD 2, 2x16 liquid crystal display, PCB footprints for H-Bridge motor driver, LIN transceiver and EEPROM. Also included are: header for expansion, eight LEDs, four potentiometers, three push buttons and a prototyping area. Included with the kit is a PIC16F627A and a PIC18F1320. Tutorial firmware is included along with the User's Guide.

11.19 PICDEM 17 Demonstration Board

The PICDEM 17 demonstration board is an evaluation board that demonstrates the capabilities of several Microchip microcontrollers, including PIC17C752, PIC17C756A, PIC17C762 and PIC17C766. A programmed sample is included. The PRO MATE II device programmer, or the PICSTART Plus development programmer, can be used to reprogram the device for user tailored application development. The PICDEM 17 demonstration board supports program download and execution from external on-board FLASH memory. A generous prototype area is available for user hardware expansion. NOTES:

12.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings †

Ambient Temperature under bias	40° to +125°C
Storage Temperature	65° to +150°C
Voltage on any pin with respect to Vss (except VDD and MCLR)	-0.6V to VDD +0.6V
Voltage on VDD with respect to Vss	0 to +7.5V
Voltage on MCLR with respect to Vss (Note 2)	0 to +14V
Voltage on RA4 with respect to Vss	8.5V
Total power Dissipation (Note 1)	1.0W
Maximum Current out of Vss pin	
Maximum Current into VDD pin	
Input Clamp Current, Iк (Vi <0 or Vi> VDD)	±20 mA
Output Clamp Current, IOK (Vo <0 or Vo>VoD)	±20 mA
Maximum Output Current sunk by any I/O pin	25 mA
Maximum Output Current sourced by any I/O pin	25 mA
Maximum Current sunk by PORTA and PORTB	
Maximum Current sourced by PORTA and PORTB	
Note 1: Power dissipation is calculated as follows: PDIS = VDD x {IDD - \sum IOH} + \sum	$\{(VDD-VOH) \times IOH\} + \sum (VOI \times IOL).$

2: Voltage spikes below Vss at the MCLR pin, inducing currents greater than 80 mA, may cause latchup. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the MCLR pin rather than pulling this pin directly to Vss.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIC16C62X







12.4 DC Characteristics: PIC16C62X/C62XA/CR62XA (Commercial, Industrial, Extended) PIC16LC62X/LC62XA/LCR62XA (Commercial, Industrial, Extended) (CONT.)

PIC16C62X/C62XA/CR62XA			$\begin{array}{l lllllllllllllllllllllllllllllllllll$					
PIC16LC62X/LC62XA/LCR62XA			$\begin{array}{llllllllllllllllllllllllllllllllllll$					
Param. No.	Sym	Characteristic	Min	Тур†	Мах	Units	Conditions	
	Vol	Output Low Voltage						
D080		I/O ports	_	_	0.6	v	IOL = 8.5 mA, VDD = 4.5V, -40° to +85°C	
			_	_	0.6	V	IOL = 7.0 mA, VDD = 4.5V, +125°C	
D083		OSC2/CLKOUT (RC only)	_	_	0.6	V	IOL = 1.6 mA, VDD = 4.5V, -40° to +85°C	
			_	_	0.6	V	IoL = 1.2 mA, VDD = 4.5V, +125°C	
	Vон	Output High Voltage ⁽³⁾						
D090		I/O ports (Except RA4)	VDD-0.7		_	v	ІОН = -3.0 mA, VDD = 4.5V, -40° to +85°С	
			VDD-0.7		_	V	Іон = -2.5 mA, Vdd = 4.5V, +125°С	
D092		OSC2/CLKOUT (RC only)	VDD-0.7	_	_	V	ІОН = -1.3 mA, VDD = 4.5V, -40° to +85°С	
			VDD-0.7	_	_	V	Іон = -1.0 mA, Vdd = 4.5V, +125°С	
	Vон	Output High Voltage ⁽³⁾						
D090		I/O ports (Except RA4)	VDD-0.7	_	_	V	ІОН = -3.0 mA, VDD = 4.5V, -40° to +85°C	
			VDD-0.7	_	_	V	ІОН = -2.5 mA, VDD = 4.5V, +125°C	
D092		OSC2/CLKOUT (RC only)	VDD-0.7	—	-	V	IOH = -1.3 mA, VDD = 4.5V, -40° to +85°С	
			VDD-0.7		—	V	IOH = -1.0 mA, VDD = 4.5V, +125°С	
D150	Vod	Open-Drain High Voltage			10 8.5*	V	RA4 pin PIC16C62X, PIC16LC62X RA4 pin PIC16C62XA, PIC16LC62XA, PIC16CR62XA, PIC16LCR62XA	
D150	Vod	Open-Drain High Voltage			10 8.5*	V	RA4 pin PIC16C62X, PIC16LC62X RA4 pin PIC16C62XA, PIC16LC62XA, PIC16CR62XA, PIC16LCR62XA	
		Capacitive Loading Specs on Output Pins						
D100	COSC 2	OSC2 pin			15	pF	In XT, HS and LP modes when external clock used to drive OSC1.	
D101	Сю	All I/O pins/OSC2 (in RC mode)			50	pF		
		Capacitive Loading Specs on Output Pins						
D100	COSC 2	OSC2 pin			15	pF	In XT, HS and LP modes when external clock used to drive OSC1.	
D101	Сю	All I/O pins/OSC2 (in RC mode)			50	pF		

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1 pin is a Schmitt Trigger input. It is not recommended that the PIC16C62X(A) be driven with external clock in RC mode.

2: The leakage current on the MCLR pin is strongly dependent on applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

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