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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

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Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	13
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	18-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lc622at-04-so

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

### **Device Differences**

Device	Voltage Range	Oscillator	Process Technology (Microns)
PIC16C620 <sup>(3)</sup>	2.5 - 6.0	See Note 1	0.9
PIC16C621 <sup>(3)</sup>	2.5 - 6.0	See Note 1	0.9
PIC16C622 <sup>(3)</sup>	2.5 - 6.0	See Note 1	0.9
PIC16C620A <sup>(4)</sup>	2.7 - 5.5	See Note 1	0.7
PIC16CR620A <sup>(2)</sup>	2.5 - 5.5	See Note 1	0.7
PIC16C621A <sup>(4)</sup>	2.7 - 5.5	See Note 1	0.7
PIC16C622A <sup>(4)</sup>	2.7 - 5.5	See Note 1	0.7

Note 1: If you change from this device to another device, please verify oscillator characteristics in your application.

2: For ROM parts, operation from 2.5V - 3.0V will require the PIC16LCR62X parts.

**3:** For OTP parts, operation from 2.5V - 3.0V will require the PIC16LC62X parts.

4: For OTP parts, operations from 2.7V - 3.0V will require the PIC16LC62XA parts.

NOTES:

#### FIGURE 4-4: DATA MEMORY MAP FOR THE PIC16C620/621

File Address	3		File Address
00h	INDF <sup>(1)</sup>	INDF <sup>(1)</sup>	80h
01h	TMR0	OPTION	81h
02h	PCL	PCL	82h
03h	STATUS	STATUS	83h
04h	FSR	FSR	84h
05h	PORTA	TRISA	85h
06h	PORTB	TRISB	86h
07h			87h
08h			88h
09h			89h
0Ah	PCLATH	PCLATH	8Ah
0Bh	INTCON	INTCON	8Bh
0Ch	PIR1	PIE1	8Ch
0Dh			8Dh
0Eh		PCON	8Eh
0Fh			8Fh
10h			90h
11h			91h
12h			92h
13h			93h
14h			94h
15h			95h
16h			96h
17h			97h
18h			98h
19h			99h
1Ah			9Ah
1Bh			9Bh
1Ch			9Ch
1Dh			9Dh
1Eh			9Eh
1Fh	CMCON	VRCON	9Fh
20h	Osmanal		A0h
	Purpose		
6Eb	Register		
70n			
Į			_
7Fh	Donk 0	Dorld 1	FFh
	Dank U	Bank T	
Unimp	plemented data me	mory locations, r	ead as '0'.
Note 1:	Not a physical re	egister.	

# FIGURE 4-5:

#### DATA MEMORY MAP FOR THE PIC16C622

File Address	3		File Address				
00h	INDF <sup>(1)</sup>	INDF <sup>(1)</sup>	80h				
01h	TMR0	OPTION	81h				
02h	PCL	PCL	82h				
03h	STATUS	STATUS	83h				
04h	FSR	FSR	84h				
05h	PORTA	TRISA	85h				
06h	PORTB	TRISB	86h				
07h			87h				
08h			88h				
09h			89h				
0Ah	PCLATH	PCLATH	8Ah				
0Bh	INTCON	INTCON	8Bh				
0Ch	PIR1	PIE1	8Ch				
0Dh			8Dh				
0Eh		PCON	8Eh				
0Fh			8Fh				
10h			90h				
11h			91h				
12h			92h				
13h			93h				
14h			94h				
15h			95h				
16h			96h				
17h			97h				
18h			98h				
19h			99h				
1Ah			9Ah				
1Bh			9Bh				
1Ch			9Ch				
1Dh			9Dh				
1Eh			9Eh				
1Fh	CMCON	VRCON	9Fh				
20h			A0h				
	General	General	7.011				
	Purpose Register	Purpose Register					
	rtogiotor	rtogiotor	BFh				
			C0h				
7Fh			FFh				
,,,,,	Bank 0	Bank 1					
Unimp	plemented data me	mory locations, re	ead as '0'.				
Note 1:	Not a physical m	aistor					
<b>Note 1:</b> Not a physical register.							

#### 4.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and Peripheral functions for controlling the desired operation of the device (Table 4-1). These registers are static RAM. The Special Function Registers can be classified into two sets (core and peripheral). The Special Function Registers associated with the "core" functions are described in this section. Those related to the operation of the peripheral features are described in the section of that peripheral feature.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR Reset	Value on all other RESETS <sup>(1)</sup>
Bank 0											
00h	INDF	Addressin register)	essing this location uses contents of FSR to address data memory (not a physical ter)								XXXX XXXX
01h	TMR0	Timer0 Mo	er0 Module's Register								uuuu uuuu
02h	PCL	Program (	Counter's (F	PC) Least S	Significant B	yte				0000 0000	0000 0000
03h	STATUS	IRP <sup>(2)</sup>	RP1 <sup>(2)</sup>	RP0	TO	PD	Z	DC	С	0001 1xxx	000q quuu
04h	FSR	Indirect da	ata memory	address po	ointer					xxxx xxxx	uuuu uuuu
05h	PORTA	—	—	—	RA4	RA3	RA2	RA1	RA0	x 0000	u 0000
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	uuuu uuuu
07h-09h	Unimplemented									_	_
0Ah	PCLATH	—	—	—	Write buffe	er for upper	5 bits of pr	ogram coui	nter	0 0000	0 0000
0Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	—	CMIF	—	—	—	—	—	—	-0	-0
0Dh-1Eh	Unimplemented									_	_
1Fh	CMCON	C2OUT	C10UT	—	—	CIS	CM2	CM1	CM0	00 0000	00 0000
Bank 1											
80h	INDF	Addressin register)	g this locat	ion uses co	ntents of FS	SR to addre	ess data me	mory (not a	a physical	xxxx xxxx	xxxx xxxx
81h	OPTION	RBPU	INTEDG	TOCS	TOSE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
82h	PCL	Program (	Counter's (F	PC) Least S	ignificant B	yte				0000 0000	0000 0000
83h	STATUS	IRP <sup>(2)</sup>	RP1 <sup>(2)</sup>	RP0	TO	PD	Z	DC	С	0001 1xxx	000q quuu
84h	FSR	Indirect da	ata memory	address po	ointer					xxxx xxxx	uuuu uuuu
85h	TRISA	-	-	—	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	1 1111	1 1111
86h	TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	1111 1111	1111 1111
87h-89h	Unimplemented									_	_
8Ah	PCLATH	-	-	—	Write buffe	er for upper	5 bits of pr	ogram coui	nter	0 0000	0 0000
8Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
8Ch	PIE1	—	CMIE	—	—	—	—	—	—	-0	-0
8Dh	Unimplemented									_	_
8Eh	PCON	_	_	_	_	—	—	POR	BOR	0x	uq
8Fh-9Eh	Unimplemented						-		-	_	_
9Fh	VRCON	VREN	VROE	VRR	_	VR3	VR2	VR1	VR0	000- 0000	000- 0000

TABLE 4-1: SPECIAL REGISTERS FOR THE PIC16C62X

Legend: — = Unimplemented locations read as '0', u = unchanged, x = unknown,

 ${\rm q}$  = value depends on condition, shaded = unimplemented

**Note 1:** Other (non Power-up) Resets include MCLR Reset, Brown-out Reset and Watchdog Timer Reset during normal operation.

2: IRP & RP1 bits are reserved; always maintain these bits clear.

#### 4.2.2.6 PCON Register

The PCON register contains flag bits to differentiate between a Power-on Reset, an external MCLR Reset, WDT Reset or a Brown-out Reset.

Note:	BOR is unknown on Power-on Reset. It					
	must then be set by the user and checked					
	on subsequent RESETS to see if BOR is					
	cleared, indicating a brown-out has					
	occurred. The $\overline{\text{BOR}}$ STATUS bit is a "don't					
	care" and is not necessarily predictable if					
	the brown-out circuit is disabled (by					
	programming BODEN bit in the					
	Configuration word).					

#### REGISTER 4-6: PCON REGISTER (ADDRESS 8Eh)

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	POR	BOR
bit 7							bit 0

bit 7-2 Unimplemented: Read as '0'

bit 1 **POR**: Power-on Reset STATUS bit

- 1 = No Power-on Reset occurred
- 0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)

bit 0 **BOR**: Brown-out Reset STATUS bit

1 = No Brown-out Reset occurred

0 = A Brown-out Reset occurred (must be set in software after a Brown-out Reset occurs)

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented	bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

#### TABLE 5-1:PORTA FUNCTIONS

Name	Bit #	Buffer Type	Function
RA0/AN0	bit0	ST	Input/output or comparator input
RA1/AN1	bit1	ST	Input/output or comparator input
RA2/AN2/VREF	bit2	ST	Input/output or comparator input or VREF output
RA3/AN3	bit3	ST	Input/output or comparator input/output
RA4/T0CKI	bit4	ST	Input/output or external clock input for TMR0 or comparator output. Output is open drain type.

Legend: ST = Schmitt Trigger input

### TABLE 5-2: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Value on All Other RESETS
05h	PORTA		_		RA4	RA3	RA2	RA1	RA0	x 0000	u 0000
85h	TRISA	_	_	_	TRISA 4	TRISA 3	TRISA 2	TRISA 1	TRISA 0	1 1111	1 1111
1Fh	CMCON	C2OUT	C1OUT	_	_	CIS	CM2	CM1	CM0	00 0000	00 0000
9Fh	VRCON	VREN	VROE	VRR	_	VR3	VR2	VR1	VR0	000- 0000	000- 0000

Legend: — = Unimplemented locations, read as '0', u = unchanged, x = unknown

Note: Shaded bits are not used by PORTA.

## 5.3 I/O Programming Considerations

#### 5.3.1 BI-DIRECTIONAL I/O PORTS

Any instruction which writes, operates internally as a read followed by a write operation. The BCF and BSF instructions, for example, read the register into the CPU, execute the bit operation and write the result back to the register. Caution must be used when these instructions are applied to a port with both inputs and outputs defined. For example, a BSF operation on bit5 of PORTB will cause all eight bits of PORTB to be read into the CPU. Then the BSF operation takes place on bit5 and PORTB is written to the output latches. If another bit of PORTB is used as a bi-directional I/O pin (e.g., bit0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and re-written to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the Input mode, no problem occurs. However, if bit0 is switched into Output mode later on, the content of the data latch may now be unknown.

Reading the port register reads the values of the port pins. Writing to the port register writes the value to the port latch. When using read-modify-write instructions (ex. BCF, BSF, etc.) on a port, the value of the port pins is read, the desired operation is done to this value, and this value is then written to the port latch.

Example 5-2 shows the effect of two sequential read-modify-write instructions (ex.,  ${\tt BCF}\,,\;\;{\tt BSF},\; etc.)$  on an I/O port

A pin actively outputting a Low or High should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output currents may damage the chip.

#### EXAMPLE 5-2: READ-MODIFY-WRITE INSTRUCTIONS ON AN I/O PORT

; Initial PORT settings:	PORTB<7:4> Inpu	ıts
;	PORTB<3:0> Outp	puts
; PORTB<7:6> have external ; connected to other circu	. pull-up and are uitry	not
;		
;	PORT latch PO	ORT pins
;		
	-	
BCF PORTB, 7	;01pp pppp 11	ipp pppp
BCF PORTB, 6	;10pp pppp 11	lpp pppp
BSF STATUS, RPO	;	
BCF TRISB, 7	;10pp pppp 11	lpp pppp
BCF TRISB, 6	;10pp pppp 10	)pp pppp
;		
; Note that the user may h	ave expected the	pin
; values to be 00pp pppp.	The 2nd BCF cause	ed
; RB7 to be latched as the	e pin value (High)	).

# 5.3.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 5-7). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should be such to allow the pin voltage to stabilize (load dependent) before the next instruction which causes that file to be read into the CPU is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or another instruction not accessing this I/O port.



#### FIGURE 5-7: SUCCESSIVE I/O OPERATION









The code example in Example 7-1 depicts the steps required to configure the comparator module. RA3 and RA4 are configured as digital output. RA0 and RA1 are configured as the V- inputs and RA2 as the V+ input to both comparators.

#### EXAMPLE 7-1: INITIALIZING COMPARATOR MODULE

MOVLW	0x03	;Init comparator mode
MOVWF	CMCON	;CM<2:0> = 011
CLRF	PORTA	;Init PORTA
BSF	STATUS, RPO	;Select Bank1
MOVLW	0x07	;Initialize data direction
MOVWF	TRISA	;Set RA<2:0> as inputs
		;RA<4:3> as outputs
		;TRISA<7:5> always read `0'
BCF	STATUS, RPO	;Select Bank 0
CALL	DELAY 10	;10µs delay
MOVF	CMCON,F	;Read CMCONtoend change condition
BCF	PIR1,CMIF	;Clear pending interrupts
BSF	STATUS, RPO	;Select Bank 1
BSF	PIE1,CMIE	;Enable comparator interrupts
BCF	STATUS, RPO	;Select Bank 0
BSF	INTCON, PEIE	;Enable peripheral interrupts
BSF	INTCON, GIE	;Global interrupt enable

# 7.2 Comparator Operation

A single comparator is shown in Figure 7-2 along with the relationship between the analog input levels and the digital output. When the analog input at VIN+ is less than the analog input VIN-, the output of the comparator is a digital low level. When the analog input at VIN+ is greater than the analog input VIN-, the output of the comparator is a digital high level. The shaded areas of the output of the comparator in Figure 7-2 represent the uncertainty due to input offsets and response time.

# 7.3 Comparator Reference

An external or internal reference signal may be used depending on the comparator Operating mode. The analog signal that is present at VIN- is compared to the signal at VIN+, and the digital output of the comparator is adjusted accordingly (Figure 7-2).





#### 7.3.1 EXTERNAL REFERENCE SIGNAL

When external voltage references are used, the comparator module can be configured to have the comparators operate from the same or different reference sources. However, threshold detector applications may require the same reference. The reference signal must be between VSs and VDD, and can be applied to either pin of the comparator(s).

#### 7.3.2 INTERNAL REFERENCE SIGNAL

The comparator module also allows the selection of an internally generated voltage reference for the comparators. Section 10, Instruction Sets, contains a detailed description of the Voltage Reference Module that provides this signal. The internal reference signal is used when the comparators are in mode CM<2:0>=010 (Figure 7-1). In this mode, the internal voltage reference is applied to the VIN+ pin of both comparators.

### 9.1 Configuration Bits

The configuration bits can be programmed (read as '0') or left unprogrammed (read as '1') to select various device configurations. These bits are mapped in program memory location 2007h.

The user will note that address 2007h is beyond the user program memory space. In fact, it belongs to the special test/configuration memory space (2000h - 3FFFh), which can be accessed only during programming.

#### REGISTER 9-1: CONFIGURATION WORD (ADDRESS 2007h)

CP1	CP0 (2)	CP1	CP0 (2)	CP1	CP0 (2)		BODEN	CP1	CP0 <sup>(2)</sup>	PWRTE	WDTE	F0SC1	F0SC0
bit 13			<u> </u>				<u> </u>		ļ	<u> </u>		<u> </u>	bit 0
bit 13-8 5-4:	B, CP Cod 10 = 01 = 00 = Cod 11 = 10 = 01 = 00 =	<b>1:0&gt;:</b> C e protec = Progra = 0400h- = 0200h- = 0000h- e protec = Progra = Progra = 0200h- = 0000h-	ode prote ction for 2 m memo -07FFh c -07FFh c -07FFh c ction for 1 m memo -03FFh c -03FFh c	ection bit 2K progr ory code ode prot ode prot ode prot ry code ory code ode prot ode prot	am mem protectio ected ected ected am mem protectio protectio ected ected	nory on off nory on off on off							
	Cod 11 = 10 = 01 = 00 =	e protec = Progra = Progra = Progra = 0000h-	ction for ( m memo m memo m memo -01FFh c	).5K prop ory code ory code ory code ode prot	gram me protectio protectio protectio	emory on off on off on off							
bit 7	Uniı	npleme	e <b>nted</b> : Re	ead as 'C	)'								
bit 6	BOI	DEN: Br	own-out	Reset E	nable bit	(1)							
	1 = 0 =	BOR en BOR dis	abled sabled										
bit 3	<b>PWI</b> 1 = 0 =	<b>PWRTE</b> : Power-up Timer Enable bit <sup>(1, 3)</sup> 1 = PWRT disabled 0 = PWRT enabled											
bit 2	<b>WD</b> 1 = ' 0 = '	TE: Wat WDT en WDT dis	chdog Ti iabled sabled	mer Ena	ble bit								
bit 1-0	FOS	C1:FO	SC0: Oso	cillator S	election	bits							
	11 = 10 = 01 = 00 =	= RC oso = HS oso = XT oso = LP oso	cillator cillator cillator cillator										
	Note	e 1: Er va er 2: Al lis	nabling B alue of bit nabled. I of the C ited.	PWRTE PWRTE P<1:0>	it Reset E. Ensur pairs ha	automa e the Po ve to be	tically ena ower-up Ti given the	bles Pov mer is e same va	wer-up T nabled a alue to er	imer (PWF nytime Bro nable the o	RT) rega own-out l code prot	rdless of Detect R tection so	the eset is cheme
		J. U	nprogram	ineu pa	ns ueidi	ait tile P	ower-up I		auleu.				
Legend	:												
R = Re	adable b	it		W = '	Writable	bit	U =	Unimple	emented	bit. read a	s '0'		

#### 9.5.1 RB0/INT INTERRUPT

External interrupt on RB0/INT pin is edge triggered, either rising if INTEDG bit (OPTION<6>) is set, or falling, if INTEDG bit is clear. When a valid edge appears on the RB0/INT pin, the INTF bit (INTCON<1>) is set. This interrupt can be disabled by clearing the INTE control bit (INTCON<4>). The INTF bit must be cleared in software in the interrupt service routine before reenabling this interrupt. The RB0/INT interrupt can wake-up the processor from SLEEP, if the INTE bit was set prior to going into SLEEP. The status of the GIE bit decides whether or not the processor branches to the interrupt vector following wake-up. See Section 9.8 for details on SLEEP and Figure 9-18 for timing of wakeup from SLEEP through RB0/INT interrupt.

#### 9.5.2 TMR0 INTERRUPT

An overflow (FFh  $\rightarrow$  00h) in the TMR0 register will set the T0IF (INTCON<2>) bit. The interrupt can be enabled/disabled by setting/clearing T0IE (INTCON<5>) bit. For operation of the Timer0 module, see Section 6.0.

#### 9.5.3 PORTB INTERRUPT

An input change on PORTB <7:4> sets the RBIF (INTCON<0>) bit. The interrupt can be enabled/disabled by setting/clearing the RBIE (INTCON<4>) bit. For operation of PORTB (Section 5.2).

Note:	If a change on the I/O pin should occur
	when the read operation is being executed
	(start of the Q2 cycle), then the RBIF
	interrupt flag may not get set.

#### 9.5.4 COMPARATOR INTERRUPT

See Section 7.6 for complete description of comparator interrupts.



#### FIGURE 9-16: INT PIN INTERRUPT TIMING

CLRW	Clear W	COMF	Complement f				
Syntax:	[label] CLRW	Syntax:	[ <i>label</i> ] COMF f,d				
Operands:	None	Operands:	$0 \leq f \leq 127$				
Operation:	$00h \rightarrow (W)$		d ∈ [0,1]				
	$1 \rightarrow Z$	Operation:	$(f) \rightarrow (dest)$				
Status Affected:	Z	Status Affected:	Z				
Encoding:	00 0001 0000 0011	Encoding:	00 1001 dfff ffff				
Description:	W register is cleared. Zero bit (Z) is set.	Description:	The contents of register 'f' are complemented. If 'd' is 0, the				
Words:	1		result is stored in W. If 'd' is 1, the				
Cycles:	1	Words:	1				
Example	CLRW						
	Before Instruction	Evernle	COME DECI 0				
	W = 0x5A	Example	Before Instruction REG1 = 0x13 After Instruction				
	W = 0x00						
	Z = 1						
			$\begin{array}{rcl} REG1 &= & 0x13 \\ W &= & 0xEC \end{array}$				
CLRWDT	Clear Watchdog Timer						
Svntax:	[label] CLRWDT						
<b>,</b>		DECF	Decrement f				
Operands:	None	DECF Syntax:	Decrement f				
Operands: Operation:	None $00h \rightarrow WDT$	DECF Syntax: Operands:	<b>Decrement f</b> [ <i>label</i> ] DECF f,d 0 < f < 127				
Operands: Operation:	None $00h \rightarrow WDT$ $0 \rightarrow WDT$ prescaler, $1 \rightarrow \overline{TO}$	DECF Syntax: Operands:	Decrement f[ label ]DECF f,d $0 \le f \le 127$ $d \in [0,1]$				
Operands: Operation:	None $00h \rightarrow WDT$ $0 \rightarrow WDT$ prescaler, $1 \rightarrow \overline{TO}$ $1 \rightarrow PD$	DECF Syntax: Operands: Operation:	Decrement f [ label ] DECF f,d $0 \le f \le 127$ $d \in [0,1]$ (f) - 1 $\rightarrow$ (dest)				
Operands: Operation: Status Affected:	None $00h \rightarrow WDT$ $0 \rightarrow WDT$ prescaler, $1 \rightarrow \overline{TO}$ $1 \rightarrow PD$ $\overline{TO}, PD$	DECF Syntax: Operands: Operation: Status Affected:	Decrement f [ <i>label</i> ] DECF f,d $0 \le f \le 127$ $d \in [0,1]$ (f) - 1 $\rightarrow$ (dest) Z				
Operands: Operation: Status Affected: Encoding:	None $00h \rightarrow WDT$ $0 \rightarrow WDT \text{ prescaler,}$ $1 \rightarrow \overline{TO}$ $1 \rightarrow PD$ $\overline{TO, PD}$ $00  0000  0110  0100$	DECF Syntax: Operands: Operation: Status Affected: Encoding:	Decrement f $[ label ]$ DECF f,d $0 \le f \le 127$ $d \in [0,1]$ $(f) - 1 \rightarrow (dest)$ Z $00$ 0011dfff				
Operands: Operation: Status Affected: Encoding: Description:	None $00h \rightarrow WDT$ $0 \rightarrow WDT \text{ prescaler,}$ $1 \rightarrow \overline{TO}$ $1 \rightarrow PD$ $\overline{TO, PD}$ $00  0000  0110  0100$ CLRWDT instruction resets the	DECF Syntax: Operands: Operation: Status Affected: Encoding: Description:	Decrement f $[label]$ DECF f,d $0 \le f \le 127$ $d \in [0,1]$ (f) - 1 $\rightarrow$ (dest)Z000011dfffDecrement register 'f'. If 'd' is 0,				
Operands: Operation: Status Affected: Encoding: Description:	None $00h \rightarrow WDT$ $0 \rightarrow WDT$ prescaler, $1 \rightarrow \overline{TO}$ $1 \rightarrow PD$ $\overline{TO}, \overline{PD}$ 00  0000  0110  0100 CLRWDT instruction resets the Watchdog Timer. It also resets the	DECF Syntax: Operands: Operation: Status Affected: Encoding: Description:	Decrement f $[ label ]$ DECF f,d $0 \le f \le 127$ $d \in [0,1]$ $(f) - 1 \rightarrow (dest)$ $Z$ $00$ $0011$ dfffffffDecrement register 'f'. If 'd' is 0,the result is stored in the W				
Operands: Operation: Status Affected: Encoding: Description:	None $00h \rightarrow WDT$ $0 \rightarrow WDT$ prescaler, $1 \rightarrow TO$ $1 \rightarrow PD$ TO, PD O CLRWDT instruction resets the Watchdog Timer. It also resets the prescaler of the WDT. STATUS bits TO and PD are set	DECF Syntax: Operands: Operation: Status Affected: Encoding: Description:	Decrement f $[label]$ DECF f,d $0 \le f \le 127$ $d \in [0,1]$ $(f) - 1 \rightarrow (dest)$ Z $00$ 0011dffffffDecrement register 'f'. If 'd' is 0,the result is stored in the Wregister. If 'd' is 1, the result isetared back in register 'f'				
Operands: Operation: Status Affected: Encoding: Description:	None $00h \rightarrow WDT$ $0 \rightarrow WDT prescaler,$ $1 \rightarrow TO$ $1 \rightarrow PD$ TO, PD 00  0000  0110  0100 CLRWDT instruction resets the Watchdog Timer. It also resets the pres <u>cal</u> er of the WDT. STATUS bits TO and PD are set.	DECF Syntax: Operands: Operation: Status Affected: Encoding: Description:	Decrement f[ label ] DECF f,d $0 \le f \le 127$ $d \in [0,1]$ (f) - 1 $\rightarrow$ (dest)Z000011dffffffDecrement register 'f'. If 'd' is 0,the result is stored in the Wregister. If 'd' is 1, the result isstored back in register 'f'.1				
Operands: Operation: Status Affected: Encoding: Description: Words:	None $00h \rightarrow WDT$ $0 \rightarrow WDT$ prescaler, $1 \rightarrow \overline{TO}$ $1 \rightarrow PD$ $\overline{TO}, \overline{PD}$ OO 0000 0110 0100 CLRWDT instruction resets the Watchdog Timer. It also resets the prescaler of the WDT. STATUS bits TO and PD are set. 1	DECF Syntax: Operands: Operation: Status Affected: Encoding: Description: Words:	Decrement f $[ label ]$ DECF f,d $0 \le f \le 127$ $d \in [0,1]$ $(f) - 1 \rightarrow (dest)$ Z000011dfffffffDecrement register 'f'. If 'd' is 0,the result is stored in the Wregister. If 'd' is 1, the result isstored back in register 'f'.11				
Operands: Operation: Status Affected: Encoding: Description: Words: Cycles:	None $\begin{array}{l} 00h \rightarrow WDT \\ 0 \rightarrow WDT \text{ prescaler,} \\ 1 \rightarrow \overline{TO} \\ 1 \rightarrow PD \\ \hline \overline{TO}, \overline{PD} \\ \hline \hline 00 & 0000 & 0110 & 0100 \\ \hline \end{array}$ CLRWDT instruction resets the Watchdog Timer. It also resets the prescaler of the WDT. STATUS bits TO and PD are set. 1 1	DECF Syntax: Operands: Operation: Status Affected: Encoding: Description: Words: Cycles:	Decrement f $[label]$ DECF f,d $0 \le f \le 127$ $d \in [0,1]$ $(f) - 1 \rightarrow (dest)$ Z $00$ $0011$ dffffffDecrement register 'f'. If 'd' is 0,the result is stored in the Wregister. If 'd' is 1, the result isstored back in register 'f'.111				
Operands: Operation: Status Affected: Encoding: Description: Words: Cycles: Example	None $00h \rightarrow WDT$ $0 \rightarrow WDT prescaler,$ $1 \rightarrow TO$ $1 \rightarrow PD$ TO, PD 00  0000  0110  0100 CLRWDT instruction resets the Watchdog Timer. It also resets the pres <u>caler of the</u> WDT. STATUS bits TO and PD are set. 1 1 CLRWDT Defense landmention	DECF Syntax: Operands: Operation: Status Affected: Encoding: Description: Words: Cycles: Example	Decrement f $[ label ]$ DECF f,d $0 \le f \le 127$ $d \in [0,1]$ $(f) - 1 \rightarrow (dest)$ Z000011dfffffffDecrement register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.11DECFCNT, 1Decrement register				
Operands: Operation: Status Affected: Encoding: Description: Words: Cycles: Example	None $00h \rightarrow WDT$ $0 \rightarrow WDT prescaler,$ $1 \rightarrow TO$ $1 \rightarrow PD$ TO, PD 00  0000  0110  0100 CLRWDT instruction resets the Watchdog Timer. It also resets the prescaler of the WDT. STATUS bits TO and PD are set. 1 1 CLRWDT Before Instruction WDT counter = 2	DECF Syntax: Operands: Operation: Status Affected: Encoding: Description: Words: Cycles: Example	Decrement f         [ label ] DECF f,d $0 \le f \le 127$ $d \in [0,1]$ (f) - 1 → (dest)         Z         00       0011         dfff         Decrement register 'f'. If 'd' is 0,         the result is stored in the W         register. If 'd' is 1, the result is         stored back in register 'f'.         1         DECF       CNT, 1         Before Instruction         CNT       = 0x01				
Operands: Operation: Status Affected: Encoding: Description: Words: Cycles: Example	None $\begin{array}{l} 00h \rightarrow WDT \\ 0 \rightarrow WDT \ prescaler, \\ 1 \rightarrow \overline{TO} \\ 1 \rightarrow PD \\ \hline TO, PD \\ \hline 00 & 0000 & 0110 & 0100 \\ \hline \end{array}$ CLRWDT instruction resets the Watchdog Timer. It also resets the prescaler of the WDT. STATUS bits TO and PD are set. 1 1 CLRWDT Before Instruction WDT counter = ? After Instruction	DECF Syntax: Operands: Operation: Status Affected: Encoding: Description: Words: Cycles: Example	Decrement f[/abe/]DECF f,d $0 \le f \le 127$ $d \in [0,1]$ (f) - 1 $\rightarrow$ (dest)Z000011dfffffffDecrement register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.11DECFCNT, 1Before Instruction $CNT = 0x01$ $Z = 0$				
Operands: Operation: Status Affected: Encoding: Description: Words: Cycles: Example	None $00h \rightarrow WDT$ $0 \rightarrow WDT prescaler,$ $1 \rightarrow TO$ $1 \rightarrow PD$ TO, PD 00  0000  0110  0100 CLRWDT instruction resets the Watchdog Timer. It also resets the pres <u>caler</u> of the WDT. STATUS bits TO and PD are set. 1 1 CLRWDT Before Instruction WDT counter = ? After Instruction WDT counter = 0x00 WDT counter = 0x00	DECF Syntax: Operands: Operation: Status Affected: Encoding: Description: Words: Cycles: Example	Decrement f         [ label ] DECF f,d $0 \le f \le 127$ $d \in [0,1]$ (f) - 1 → (dest)         Z         00       0011         dfff       ffff         Decrement register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.         1       1         DECF       CNT, 1         Before Instruction         CNT       =         QNT       =         QNT       =         QNT       =				
Operands: Operation: Status Affected: Encoding: Description: Words: Cycles: Example	None $\begin{array}{c} 00h \rightarrow WDT \\ 0 \rightarrow WDT \ prescaler, \\ 1 \rightarrow TO \\ 1 \rightarrow PD \\ \hline TO, PD \\ \hline 00 & 0000 & 0110 & 0100 \\ \hline \\ CLRWDT \ instruction \ resets the \\ Watchdog Timer. It also resets the \\ Watchdog Timer. It also resets the \\ prescaler of the WDT. STATUS \\ bits TO and PD are set. \\ 1 \\ 1 \\ CLRWDT \\ \hline \\ Before \ Instruction \\ WDT \ counter \ = \ ? \\ After \ Instruction \\ WDT \ counter \ = \ 0 \\ \hline TO \ = \ 1 \end{array}$	DECF Syntax: Operands: Operation: Status Affected: Encoding: Description: Words: Cycles: Example	Decrement f $[label]$ DECF f,d $0 \le f \le 127$ $d \in [0,1]$ $(f) - 1 \rightarrow (dest)$ Z $00$ $0011$ dfffffDecrement register 'f'. If 'd' is 0,the result is stored in the Wregister. If 'd' is 1, the result isstored back in register 'f'.11DECFCNTCNT $Z$ $=$ 0After InstructionCNTCNT $CNT$ $CNT$ $T$ $0x00$ $Z$ $Z$ $T$				

## 11.9 MPLAB ICE 2000 High Performance Universal In-Circuit Emulator

The MPLAB ICE 2000 universal in-circuit emulator is intended to provide the product development engineer with a complete microcontroller design tool set for PICmicro microcontrollers. Software control of the MPLAB ICE 2000 in-circuit emulator is advanced by the MPLAB Integrated Development Environment, which allows editing, building, downloading and source debugging from a single environment.

The MPLAB ICE 2000 is a full-featured emulator system with enhanced trace, trigger and data monitoring features. Interchangeable processor modules allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the MPLAB ICE in-circuit emulator allows expansion to support new PICmicro microcontrollers.

The MPLAB ICE 2000 in-circuit emulator system has been designed as a real-time emulation system with advanced features that are typically found on more expensive development tools. The PC platform and Microsoft<sup>®</sup> Windows 32-bit operating system were chosen to best make these features available in a simple, unified application.

# 11.10 MPLAB ICE 4000 High Performance Universal In-Circuit Emulator

The MPLAB ICE 4000 universal in-circuit emulator is intended to provide the product development engineer with a complete microcontroller design tool set for highend PICmicro microcontrollers. Software control of the MPLAB ICE in-circuit emulator is provided by the MPLAB Integrated Development Environment, which allows editing, building, downloading and source debugging from a single environment.

The MPLAB ICD 4000 is a premium emulator system, providing the features of MPLAB ICE 2000, but with increased emulation memory and high speed performance for dsPIC30F and PIC18XXXX devices. Its advanced emulator features include complex triggering and timing, up to 2 Mb of emulation memory, and the ability to view variables in real-time.

The MPLAB ICE 4000 in-circuit emulator system has been designed as a real-time emulation system with advanced features that are typically found on more expensive development tools. The PC platform and Microsoft Windows 32-bit operating system were chosen to best make these features available in a simple, unified application.

# 11.11 MPLAB ICD 2 In-Circuit Debugger

Microchip's In-Circuit Debugger, MPLAB ICD 2, is a powerful, low cost, run-time development tool, connecting to the host PC via an RS-232 or high speed USB interface. This tool is based on the FLASH PICmicro MCUs and can be used to develop for these and other PICmicro microcontrollers. The MPLAB ICD 2 utilizes the in-circuit debugging capability built into the FLASH devices. This feature, along with Microchip's In-Circuit Serial Programming<sup>™</sup> (ICSP<sup>™</sup>) protocol, offers cost effective in-circuit FLASH debugging from the graphical user interface of the MPLAB Integrated Development Environment. This enables a designer to develop and debug source code by setting breakpoints, single-stepping and watching variables, CPU status and peripheral registers. Running at full speed enables testing hardware and applications in real-time. MPLAB ICD 2 also serves as a development programmer for selected PICmicro devices.

## 11.12 PRO MATE II Universal Device Programmer

The PRO MATE II is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features an LCD display for instructions and error messages and a modular detachable socket assembly to support various package types. In Stand-Alone mode, the PRO MATE II device programmer can read, verify, and program PICmicro devices without a PC connection. It can also set code protection in this mode.

### 11.13 PICSTART Plus Development Programmer

The PICSTART Plus development programmer is an easy-to-use, low cost, prototype programmer. It connects to the PC via a COM (RS-232) port. MPLAB Integrated Development Environment software makes using the programmer simple and efficient. The PICSTART Plus development programmer supports most PICmicro devices up to 40 pins. Larger pin count devices, such as the PIC16C92X and PIC17C76X, may be supported with an adapter socket. The PICSTART Plus development programmer is CE compliant.





**2**: The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.













Parameter No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
10*	TosH2ckL	OSC1↑ to CLKOUT↓ <sup>(1)</sup>		75 —	200 400	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
11*	TosH2ck H	OSC1↑ to CLKOUT↑ <sup>(1)</sup>	_	75 —	200 400	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
12*	TckR	CLKOUT rise time <sup>(1)</sup>		35 —	100 200	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
13*	TckF	CLKOUT fall time <sup>(1)</sup>		35 —	100 200	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
14*	TckL2ioV	CLKOUT $\downarrow$ to Port out valid <sup>(1)</sup>	_	—	20	ns	
15*	TioV2ckH	Port in valid before CLKOUT ↑ <sup>(1)</sup>	Tosc +200 ns Tosc +400 ns	_	_	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
16*	TckH2iol	Port in hold after CLKOUT $\uparrow^{(1)}$	0	—		ns	
17*	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid	_	50	150 300	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
18*	TosH2iol	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	100 200	_	_	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
19*	TioV2osH	Port input valid to OSC1 <sup>↑</sup> (I/O in setup time)	0	—	—	ns	
20*	TioR	Port output rise time	_	10 —	40 80	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
21*	TioF	Port output fall time	_	10 —	40 80	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
22*	Tinp	RB0/INT pin high or low time	25 40	_	_	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
23	Trbp	RB<7:4> change interrupt high or low time	Тсү	—	—	ns	

# TABLE 12-4: CLKOUT AND I/O TIMING REQUIREMENTS

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.

# 13.0 DEVICE CHARACTERIZATION INFORMATION

The graphs and tables provided in this section are for design guidance and are not tested. In some graphs or tables, the data presented is outside specified operating range (e.g., outside specified VDD range). This is for information only and devices will operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. "Typical" represents the mean of the distribution, while "max" or "min" represents (mean +  $3\sigma$ ) and (mean -  $3\sigma$ ) respectively, where  $\sigma$  is standard deviation.



FIGURE 13-1: IDD VS. FREQUENCY (XT MODE, VDD = 5.5V)

FIGURE 13-2: PIC16C622A IPD VS. VDD (WDT DISABLE)



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# 18-Lead Plastic Small Outline (SO) - Wide, 300 mil (SOIC)







		INCHES*		MILLIMETERS			
Dimension	MIN	NOM	MAX	MIN	NOM	MAX	
Number of Pins	n		18			18	
Pitch	р		.050			1.27	
Overall Height	А	.093	.099	.104	2.36	2.50	2.64
Molded Package Thickness	A2	.088	.091	.094	2.24	2.31	2.39
Standoff §	A1	.004	.008	.012	0.10	0.20	0.30
Overall Width	E	.394	.407	.420	10.01	10.34	10.67
Molded Package Width	E1	.291	.295	.299	7.39	7.49	7.59
Overall Length	D	.446	.454	.462	11.33	11.53	11.73
Chamfer Distance	h	.010	.020	.029	0.25	0.50	0.74
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	ф	0	4	8	0	4	8
Lead Thickness	С	.009	.011	.012	0.23	0.27	0.30
Lead Width	В	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

\* Controlling Parameter § Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side. JEDEC Equivalent: MS-013

Drawing No. C04-051

20-Lead Plastic Shrink Small Outline (SS) - 209 mil, 5.30 mm (SSOP)



		INCHES*		MILLIMETERS			
Dimension	MIN	NOM	MAX	MIN	NOM	MAX	
Number of Pins	n		20			20	
Pitch	р		.026			0.65	
Overall Height	Α	.068	.073	.078	1.73	1.85	1.98
Molded Package Thickness	A2	.064	.068	.072	1.63	1.73	1.83
Standoff §	A1	.002	.006	.010	0.05	0.15	0.25
Overall Width	E	.299	.309	.322	7.59	7.85	8.18
Molded Package Width	E1	.201	.207	.212	5.11	5.25	5.38
Overall Length	D	.278	.284	.289	7.06	7.20	7.34
Foot Length	L	.022	.030	.037	0.56	0.75	0.94
Lead Thickness	С	.004	.007	.010	0.10	0.18	0.25
Foot Angle	¢	0	4	8	0.00	101.60	203.20
Lead Width	В	.010	.013	.015	0.25	0.32	0.38
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

\* Controlling Parameter § Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side. JEDEC Equivalent: MO-150 Drawing No. C04-072

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