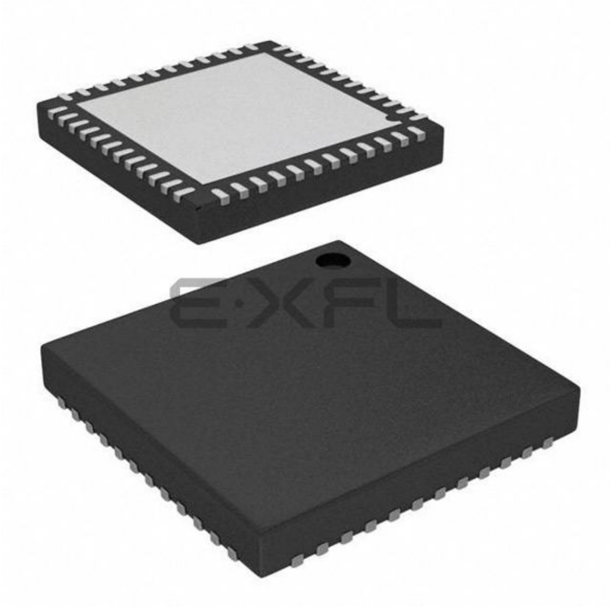
Infineon Technologies - CY7C64355-48LFXC Datasheet



Welcome to E-XFL.COM

Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

What Are Embedded - Microcontrollers - Application Specific?

Application specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	USB Microcontroller
Core Processor	M8C
Program Memory Type	FLASH (16kB)
Controller Series	CY7C643xx
RAM Size	1K x 8
Interface	I²C, SPI, USB
Number of I/O	36
Voltage - Supply	3V ~ 5.5V
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy7c64355-48lfxc

Email: info@E-XFL.COM Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Functional Overview

The enCoRe V family of devices are designed to replace multiple traditional full-speed USB microcontroller system components with one, low cost single-chip programmable component. Communication peripherals (I2C/SPI), a fast CPU, Flash program memory, SRAM data memory, and configurable IO are included in a range of convenient pinouts.

The architecture for this device family, as illustrated (enCoRe V), is comprised of three main areas: the CPU core, the system resources, and the full-speed USB system. Depending on the enCoRe V package, up to 36 general purpose IO (GPIO) are also included.

This product is an enhanced version of Cypress' successful full-speed USB peripheral controllers. Enhancements include faster CPU at lower voltage operation, lower current consumption, twice the RAM and Flash, hot-swapable IOs, I2C hardware address recognition, new very low current sleep mode, and new package options.

The enCoRe V Core

The enCoRe V Core is a powerful engine that supports a rich instruction set. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, and IMO (internal main oscillator) and ILO (internal low speed oscillator). The CPU core, called the M8C, is a powerful processor with speeds up to 24 MHz. The M8C is a four-MIPS, 8-bit Harvard architecture microprocessor.

System resources provide additional capability, such as a configurable I2C slave/SPI master-slave communication interface and various system resets supported by the M8C.

Additional System Resources

System resources, some of which have been previously listed, provide additional capability useful to complete systems. Additional resources include low voltage detection and power on reset. Brief statements describing the merits of each system resource are presented below.

- Full-speed USB (12 Mbps) with nine configurable endpoints and 512 bytes of dedicated USB RAM. No external components are required except two series resistors. It is specified for commercial temperature USB operation. For reliable USB operation, ensure the supply voltage is between 4.35V and 5.25V, or around 3.3V.
- 10-bit on-chip ADC shared between system performance manager (used to calculate parameters based on temperature for flash write operations) and the user.
- The I2C slave/SPI master-slave module provides 50/100/400 kHz communication over two wires. SPI communication over 3 or 4 wires runs at speeds of 46.9 kHz to 3 MHz (lower for a slower system clock).
- In the case of I2C slave mode, the hardware address recognition feature reduces the already low power consumption by eliminating the need for CPU intervention until a packet addressed to the target device has been received.
- Low Voltage Detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced POR (power on reset) circuit eliminates the need for a system supervisor.
- The 5V maximum input, 1.8/2.5/3V-selectable output, low-dropout regulator (LDO) provides regulation for IOs. A register controlled bypass mode allows the user to disable the LDO.
- Standard Cypress PSoC IDE tools are available for debugging the enCoRe V family of parts.

Getting Started

The quickest path to understanding the enCoRe V silicon is by reading this data sheet and using the PSoC Designer Integrated Development Environment (IDE). This data sheet is an overview of the enCoRe V integrated circuit and presents specific pin, register, and electrical specifications.

For up-to-date ordering, packaging, and electrical specification information, reference the latest enCoRe V device data sheets on the web at http://www.cypress.com.

Development Kits

Development Kits are available from the following distributors: Digi-Key, Avnet, Arrow, and Future. The Cypress Online Store contains development kits, **C** compilers, and all accessories for PSoC development. Go to the Cypress Online Store web site at http://www.cypress.com, click the Online Store shopping cart icon at the bottom of the web page, and click **USB (Universal Serial Bus)** to view a current list of available items.

Technical Training

Free PSoC and USB technical training is available for beginners and is taught by a marketing or application engineer over the phone. PSoC training classes cover designing, debugging, advanced analog, as well as application-specific classes covering topics such as PSoC, USB and the LIN bus. Go to http://www.cypress.com, click on Design Support located on the left side of the web page, and select **Technical Training** for more details.

Consultants

Certified Cypress USB Consultants offer everything from technical assistance to completed USB designs. To contact or become a Cypress PSoC/USB Consultant go to http://www.cypress.com, click on **Design Support** located on the left side of the web page, and select **CYPros Consultants**.

Technical Support

Cypress application engineers take pride in fast and accurate response. You can reach them with a 4-hour guaranteed response at http://www.cypress.com/support/login.cfm.

Application Notes

Many application notes are available to assist you in every aspect of your design effort. To view the USB application notes, go to the http://www.cypress.com web site and select **Application Notes** under the Design Resources list located in the center of the web page. By default, application notes are sorted by date .

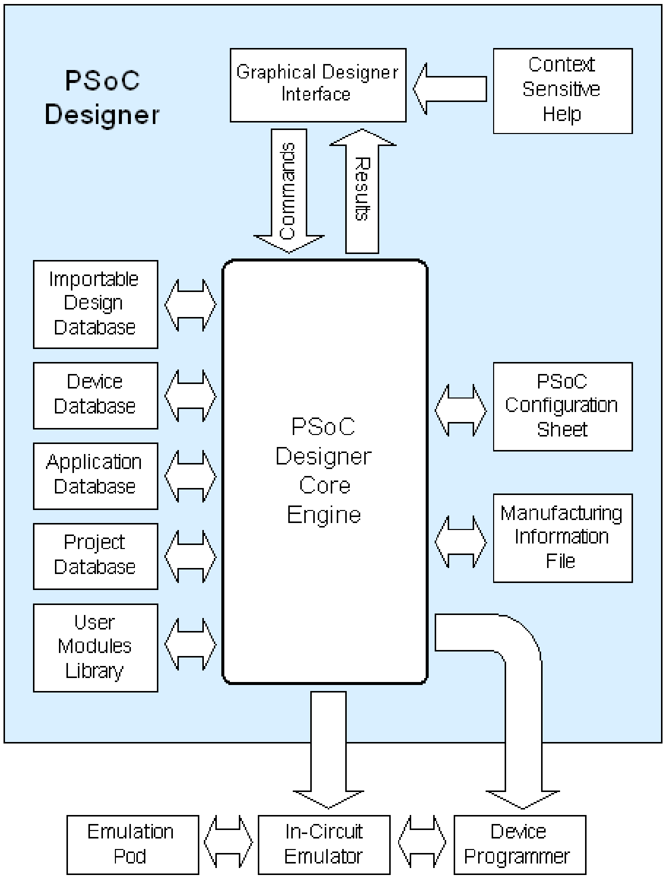
Development Tools

PSoC Designer is a Microsoft Windows-based, integrated development environment for the Programmable System-on-Chip (PSoC) devices. The PSoC Designer IDE and application runs on Windows NT 4.0, Windows 2000, Windows Millennium (Me), or Windows XP. (Reference the PSoC Designer Functional Flow diagram below.)

PSoC Designer helps the customer to select an operating configuration for the USB, write application code that uses the USB, and debug the application. This system provides design database management by project, an integrated debugger with In-Circuit Emulator, in-system programming support, and the CYASM macro assembler for the CPUs.

PSoC Designer also supports a high-level C language compiler developed specifically for the devices in the family.

Figure 1. PSoC Designer Subsystems



PSoC Designer Software Subsystems

Device Editor

The device editor subsystem allows the user to select different onboard analog and digital components called user modules using the enCoRe V device blocks. Examples of user modules are timers, 10-bit ADC, SPI/I2C etc.

The device editor also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration allows for changing configurations at run time.

PSoC Designer sets up power-on initialization tables for selected enCoRe V block configurations and creates source code for an application framework. The framework contains software to operate the selected components and, if the project uses more than one operating configuration, contains routines to switch between different sets of enCoRe V block configurations at run time. PSoC Designer can print out a configuration sheet for a given project configuration for use during application programming in conjunction with the Device Data Sheet. Once the framework is generated, the user can add application-specific code to flesh out the framework. It is also possible to change the selected components and regenerate the framework.

Application Editor

In the Application Editor you can edit your C language and Assembly language source code. You can also assemble, compile, link, and build.

Assembler. The macro assembler allows the merging of assembly code seamlessly with C code. The link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compiler. A C language compiler is available that supports the enCoRe V family of devices. Even if you have never worked in the C language before, the product quickly allows you to create complete C programs for the enCoRe V family devices.

The embedded, optimizing C compiler provides all the features of C tailored to the enCoRe V architecture. It comes complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

The PSoC Designer Debugger subsystem provides hardware in-circuit emulation, allowing the designer to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow the designer to read the program and read and write data memory, read and write IO registers, read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows the designer to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help for the user. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer in getting started.

Hardware Tools

In-Circuit Emulator

A low cost, high functionality ICE (In-Circuit Emulator) is available for development support. This hardware has the capability to program single devices.

The emulator consists of a base unit that connects to the PC by way of a USB port. The base unit is universal and operates with most Cypress USB and all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the enCoRe V device in the target board and performs full-speed (24 MHz) operation.

Designing with User Modules

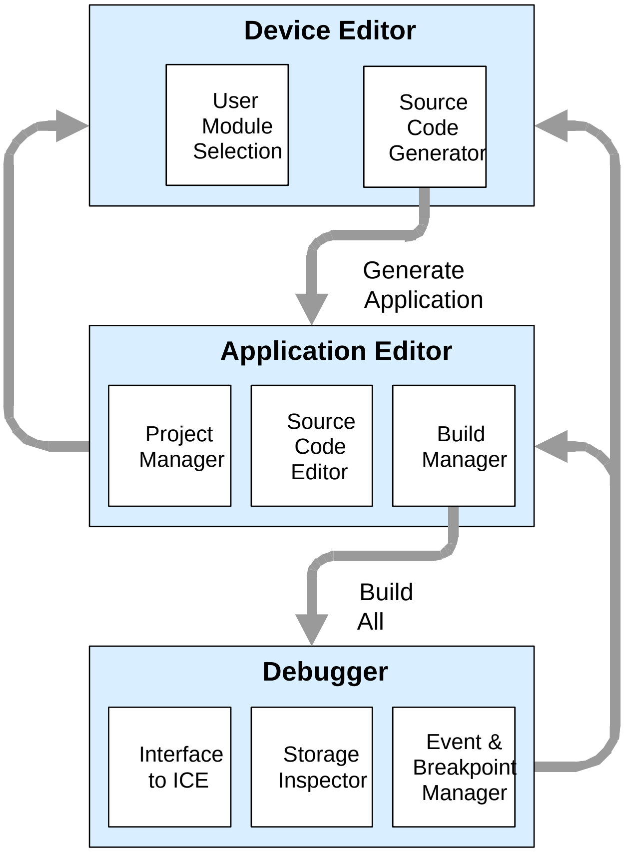
To speed the development process, the PSoC Designer Integrated Development Environment (IDE) provides a feature where the resources of the part are selected as user modules. For example, the timers, I2C, SPI resources are available as user modules. User modules make selecting and implementing peripheral devices simple and easy.

Each user module establishes the basic register settings that implement the selected function. It also provides parameters that allow you to tailor its precise configuration to your particular application. User modules also provide tested software to cut your development time. The user module application programming interface (API) provides high-level functions to control and respond to hardware events at run time. The API also provides optional interrupt service routines that you can adapt as needed.

The API functions are documented in user module data sheets that are viewed directly in the PSoC Designer IDE. These data sheets explain the internal operation of the user module and provide performance specifications. Each data sheet describes the use of each user module parameter and documents the setting of each register controlled by the user module.

The development process starts when you open a new project and bring up the Device Editor, a graphical user interface (GUI) for configuring the hardware. You pick and place the user modules you need for your project. The tool automatically builds signal chains by connecting user modules to the default IO pins or as required. At this stage, you also configure the clock source connections and enter parameter values directly or by selecting values from drop-down menus. When you are ready to test the hardware configuration or move on to developing code for the project, you perform the “Generate Application” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the high-level user module API functions.

Figure 2. User Module and Source Code Development Flows



The next step is to write your main program, and any sub-routines using PSoC Designer’s Application Editor subsystem. The Application Editor includes a Project Manager that allows you to open the project source code files (including all generated code files) from a hierarchal view. The source code editor provides syntax coloring and advanced edit features for both C and assembly language. File search capabilities include simple string searches and recursive “grep-style” patterns. A single mouse click invokes the Build Manager. It employs a professional-strength “makefile” system to automatically analyze all file dependencies and run the compiler and assembler as necessary. Project-level options control optimization strategies used by the compiler and linker. Syntax errors are displayed in a console window. Double clicking the error message takes you directly to the offending line of source code. When all is correct, the linker builds a HEX file image suitable for programming.

The last step in the development process takes place inside the PSoC Designer’s Debugger subsystem. The Debugger downloads the HEX image to the In-Circuit Emulator (ICE) where it runs at full-speed. Debugger capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint and watch-variable features, the Debugger provides a large trace buffer and allows you define complex breakpoint events that include monitoring address and data bus values, memory locations and external signals.

Document Conventions

Acronyms Used

The following table lists the acronyms that are used in this document.

Acronym	Description
API	application programming interface
CPU	central processing unit
GPIO	general purpose IO
GUI	graphical user interface
ICE	in-circuit emulator
ILO	internal low speed oscillator
IMO	internal main oscillator
IO	input/output
LSb	least-significant bit
LVD	low voltage detect
MSb	most-significant bit
POR	power on reset
PPOR	precision power on reset
PSoC®	Programmable System-on-Chip™
SLIMO	slow IMO
SRAM	static random access memory

Units of Measure

A units of measure table is located in the Electrical Specifications section. Table 5 on page 15 lists all the abbreviations used to measure the enCoRe V devices.

Numeric Naming

Hexidecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexidecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (e.g., 01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’, ‘b’, or 0x are decimal.

Pin Configuration

The enCoRe V USB device is available in a variety of packages which are listed and illustrated in the subsequent tables.

16-Pin Part Pinout

Figure 3. CY7C64315/CY7C64316 16-Pin enCoRe V Device

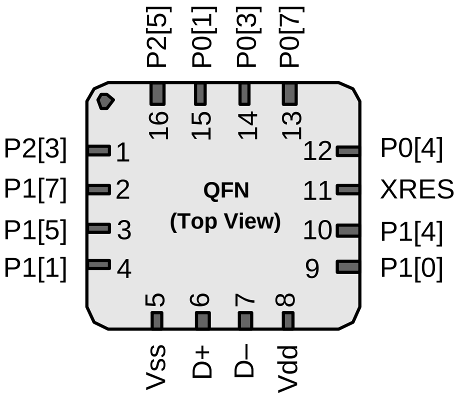


Table 1. 16-Pin Part Pinout (QFN)

Pin No.	Type	Name	Description
	Digital		
1	IO	P2[3]	Digital IO, Crystal Input (Xin)
2	IOHR	P1[7]	Digital IO, SPI SS, I2C SCL
3	IOHR	P1[5]	Digital IO, SPI MISO, I2C SDA
4	IOHR	P1[1](1)	Digital IO, ISSP CLK, 12C SCL, SPI MOSI
5	Power	Vss	Ground connection
6	USB line	D+	USB PHY
7	USB line	D–	USB PHY
8	Power	Vdd	Supply
9	IOHR	P1[0](1)	Digital IO, ISSP DATA, I2C SDA, SPI CLK
10	IOHR	P1[4]	Digital IO, optional external clock input (EXTCLK)
11	Input	XRES	Active high external reset with internal pull down
12	IOH	P0[4]	Digital IO
13	IOH	P0[7]	Digital IO
14	IOH	P0[3]	Digital IO
15	IOH	P0[1]	Digital IO
16	IO	P2[5]	Digital IO, Crystal Output (Xout)

LEDGEND I = Input, O = Outpit, OH = 5 mA High Output Drive, R = Regulated Output.

Note

1. These are the in-system serial programming (ISSP) pins, that are not High Z at power on reset (POR).

32-Pin Part Pinout

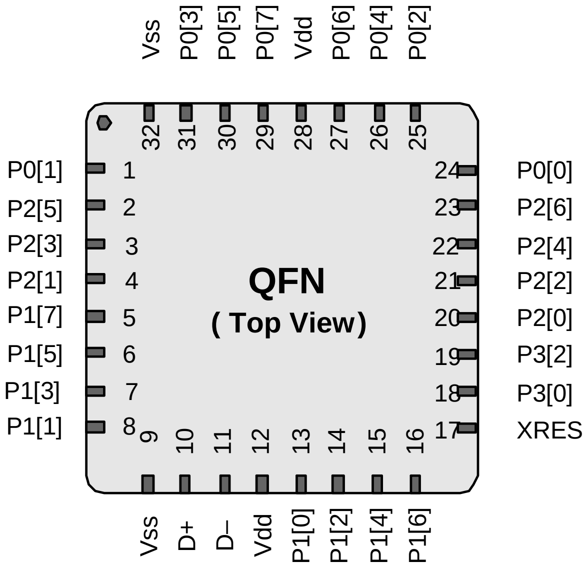


Figure 4. CY7C64345 32-Pin enCoRe V USB Device

Table 2. 32-Pin Part Pinout (QFN)

Pin No.	Type	Name	Description
1	IOH	P0[1]	Digital IO
2	IO	P2[5]	Digital IO, Crystal Output (Xout)
3	IO	P2[3]	Digital IO, Crystal Input (Xin)
4	IO	P2[1]	Digital IO
5	IOHR	P1[7]	Digital IO, I2C SCL, SPI SS
6	IOHR	P1[5]	Digital IO, I2C SDA, SPI MISO
7	IOHR	P1[3]	Digital IO, SPI CLK
8	IOHR	P1[1](2)	Digital IO, ISSP CLK, I2C SCL, SPI MOSI
9	Power	Vss	Ground
10	IO	D+	USB PHY
11	IO	D–	USB PHY
12	Power	Vdd	Supply voltage
13	IOHR	P1[0](2)	Digital IO, ISSP DATA, I2C SDA, SPI CLK
14	IOHR	P1[2]	Digital IO
15	IOHR	P1[4]	Digital IO, optional external clock input (EXTCLK)
16	IOHR	P1[6]	Digital IO
17	Reset	XRES	Active high external reset with internal pull down
18	IO	P3[0]	Digital IO
19	IO	P3[2]	Digital IO
20	IO	P2[0]	Digital IO
21	IO	P2[2]	Digital IO

Note

2. These are the in-system serial programming (ISSP) pins, that are not High Z at power on reset (POR).

Table 2. 32-Pin Part Pinout (QFN) (continued)

Pin No.	Type	Name	Description
22	IO	P2[4]	Digital IO
23	IO	P2[6]	Digital IO
24	IOH	P0[0]	Digital IO
25	IOH	P0[2]	Digital IO
26	IOH	P0[4]	Digital IO
27	IOH	P0[6]	Digital IO
28	Power	Vdd	Supply voltage
29	IOH	P0[7]	Digital IO
30	IOH	P0[5]	Digital IO
31	IOH	P0[3]	Digital IO
32	Power	Vss	Ground
CP	Power	Vss	Ensure the center pad is connected to ground

LEDGEND I = Input, O = Outpit, OH = 5 mA High Output Drive, R = Regulated Output.

48-Pin Part Pinout

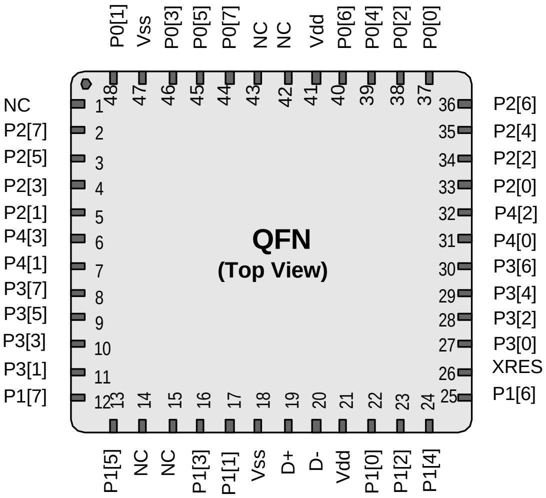


Figure 5. CY7C64355/CY7C64356 48-Pin enCoRe V USB Device

Table 3. 48-Pin Part Pinout (QFN)

Pin No.	Type	Pin Name	Description
1	NC	NC	No connection
2	IO	P2[7]	Digital IO
3	IO	P2[5]	Digital IO, Crystal Out (Xout)
4	IO	P2[3]	Digital IO, Crystal In (Xin)
5	IO	P2[1]	Digital IO
6	IO	P4[3]	Digital IO
7	IO	P4[1]	Digital IO
8	IO	P3[7]	Digital IO
9	IO	P3[5]	Digital IO
10	IO	P3[3]	Digital IO
11	IO	P3[1]	Digital IO
12	IOHR	P1[7]	Digital IO, I2C SCL, SPI SS
13	IOHR	P1[5]	Digital IO, I2C SDA, SPI MISO
14	NC	NC	No connection
15	NC	NC	No connection
16	IOHR	P1[3]	Digital IO, SPI CLK
17	IOHR	P1[1](3)	Digital IO, ISSP CLK, I2C SCL, SPI MOSI
18	Power	Vss	Supply ground
19	IO	D+	USB
20	IO	D–	USB
21	Power	Vdd	Supply voltage
22	IOHR	P1[0](3)	Digital IO, ISSP DATA, I2C SDA, SPI CLK

Note

3. These are the in-system serial programming (ISSP) pins, that are not High Z at power on reset (POR).

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
	23			63			A3		RES_WDT	E3	W
	24		PMA8_DR	64	RW		A4		INT_MSK3	E4	RW
	25		PMA9_DR	65	RW		A5			E5	
	26		PMA10_DR	66	RW		A6			E6	
	27		PMA11_DR	67	RW		A7			E7	
	28		PMA12_DR	68	RW		A8			E8	
SPI_TXR	29	W	PMA13_DR	69	RW		A9			E9	
SPI_RXR	2A	R	PMA14_DR	6A	RW		AA			EA	
SPI_CR	2B	#	PMA15_DR	6B	RW		AB			EB	
	2C		TMP_DR0	6C	RW		AC			EC	
	2D		TMP_DR1	6D	RW		AD			ED	
	2E		TMP_DR2	6E	RW		AE			EE	
	2F		TMP_DR3	6F	RW		AF			EF	
	30			70		PT0_CFG	B0	RW		F0	
USB_SOF0	31	R		71		PT0_DATA1	B1	RW		F1	
USB_SOF1	32	R		72		PT0_DATA0	B2	RW		F2	
USB_CR0	33	RW		73		PT1_CFG	B3	RW		F3	
USBIO_CR0	34	#		74		PT1_DATA1	B4	RW		F4	
USBIO_CR1	35	#		75		PT1_DATA0	B5	RW		F5	
EP0_CR	36	#		76		PT2_CFG	B6	RW		F6	
EP0_CNT0	37	#		77		PT2_DATA1	B7	RW	CPU_F	F7	RL
EP0_DR0	38	RW		78		PT2_DATA0	B8	RW		F8	
EP0_DR1	39	RW		79			B9			F9	
EP0_DR2	3A	RW		7A			BA			FA	
EP0_DR3	3B	RW		7B			BB			FB	
EP0_DR4	3C	RW		7C			BC			FC	
EP0_DR5	3D	RW		7D			BD			FD	
EP0_DR6	3E	RW		7E			BE		CPU_SCR1	FE	#
EP0_DR7	3F	RW		7F			BF		CPU_SCR0	FF	#

Gray fields are reserved; do not access these fields. # Access is bit specific.

Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW	PMA4_RA	40	RW		80			C0	
PRT0DM1	01	RW	PMA5_RA	41	RW		81			C1	
	02		PMA6_RA	42	RW		82			C2	
	03		PMA7_RA	43	RW		83			C3	
PRT1DM0	04	RW	PMA8_WA	44	RW		84			C4	
PRT1DM1	05	RW	PMA9_WA	45	RW		85			C5	
	06		PMA10_WA	46	RW		86			C6	
	07		PMA11_WA	47	RW		87			C7	
PRT2DM0	08	RW	PMA12_WA	48	RW		88			C8	
PRT2DM1	09	RW	PMA13_WA	49	RW		89			C9	
	0A		PMA14_WA	4A	RW		8A			CA	
	0B		PMA15_WA	4B	RW		8B			CB	
PRT3DM0	0C	RW	PMA8_RA	4C	RW		8C			CC	
PRT3DM1	0D	RW	PMA9_RA	4D	RW		8D			CD	
	0E		PMA10_RA	4E	RW		8E			CE	
	0F		PMA11_RA	4F	RW		8F			CF	
PRT4DM0	10	RW	PMA12_RA	50	RW		90			D0	
PRT4DM1	11	RW	PMA13_RA	51	RW		91			D1	
	12		PMA14_RA	52	RW		92			D2	
	13		PMA15_RA	53	RW		93			D3	
	14		EP1_CR0	54	#		94			D4	
	15		EP2_CR0	55	#		95			D5	
	16		EP3_CR0	56	#		96			D6	
	17		EP4_CR0	57	#		97			D7	
	18		EP5_CR0	58	#		98			D8	
	19		EP6_CRO	59	#		99			D9	
	1A		EP7_CR0	5A	#		9A			DA	
	1B		EP8_CR0	5B	#		9B			DB	
	1C			5C			9C		IO_CFG	DC	RW
	1D			5D			9D		OUT_P1	DD	RW
	1E			5E			9E			DE	
	1F			5F			9F			DF	
	20			60			A0		OSC_CR0	E0	RW
	21			61			A1		ECO_CFG	E1	#
	22			62			A2		OSC_CR2	E2	RW
	23			63			A3		VLT_CR	E3	RW
	24			64			A4		VLT_CMP	E4	R
	25			65			A5			E5	
	26			66			A6			E6	
	27			67			A7			E7	
	28			68			A8		IMO_TR	E8	W
SPI_CFG	29	RW		69			A9		ILO_TR	E9	W
	2A			6A			AA			EA	
	2B			6B			AB		SLP_CFG	EB	RW
	2C		TMP_DR0	6C	RW		AC		SLP_CFG2	EC	RW
	2D		TMP_DR1	6D	RW		AD		SLP_CFG3	ED	RW
	2E		TMP_DR2	6E	RW		AE			EE	
	2F		TMP_DR3	6F	RW		AF			EF	
USB_CR1	30	#		70			B0			F0	
	31			71			B1			F1	
	32			72			B2			F2	
USBIO_CR2	33	RW		73			B3			F3	
PMA0_WA	34	RW		74			B4			F4	
PMA1_WA	35	RW		75			B5			F5	
PMA2_WA	36	RW		76			B6			F6	
PMA3_WA	37	RW		77			B7		CPU_F	F7	RL
PMA4_WA	38	RW		78			B8			F8	
PMA5_WA	39	RW		79			B9			F9	

Gray fields are reserved; do not access these fields. # Access is bit specific.

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PMA6_WA	3A	RW		7A			BA			FA	
PMA7_WA	3B	RW		7B			BB			FB	
PMA0_RA	3C	RW		7C			BC			FC	
PMA1_RA	3D	RW		7D			BD			FD	
PMA2_RA	3E	RW		7E			BE			FE	
PMA3_RA	3F	RW		7F			BF			FF	

Gray fields are reserved; do not access these fields. # Access is bit specific.

Electrical Characteristics

Absolute Maximum Ratings

Storage Temperature (T_{STG}) (4)	-55^{o}C to 125^{o}C (Typical +25^{o}C)
Supply Voltage Relative to Vss (Vdd)	-0.5V to +6.0V
DC Input Voltage (V_{IO})	Vss - 0.5V to Vdd + 0.5V
DC Voltage Applied to Tri-state (V_{IOZ})	Vss - 0.5V to Vdd + 0.5V
Maximum Current into any Port Pin (I_{MIO})	-25mA to +50mA
Electro Static Discharge Voltage (ESD) (5)	2000V
Latch-up Current (LU) (6)	200mA

Operating Conditions

Ambient Temperature (T_A)	0^{o}C to 70^{o}C
Operational Die Temperature (T_J)(7)	0^{o}C to 85^{o}C

DC Electrical Characteristics

DC Chip-Level Specifications

Table 6 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 6. DC Chip-Level Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Vdd	Supply Voltage	See table titled DC POR and LVD Specifications on page 18.	3.0	–	5.5	V
I_{DD24}	Supply Current, IMO = 24 MHz	Conditions are Vdd = 3.0V, T_A = 25^{o}C, CPU = 24 MHz, No USB/I2C/SPI.	–	–	2.15	mA
I_{DD12}	Supply Current, IMO = 12 MHz	Conditions are Vdd = 3.0V, T_A = 25^{o}C, CPU = 12 MHz, No USB/I2C/SPI.	–	–	1.45	mA
I_{DD6}	Supply Current, IMO = 6 MHz	Conditions are Vdd = 3.0V, T_A = 25^{o}C, CPU = 6 MHz, No USB/I2C/SPI.	–	–	1.1	mA
I_{SB0}	Deep Sleep Current	Vdd = 3.0V, T_A = 25^{o}C, IO regulator turned off.	–	0.1	–	μA
I_{SB1}	Standby Current with POR, LVD and Sleep Timer	Vdd = 3.0V, T_A = 25^{o}C, IO regulator turned off.	–	–	1.5	μA

Notes

4. Higher storage temperatures reduce data retention time. Recommended Storage Temperature is +25°C ± 25°C. Extended duration storage temperatures above 85^{o}C degrade reliability.
5. Human Body Model ESD.
6. Per JESD78 standard.
7. The temperature rise from ambient to junction is package specific. See "Package Diagram" on page 22 for Thermal Impedances. The user must limit the power consumption to comply with this requirement.

Table 7. DC Characteristics – USB Interface

Symbol	Description	Conditions	Min	Typ	Max	Units
Rusbi	USB D+ pull up resistance	With idle bus	0.900	TBD	1.575	kΩ
Rusba	USB D+ pull up resistance	While receiving traffic	1.425	TBD	3.090	kΩ
Vohusb	Static Output High		2.8	TBD	3.6	V
Volusb	Static Output Low			TBD	0.3	V
Vdi	Differential Input Sensitivity		0.2	TBD		V
Vcm	Differential Input Common Mode Range		TBD	TBD	TBD	V
Vse	Single Ended Receiver Threshold		0.8	TBD	2.0	V
Cin	Transceiver Capacitance			TBD	50	pF
Iio	Hi-Z State Data Line Leakage	On D+ or D- line	TBD	TBD	TBD	uA
Rps2	PS/2 Pull-up resistance		3	TBD	7	kΩ
Rext	External USB Series Resistor	In series with each USB pin	23	TBD	25	Ω

DC General Purpose IO Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0V to 5.5V and 0°C $\leq T_A \leq$ 70°C. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 8. 3.0V and 5.5V DC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{PU}	Pull up resistor		4	5.6	8	kΩ
V_{OH1}	High Output Voltage Port 0, 2, or 3 Pins	OH ≤ 10 µA, Vdd ≥ 3.0V, maximum of 10 mA source current in all IOs.	Vdd - 0.2	–	–	V
V_{OH2}	High Output Voltage Port 0, 2, or 3 Pins	OH = 1mA Vdd > 3.0, maximum of 20 mA source current in all IOs.	Vdd - 0.9	–	–	V
V_{OH3}	High Output Voltage Port 1 Pins with LDO Regulator Disabled	OH < 10 µA, Vdd > 3.0V, maximum of 10 mA source current in all IOs.	Vdd - 0.2	–	–	V
V_{OH4}	High Output Voltage Port 1 Pins with LDO Regulator Disabled	OH = 5mA, Vdd > 3.0V, maximum of 20 mA source current in all IOs.	Vdd - 0.9	–	–	V
V_{OH5}	High Output Voltage Port 1 Pins with LDO Regulator Enabled	OH < 10µA, Vdd > 3.1V, maximum of 4 IOs all sourcing 5 mA.	2.85	3.0	3.15	V
V_{OH6}	High Output Voltage Port 1 Pins with LDO Regulator Enabled	OH = 5 mA, Vdd > 3.1V, maximum of 20 mA source current in all IOs.	2.2	–	–	V
V_{OL}	Low Output Voltage	OL = 20mA, Vdd > 3.3V, maximum of 60 mA sink current on even port pins (for example, P0[2] and P1[4]) and 60 mA sink current on odd port pins (for example, P0[3] and P1[5]).	–	–	0.75	V
V_{IL}	Input Low Voltage	Vdd = 3.3 to 5.5.	–	–	0.8	V
V_{IH}	Input High Voltage	Vdd = 3.3 to 5.5.	2.0	–		V
V_H	Input Hysteresis Voltage		50	60	200	mV
I_{IL}	Input Leakage (Absolute Value)		–	1	25	nA
C_{IN}	Capacitive Load on Pins as Input	Package and pin dependent. Temp = 25^{o}C.	0.5	1.7	5	pF
C_{OUT}	Capacitive Load on Pins as Output	Package and pin dependent. Temp = 25^{o}C.	0.5	1.7	5	pF

DC POR and LVD Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 9. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units
V_{PPOR}	Vdd Value for PPOR Trip PORLEV[1:0] = 10b, HPOR = 1	–	2.82	2.95	V
	Vdd Value for LVD Trip				
V_{LVD0}	VM[2:0] = 000b	–	–	–	–
V_{LVD1}	VM[2:0] = 001b	–	–	–	–
V_{LVD2}	M[2:0] = 010b[8]	2.85	2.92	2.99	V
V_{LVD3}	VM[2:0] = 011b	2.95	3.02	3.09	V
V_{LVD4}	VM[2:0] = 100b	3.06	3.13	3.20	V
V_{LVD5}	VM[2:0] = 101b	–	–	–	–
V_{LVD6}	VM[2:0] = 110b	–	–	–	–
V_{LVD7}	VM[2:0] = 111b	4.62	4.73	4.83	V

DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 10.DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units
Vdd_{IWRITE}	Supply Voltage for Flash Write Operations	3.0	–	–	V
I_{DDP}	Supply Current During Programming or Verify	–	5	25	mA
V_{ILP}	Input Low Voltage During Programming or Verify	–	–	V_{IL}	V
V_{IHP}	Input High Voltage During Programming or Verify	V_{IH}	–	–	V
I_{ILP}	Input Current when Applying Vilp to P1[0] or P1[1] During Programming or Verify[9]	–	–	0.2	mA
I_{IHP}	Input Current when Applying Vihp to P1[0] or P1[1] During Programming or Verify[10]	–	–	1.5	mA
V_{OLV}	Output Low Voltage During Programming or Verify	–	–	Vss + 0.75	V
V_{OHV}	Output High Voltage During Programming or Verify	Vdd - 1.0	–	Vdd	V
$Flash_{ENPB}$	Flash Write Endurance[11]	50,000	–	–	Cycles
$Flash_{DR}$	Flash Data Retention[12]	10	20	–	Years

Notes

[8] Always greater than 50 mV above V_{PPOR} (PORLEV = 10) for falling supply.
[9] Driving internal pull down resistor.
[10] Driving internal pull down resistor.
[11] Erase/write cycles per block.
[12] Following maximum Flash write cycles.

AC Electrical Characteristics

AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 11.AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units
F_{MAX}	Maximum Operating Frequency(13)	24	–	–	MHz
F_{CPU}	Maximum Processing Frequency(14)	24	–	–	MHz
F_{32K1}	Internal Low Speed Oscillator Frequency	30.4	32	33.6	kHz
F_{IMO24}	Internal Main Oscillator Stability for 24 MHz ± 5%(15)	22.8	24	25.2	MHz
F_{IMO12}	Internal Main Oscillator Stability for 12 MHz(16)	11.4	12	12.6	MHz
F_{IMO6}	Internal Main Oscillator Stability for 6 MHz(17)	5.7	6.0	6.3	MHz
DC_{IMO}	Duty Cycle of IMO	40	50	60	%
T_{RAMP}	Supply Ramp Time	0	–	–	µs

Table 12.AC Characteristics – USB Data Timings

Symbol	Description	Conditions	Min	Typ	Max	Units
Tdrate	Full-speed data rate	Average bit rate	12–0.25%	12	12 + 0.25	MHz
Tdjr1	Receiver data jitter tolerance	To next transition	-8	TBD	8	ns
Tdjr2	Receiver data jitter tolerance	To pair transition	-5	TBD	5	ns
Tudj1	Driver differential jitter	To next transition	-3.5	TBD	3.5	ns
Tudj2	Driver differential jitter	To pair transition	-4.0	TBD	4.0	ns
Tfdeop	Source jitter for differntial transition	To SE0 transition	-2	TBD	5	ns
Tfeopt	Source SE0 interval of EOP		160	TBD	175	ns
Tfeopr	Receiver SE0 interval of EOP		82	TBD		ns
Tfst	Width of SE0 interval during differential transition			TBD	14	ns

Table 13.AC Characteristics – USB Driver

Symbol	Description	Conditions	Min	Typ	Max	Units
Tr	Transition rise time	50 pF	4	TBD	20	ns
Tf	Transition fall time	50 pF	4	TBD	20	ns
TR	Rise/fall time matching		90.00	TBD	111.11	%
Vcrs	Output signal crossover voltage		1.3	TBD	2.0	V

Notes

13. Vdd = 3.0V and $T_J = 85^oC$, digital clocking functions.
14. Vdd = 3.0V and $T_J = 85^oC$, CPU speed.
15. Trimmed for 3.3V operation using factory trim values.
16. Trimmed for 3.3V operation using factory trim values.
17. Trimmed for 3.3V operation using factory trim values.

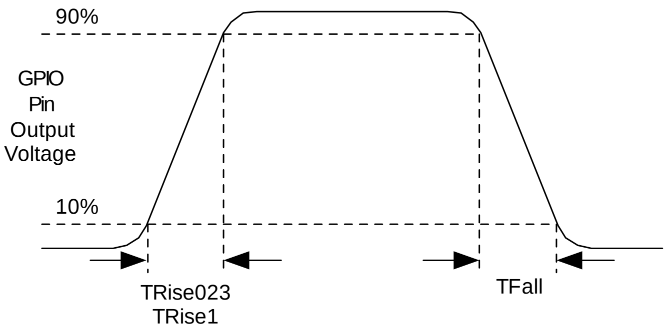
AC General Purpose IO Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 14.AC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{GPIO}	GPIO Operating Frequency	Normal Strong Mode, Port 1	0	–	12	MHz
TRise023	Rise Time, Strong Mode Ports 0, 2, 3	Vdd = 3.3 to 5.5V, 10% - 90%	15	–	80	ns
TRise1	Rise Time, Strong Mode Port 1	Vdd = 3.3 to 5.5V, 10% - 90%	7	–	50	ns
TFall	Fall Time, Strong Mode All Ports	Vdd = 3.3 to 5.5V, 10% - 90%	7	–	50	ns

Figure 8. GPIO Timing Diagram



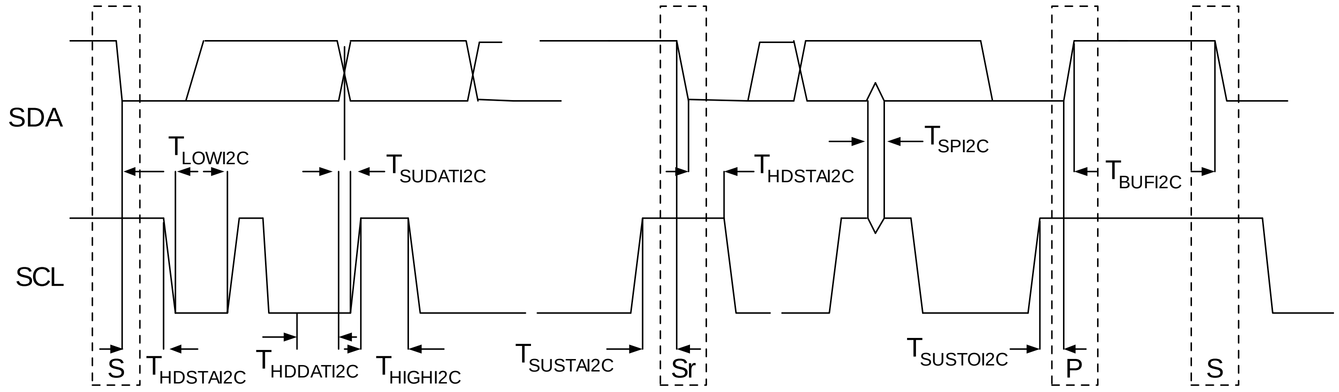
AC External Clock Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 15.AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units
F_{OSCEXT}	Frequency	0.750	–	25.2	MHz
–	High Period	20.6	–	5300	ns
–	Low Period	20.6	–	–	ns
–	Power Up IMO to Switch	150	–	–	µs

Figure 9. Definition for Timing for Fast/Standard Mode on the I²C Bus



Package Diagram

This chapter illustrates the packaging specifications for the enCoRe V USB device, along with the thermal impedances for each package.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the enCoRe V emulation tools and their dimensions, refer to the development kit.

Packaging Dimensions

Figure 10. 16-Lead (3x3 x 0.6 mm) QFN

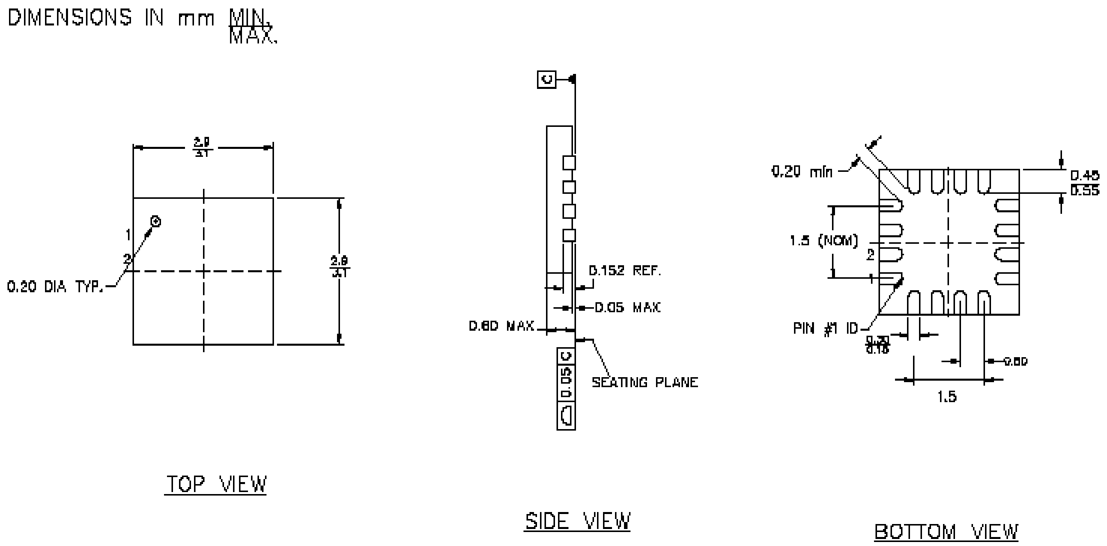
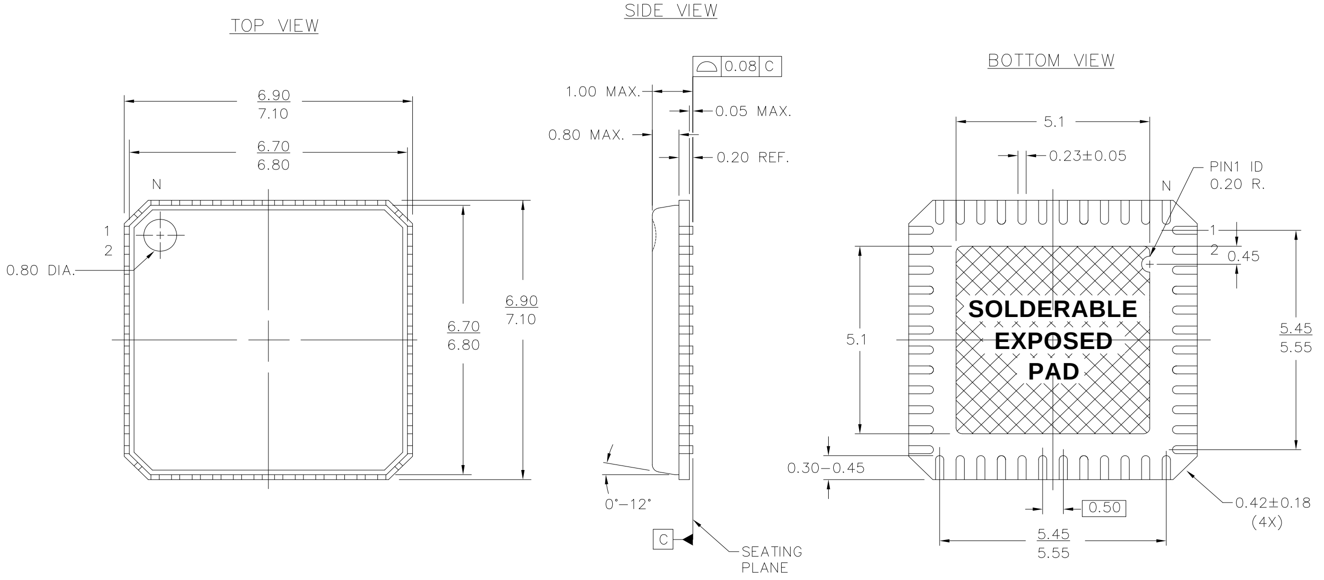


Figure 12. 48-Lead (7x7 mm) QFN



NOTES:

1. ▨ HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 0.13g
4. ALL DIMENSIONS ARE IN MM [MIN/MAX]
5. PACKAGE CODE

PART #	DESCRIPTION
LF48A	STANDARD
LY48A	LEAD FREE

001-12919 *A

.

Thermal Impedances

Table 19.Thermal Impedances per Package

Package	Typical θ_{JA} *
16 QFN	46 ^{o}C/W
32 QFN**	14.5 ^{o}C/W
48 QFN**	28 ^{o}C/W

***** $T_J = T_A$ + Power x θ_{JA}
** To achieve the thermal impedance specified for the ** package, solder the center thermal pad to the PCB ground plane.

Solder Reflow Peak Temperature

Following is the minimum solder reflow peak temperature to achieve good solderability.

Table 20.Solder Reflow Peak Temperature

Package	Minimum Peak Temperature*	Maximum Peak Temperature
16 QFN	240^{o}C	260^{o}C
32 QFN	240^{o}C	260^{o}C
48 QFN	240^{o}C	260^{o}C

*Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220 ± 5^{o}C with Sn-Pb or 245 ± 5^{o}C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

Ordering Information

Ordering Code	Package Information	Flash	SRAM	No. of GPIOs	Target Applications
CY7C64315-16LKXC	16-lead QFN (3x3x0.6mm)	16K	1K	11	Mid-tier FS USB dongle, RC-host module
CY7C64316-16LKXC	16-lead QFN (3x3x0.6mm)	32K	2K	11	Hi-end FS USB dongle, RC-host module
CY7C64345-32LKXC	32-lead QFN (5x5x0.6mm)	16K	1K	25	Full-speed USB mouse
CY7C64355-48LFXC	48-lead QFN (7x7x1.0mm)	16K	1K	36	Full-speed USB keyboard
CY7C64356-48LFXC	48-lead QFN (7x7x1.0mm)	32K	2K	36	Hi-End FS USB keyboard

Document History Page

Document Title: CY7C6431X, CY7C64345, CY7C6435X ENCORE TM V FULL-SPEED USB CONTROLLER **Document Number: 001-12394**			
REV.	**ECN.**	**Orig. of Change**	**Description of Change**
**	626256	TYJ	New data sheet.
*A	735718	TYJ/ARI	Filled in TBDs, added new block diagram, and corrected some values. Part numbers updated as per new specifications.
*B	1120404	ARI	Corrected the block diagram and Figure 3, which is the 16-pin enCoRe V device. Corrected the description to pin 29 on Table 2, the Typ/Max values for I_{SB0} on the DC chip-level specifications, the current value for the latch-up current in the Electrical Characteristics section, and corrected the 16 QFN package information in the Thermal Impedance table. Corrected some of the bulleted items on the first page. Added DC Characteristics–USB Interface table. Added AC Characteristics–USB Data Timings table. Added AC Characteristics–USB Driver table. Corrected Flash Write Endurance minimum value in the DC Programming Specifications table. Corrected the Flash Erase Time max value and the Flash Block Write Time max value in the AC Programming Specifications table. Implemented new latest template. Include paramters: Vcrs, Rpu (USB, active), Rpu (USB suspend), Tfdeop, Tfeopr2, Tfeopt, Tfst. Added register map tables. Corrected a value in the DC Chip-Level Specifications table.
*C	1241024	TYJ/ARI	Corrected Idd values in Table 6 - DC Chip-Level Specifications.
*D	1639963	AESA	Post to www.cypress.com

© Cypress Semiconductor Corporation, 2007. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.

PSoC Designer™, Programmable System-on-Chip™, and PSoC Express™ are trademarks and PSoC® is a registered trademark of Cypress Semiconductor Corp. All other trademarks or registered trademarks referenced herein are property of the respective corporations. Purchase of I2C components from Cypress or one of its sublicensed Associated Companies conveys a license under the Philips I2C Patent Rights to use these components in an I2C system, provided that the system conforms to the I2C Standard Specification as defined by Philips. All products and company names mentioned in this document may be the trademarks of their respective holders.