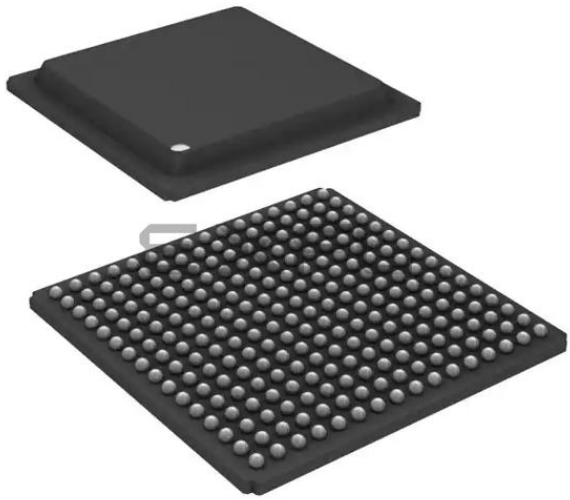

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	133MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (2)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 100°C (TA)
Security Features	-
Package / Case	256-BBGA
Supplier Device Package	256-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc870cvr133

  - HDLC bus (implements an HDLC-based local area network (LAN))
  - Asynchronous HDLC to support point-to-point protocol (PPP)
  - AppleTalk
  - Universal asynchronous receiver transmitter (UART)
  - Synchronous UART
  - Serial infrared (IrDA)
  - Binary synchronous communication (BISYNC)
  - Totally transparent (bit streams)
  - Totally transparent (frame based with optional cyclic redundancy check (CRC))
- SMC (serial management channel)
  - UART (low-speed operation)
  - Transparent
- Universal serial bus (USB)—Supports operation as a USB function endpoint, a USB host controller, or both for testing purposes (loopback diagnostics)
  - USB 2.0 full-/low-speed compatible
  - The USB function mode has the following features:
    - Four independent endpoints support control, bulk, interrupt, and isochronous data transfers
    - CRC16 generation and checking
    - CRC5 checking
    - NRZI encoding/decoding with bit stuffing
    - 12- or 1.5-Mbps data rate
    - Flexible data buffers with multiple buffers per frame
    - Automatic retransmission upon transmit error
  - The USB host controller has the following features:
    - Supports control, bulk, interrupt, and isochronous data transfers
    - CRC16 generation and checking
    - NRZI encoding/decoding with bit stuffing
    - Supports both 12- and 1.5-Mbps data rates (automatic generation of preamble token and data rate configuration). Note that low-speed operation requires an external hub.
    - Flexible data buffers with multiple buffers per frame
    - Supports local loopback mode for diagnostics (12 Mbps only)
- Serial peripheral interface (SPI)
  - Supports master and slave modes
  - Supports multiple-master operation on the same bus
- Inter-integrated circuit (I^2C) port
  - Supports master and slave modes
  - Supports a multiple-master environment

3 Maximum Tolerated Ratings

This section provides the maximum tolerated voltage and temperature ranges for the MPC875/MPC870. Table 2 displays the maximum tolerated ratings and Table 3 displays the operating temperatures.

Table 2. Maximum Tolerated Ratings

Rating	Symbol	Value	Unit
Supply voltage[1]	V_{DDL} (core voltage)	–0.3 to 3.4	V
	V_{DDH} (I/O voltage)	–0.3 to 4	V
	V_{DDSYN}	–0.3 to 3.4	V
	Difference between V_{DDL} and V_{DDSYN}	<100	mV
Input voltage[2]	V_{in}	GND – 0.3 to V_{DDH}	V
Storage temperature range	T_{stg}	–55 to +150	°C

1 The power supply of the device must start its ramp from 0.0 V.

2 Functional operating conditions are provided with the DC electrical specifications in Table 6. Absolute maximum ratings are stress ratings only; functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.
Caution: All inputs that tolerate 5 V cannot be more than 2.5 V greater than V_{DDH}. This restriction applies to power up and normal operation (that is, if the MPC875/MPC870 is unpowered, a voltage greater than 2.5 V must not be applied to its inputs).

Figure 3 shows the undershoot and overshoot voltages at the interfaces of the MPC875/MPC870.

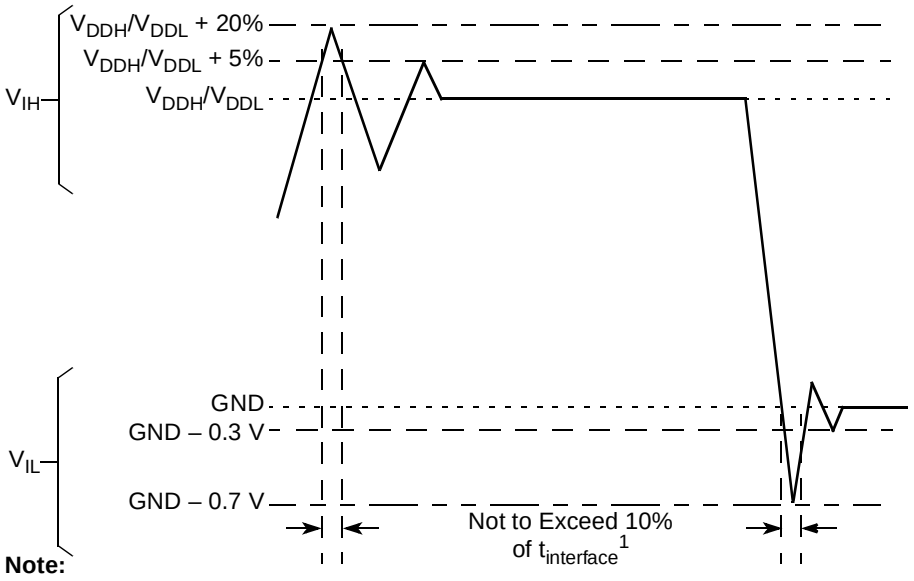

Figure 3. Undershoot/Overshoot Voltage for V_{DDH} and V_{DDL}

Table 10. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B33a	CLKOUT rising edge to $\overline{\text{GPL}}$ valid as requested by control bit GxT3 in the corresponding word in the UPM (MAX = 0.25 × B1 + 6.80)	7.60	14.30	6.30	13.00	3.80	10.50	3.13	10.00	ns
B34	A(0:31), BADDR(28:30), and D(0:31) to $\overline{\text{CS}}$ valid, as requested by control bit CST4 in the corresponding word in the UPM (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	1.80	—	1.13	—	ns
B34a	A(0:31), BADDR(28:30), and D(0:31) to $\overline{\text{CS}}$ valid, as requested by control bit CST1 in the corresponding word in the UPM (MIN = 0.50 × B1 – 2.00)	13.20	—	10.50	—	5.60	—	4.25	—	ns
B34b	A(0:31), BADDR(28:30), and D(0:31) to $\overline{\text{CS}}$ valid, as requested by CST2 in the corresponding word in UPM (MIN = 0.75 × B1 – 2.00)	20.70	—	16.70	—	9.40	—	6.80	—	ns
B35	A(0:31), BADDR(28:30) to $\overline{\text{CS}}$ valid as requested by control bit BST4 in the corresponding word in the UPM (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	1.80	—	1.13	—	ns
B35a	A(0:31), BADDR(28:30), and D(0:31) to $\overline{\text{BS}}$ valid as requested by BST1 in the corresponding word in the UPM (MIN = 0.50 × B1 – 2.00)	13.20	—	10.50	—	5.60	—	4.25	—	ns
B35b	A(0:31), BADDR(28:30), and D(0:31) to $\overline{\text{BS}}$ valid as requested by control bit BST2 in the corresponding word in the UPM (MIN = 0.75 × B1 – 2.00)	20.70	—	16.70	—	9.40	—	7.40	—	ns
B36	A(0:31), BADDR(28:30), and D(0:31) to $\overline{\text{GPL}}$ valid as requested by control bit GxT4 in the corresponding word in the UPM (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	1.80	—	1.13	—	ns
B37	UPWAIT valid to CLKOUT falling edge[9] (MIN = 0.00 × B1 + 6.00)	6.00	—	6.00	—	6.00	—	6.00	—	ns
B38	CLKOUT falling edge to UPWAIT valid[9] (MIN = 0.00 × B1 + 1.00)	1.00	—	1.00	—	1.00	—	1.00	—	ns
B39	$\overline{\text{AS}}$ valid to CLKOUT rising edge[10] (MIN = 0.00 × B1 + 7.00)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B40	A(0:31), TSIZ(0:1), RD/$\overline{\text{WR}}$, $\overline{\text{BURST}}$ valid to CLKOUT rising edge (MIN = 0.00 × B1 + 7.00)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B41	$\overline{\text{TS}}$ valid to CLKOUT rising edge (setup time) (MIN = 0.00 × B1 + 7.00)	7.00	—	7.00	—	7.00	—	7.00	—	ns

Figure 9 provides the timing for the synchronous input signals.

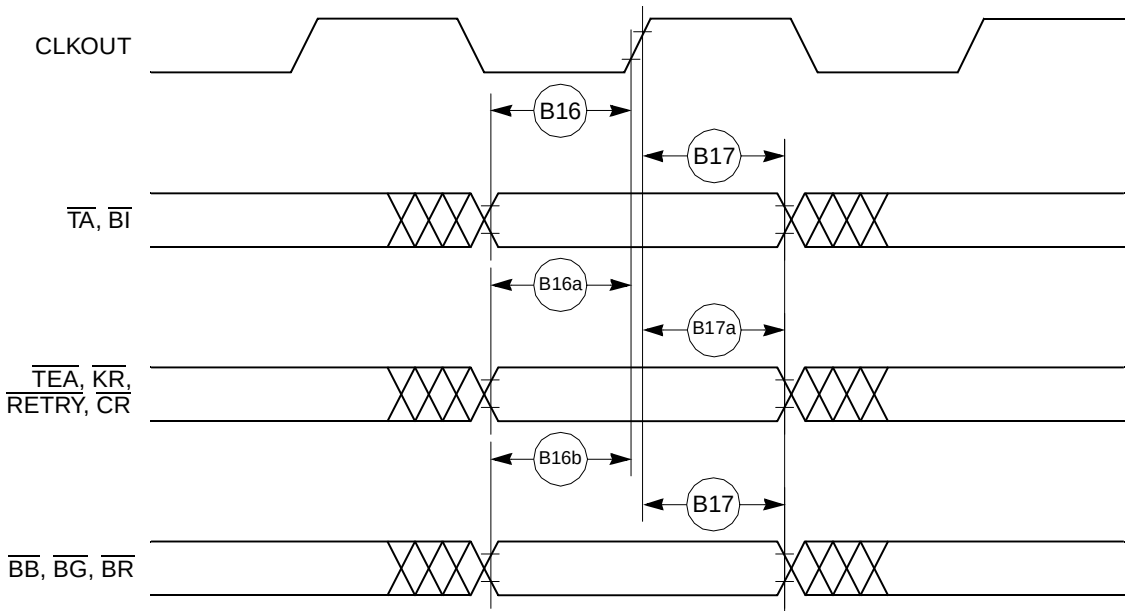

Figure 9. Synchronous Input Signals Timing

Figure 10 provides normal case timing for input data. It also applies to normal read accesses under the control of the user-programmable machine (UPM) in the memory controller.

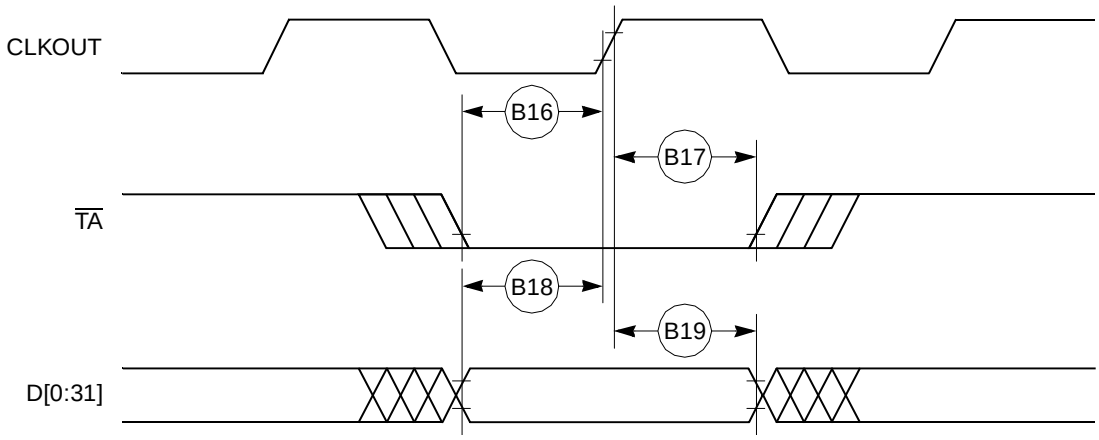

Figure 10. Input Data Timing in Normal Case

Figure 19 provides the timing for the external bus controlled by the UPM.

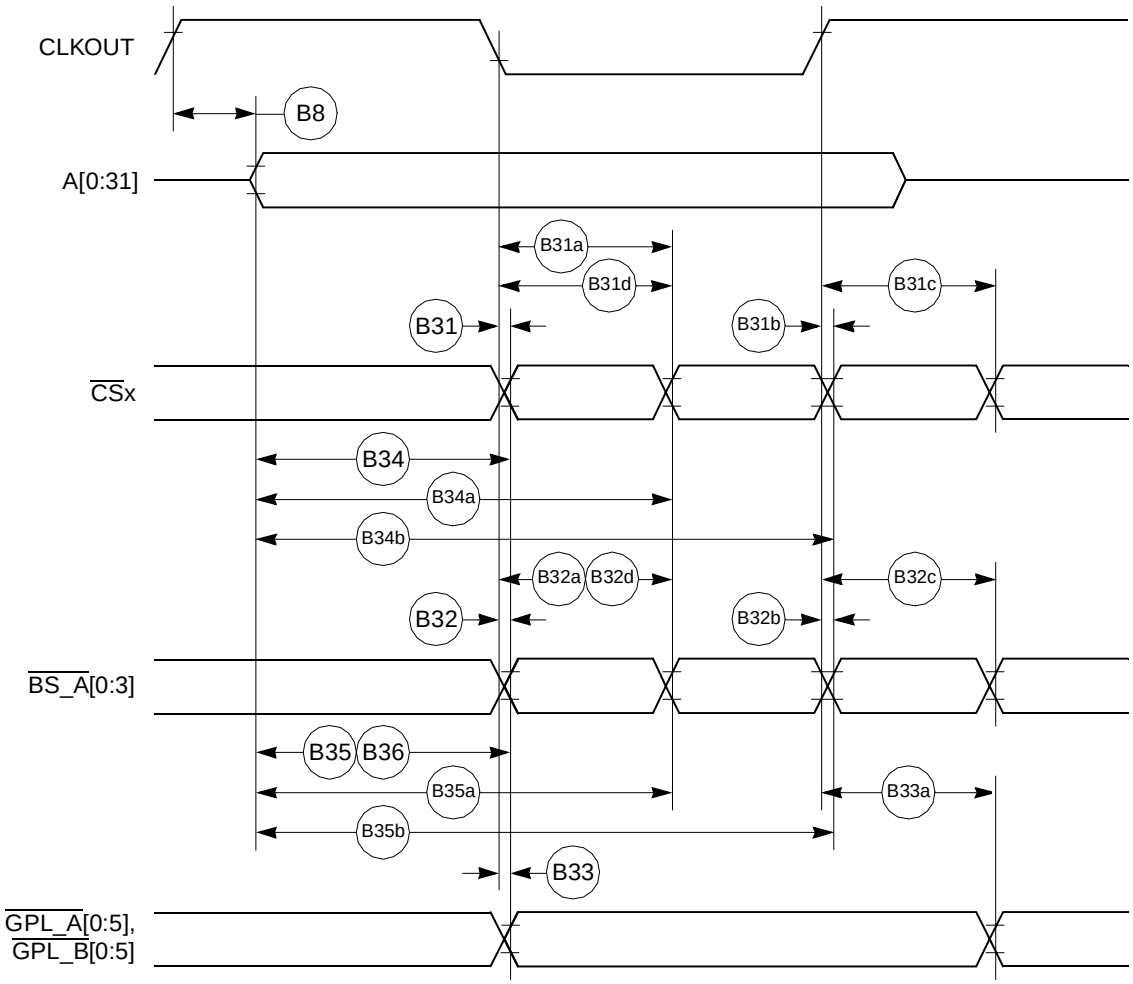

Figure 19. External Bus Timing (UPM Controlled Signals)

Table 15 shows the reset timing for the MPC875/MPC870.

Table 15. Reset Timing

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
R69	CLKOUT to $\overline{\text{HRESET}}$ high impedance (MAX = 0.00 × B1 + 20.00)	—	20.00	—	20.00	—	20.00	—	20.00	ns
R70	CLKOUT to $\overline{\text{SRESET}}$ high impedance (MAX = 0.00 × B1 + 20.00)	—	20.00	—	20.00	—	20.00	—	20.00	ns
R71	$\overline{\text{RSTCONF}}$ pulse width (MIN = 17.00 × B1)	515.20	—	425.00	—	257.60	—	212.50	—	ns
R72	—	—	—	—	—	—	—	—	—	—
R73	Configuration data to $\overline{\text{HRESET}}$ rising edge setup time (MIN = 15.00 × B1 + 50.00)	504.50	—	425.00	—	277.30	—	237.50	—	ns
R74	Configuration data to $\overline{\text{RSTCONF}}$ rising edge setup time (MIN = 0.00 × B1 + 350.00)	350.00	—	350.00	—	350.00	—	350.00	—	ns
R75	Configuration data hold time after $\overline{\text{RSTCONF}}$ negation (MIN = 0.00 × B1 + 0.00)	0.00	—	0.00	—	0.00	—	0.00	—	ns
R76	Configuration data hold time after $\overline{\text{HRESET}}$ negation (MIN = 0.00 × B1 + 0.00)	0.00	—	0.00	—	0.00	—	0.00	—	ns
R77	$\overline{\text{HRESET}}$ and $\overline{\text{RSTCONF}}$ asserted to data out drive (MAX = 0.00 × B1 + 25.00)	—	25.00	—	25.00	—	25.00	—	25.00	ns
R78	$\overline{\text{RSTCONF}}$ negated to data out high impedance (MAX = 0.00 × B1 + 25.00)	—	25.00	—	25.00	—	25.00	—	25.00	ns
R79	CLKOUT of last rising edge before chip three-states $\overline{\text{HRESET}}$ to data out high impedance (MAX = 0.00 × B1 + 25.00)	—	25.00	—	25.00	—	25.00	—	25.00	ns
R80	DSDI, DSCK setup (MIN = 3.00 × B1)	90.90	—	75.00	—	45.50	—	37.50	—	ns
R81	DSDI, DSCK hold time (MIN = 0.00 × B1 + 0.00)	0.00	—	0.00	—	0.00	—	0.00	—	ns
R82	$\overline{\text{SRESET}}$ negated to CLKOUT rising edge for DSDI and DSCK sample (MIN = 8.00 × B1)	242.40	—	200.00	—	121.20	—	100.00	—	ns

Figure 34 shows the reset timing for the data bus configuration.

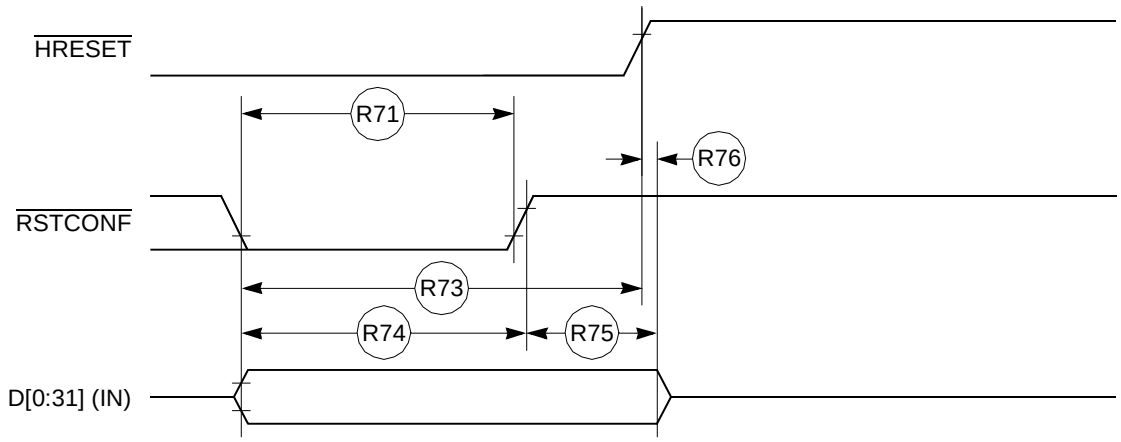

Figure 34. Reset Timing—Configuration from Data Bus

Figure 35 provides the reset timing for the data bus weak drive during configuration.

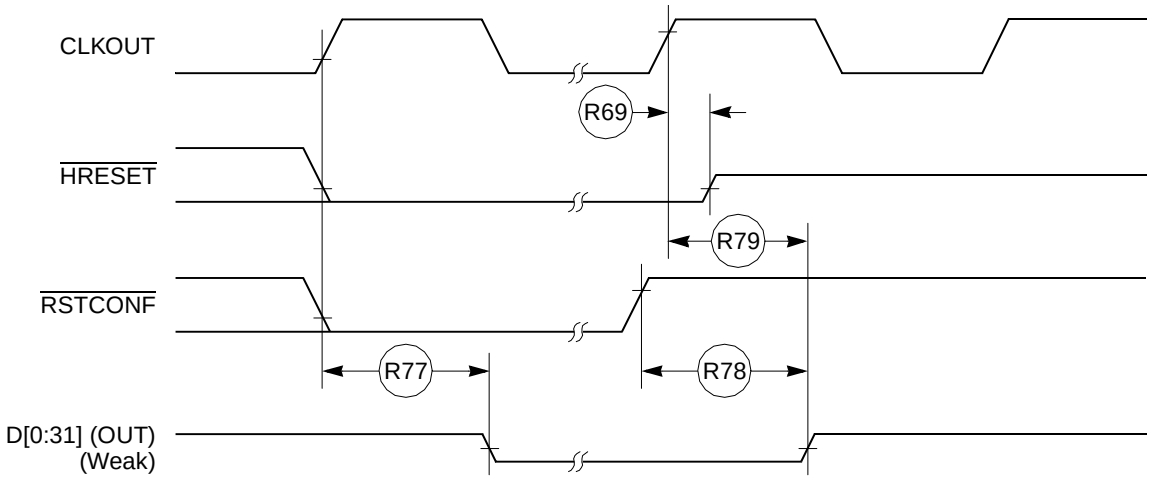

Figure 35. Reset Timing—Data Bus Weak Drive During Configuration

Figure 36 provides the reset timing for the debug port configuration.

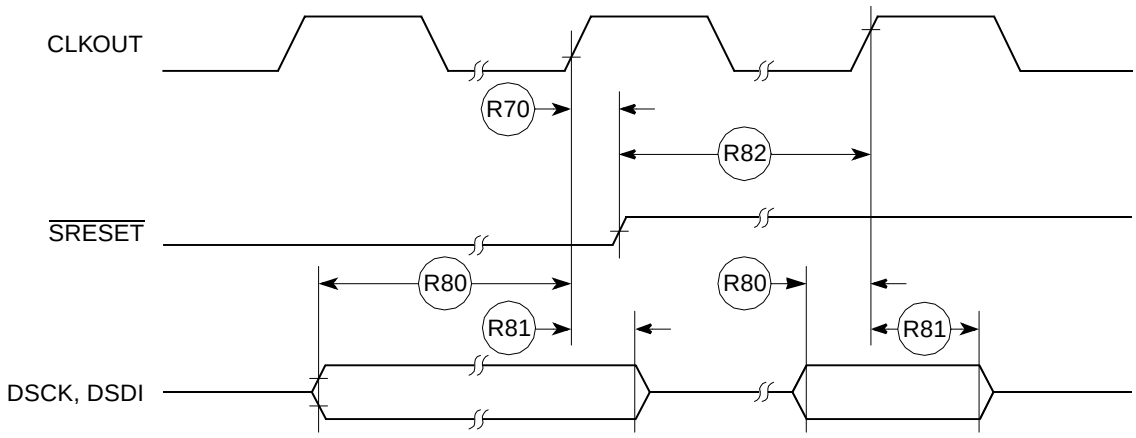

Figure 36. Reset Timing—Debug Port Configuration

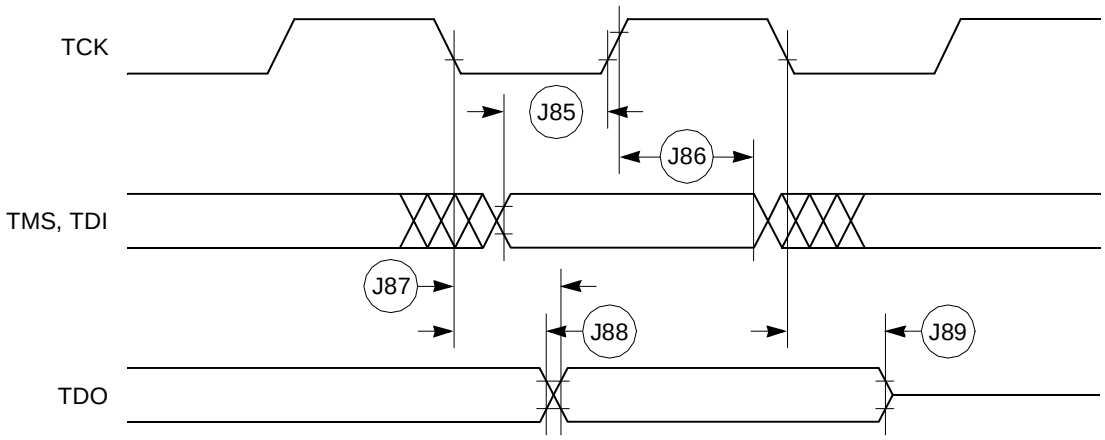

Figure 38. JTAG Test Access Port Timing Diagram

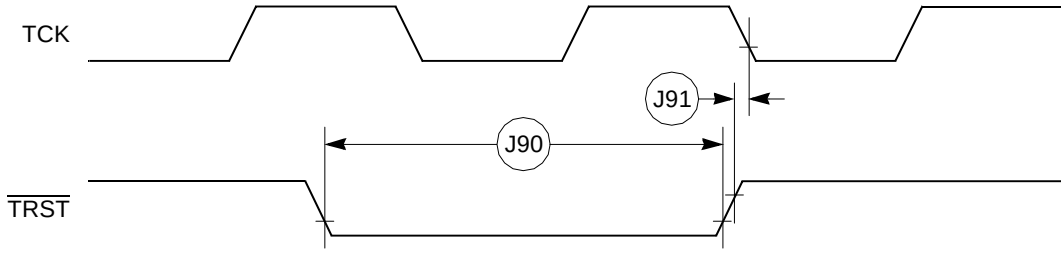

Figure 39. JTAG $\overline{\text{TRST}}$ Timing Diagram

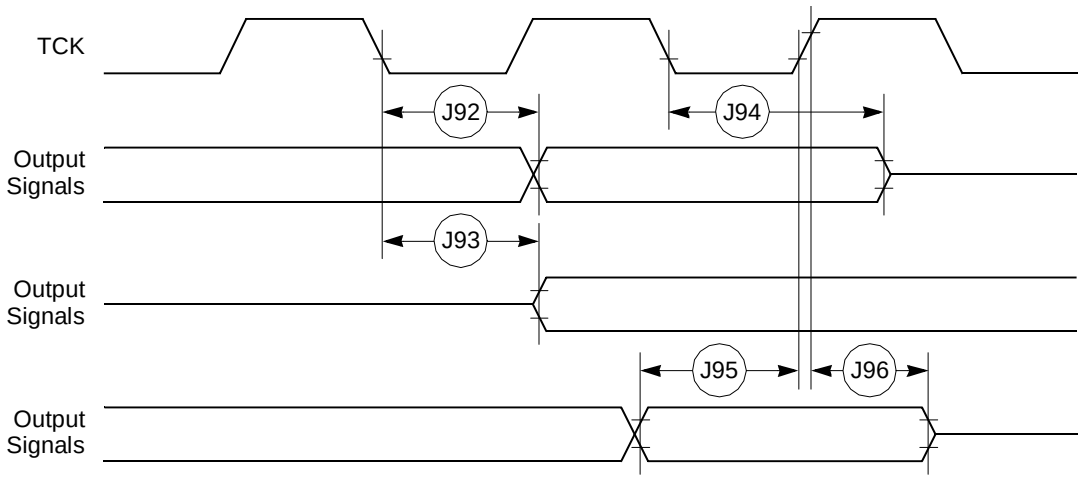

Figure 40. Boundary Scan (JTAG) Timing Diagram

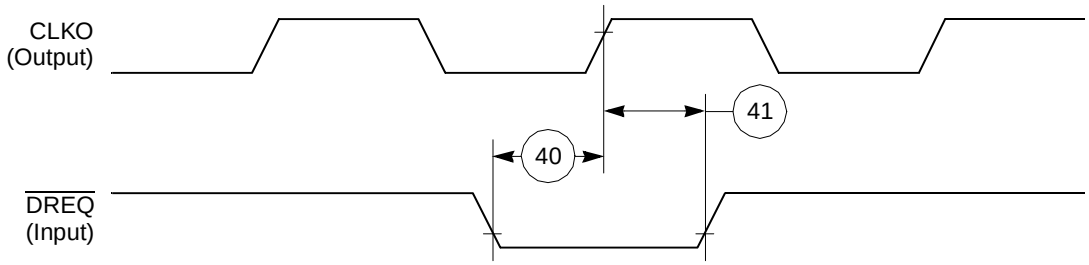

Figure 42. IDMA External Requests Timing Diagram

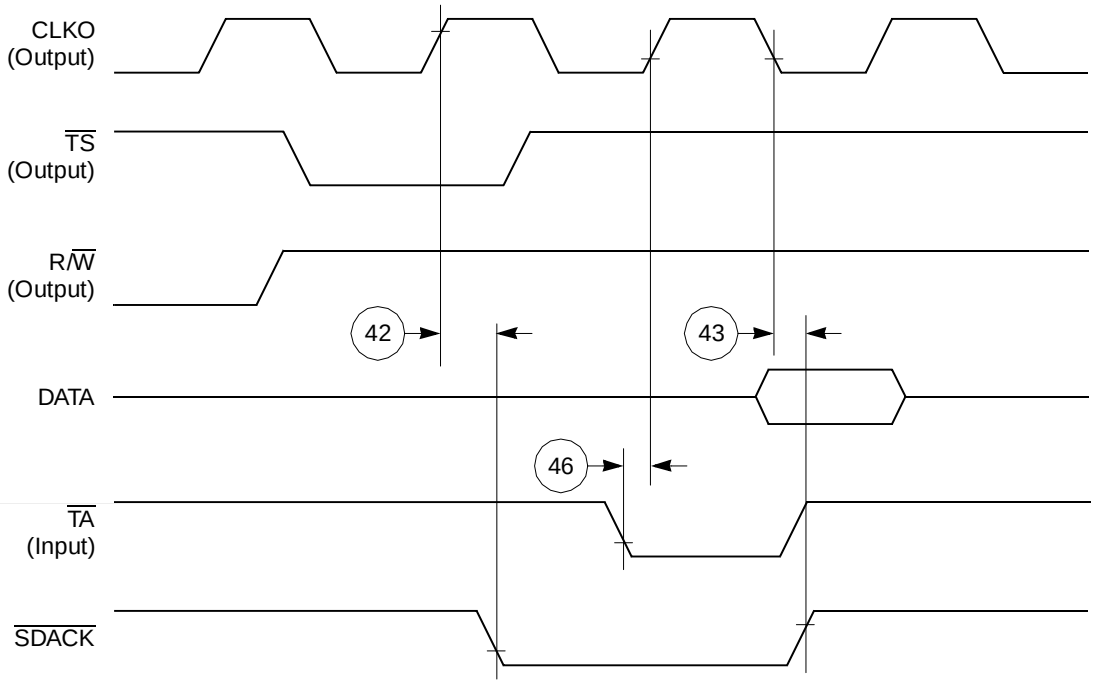

Figure 43. SDACK Timing Diagram—Peripheral Write, Externally-Generated TA

13.3 Baud Rate Generator AC Electrical Specifications

Table 19 provides the baud rate generator timings as shown in Figure 46.

Table 19. Baud Rate Generator Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
50	BRGO rise and fall time	—	10	ns
51	BRGO duty cycle	40	60	%
52	BRGO cycle	40	—	ns

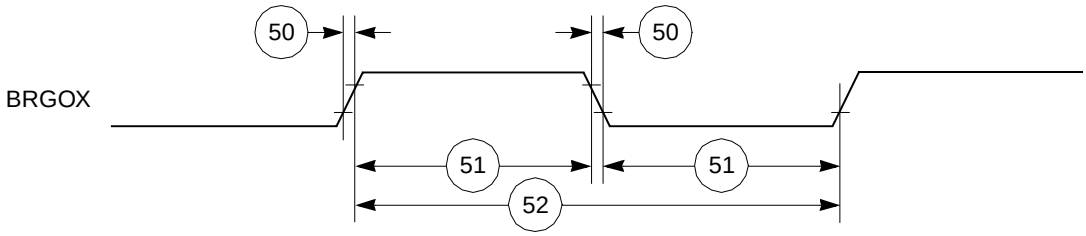

Figure 46. Baud Rate Generator Timing Diagram

13.4 Timer AC Electrical Specifications

Table 20 provides the general-purpose timer timings as shown in Figure 47.

Table 20. Timer Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
61	TIN/$\overline{\text{TGATE}}$ rise and fall time	10	—	ns
62	TIN/$\overline{\text{TGATE}}$ low time	1	—	clk
63	TIN/$\overline{\text{TGATE}}$ high time	2	—	clk
64	TIN/$\overline{\text{TGATE}}$ cycle time	3	—	clk
65	CLKO low to $\overline{\text{TOUT}}$ valid	3	25	ns

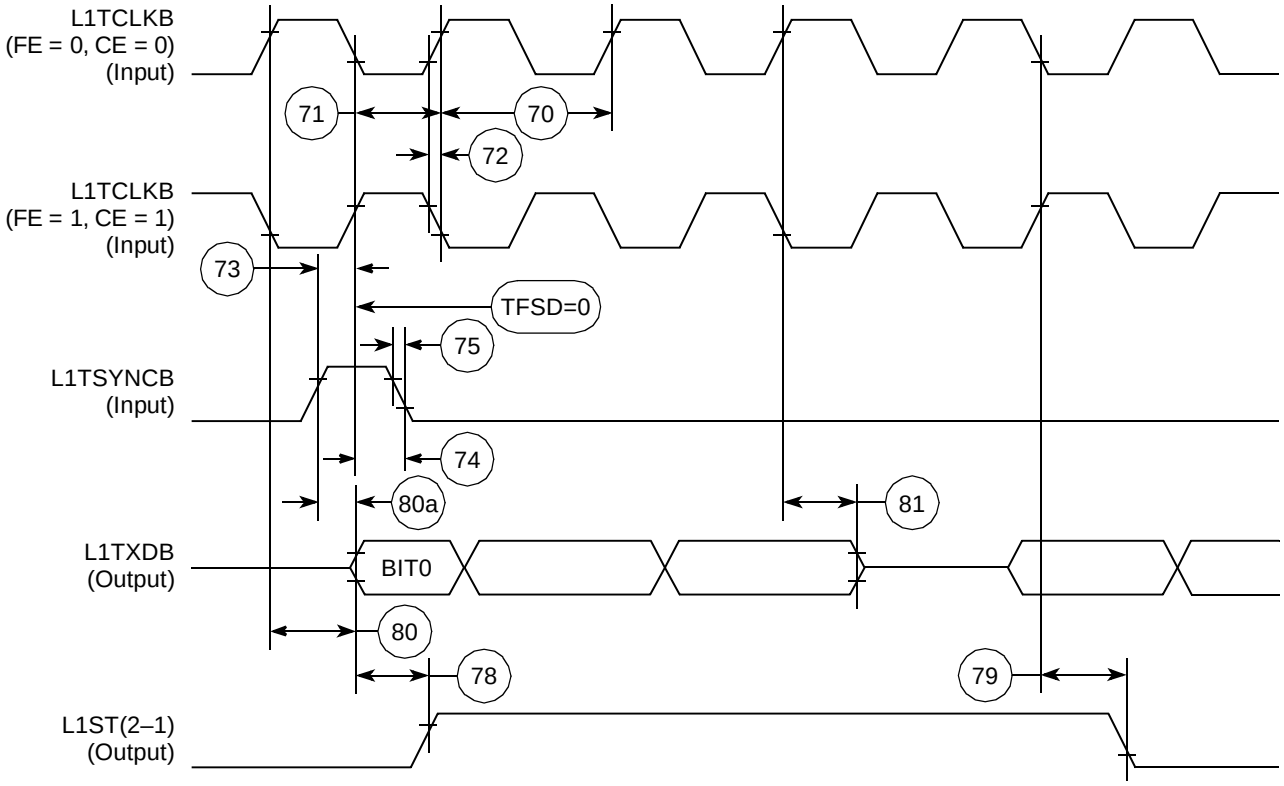

Figure 50. SI Transmit Timing Diagram (DSC = 0)

13.6 SCC in NMSI Mode Electrical Specifications

Table 22 provides the NMSI external clock timing.

Table 22. NMSI External Clock Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
100	RCLK3 and TCLK3 width high[1]	1/SYNCCLK	—	ns
101	RCLK3 and TCLK3 width low	1/SYNCCLK + 5	—	ns
102	RCLK3 and TCLK3 rise/fall time	—	15.00	ns
103	TXD3 active delay (from TCLK3 falling edge)	0.00	50.00	ns
104	$\overline{\text{RTS3}}$ active/inactive delay (from TCLK3 falling edge)	0.00	50.00	ns
105	$\overline{\text{CTS3}}$ setup time to TCLK3 rising edge	5.00	—	ns
106	RXD3 setup time to RCLK3 rising edge	5.00	—	ns
107	RXD3 hold time from RCLK3 rising edge[2]	5.00	—	ns
108	$\overline{\text{CD3}}$ setup time to RCLK3 rising edge	5.00	—	ns

1 The ratios SYNCCLK/RCLK3 and SYNCCLK/TCLK3 must be greater than or equal to 2.25/1.
2 Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as external SYNC signals.

Table 23 provides the NMSI internal clock timing.

Table 23. NMSI Internal Clock Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
100	RCLK3 and TCLK3 frequency[1]	0.00	SYNCCLK/3	MHz
102	RCLK3 and TCLK3 rise/fall time	—	—	ns
103	TXD3 active delay (from TCLK3 falling edge)	0.00	30.00	ns
104	$\overline{\text{RTS3}}$ active/inactive delay (from TCLK3 falling edge)	0.00	30.00	ns
105	$\overline{\text{CTS3}}$ setup time to TCLK3 rising edge	40.00	—	ns
106	RXD3 setup time to RCLK3 rising edge	40.00	—	ns
107	RXD3 hold time from RCLK3 rising edge[2]	0.00	—	ns
108	$\overline{\text{CD3}}$ setup time to RCLK3 rising edge	40.00	—	ns

1 The ratios SYNCCLK/RCLK3 and SYNCCLK/TCLK3 must be greater or equal to 3/1.
2 Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as external SYNC signals.

Figure 53 through Figure 55 show the NMSI timings.

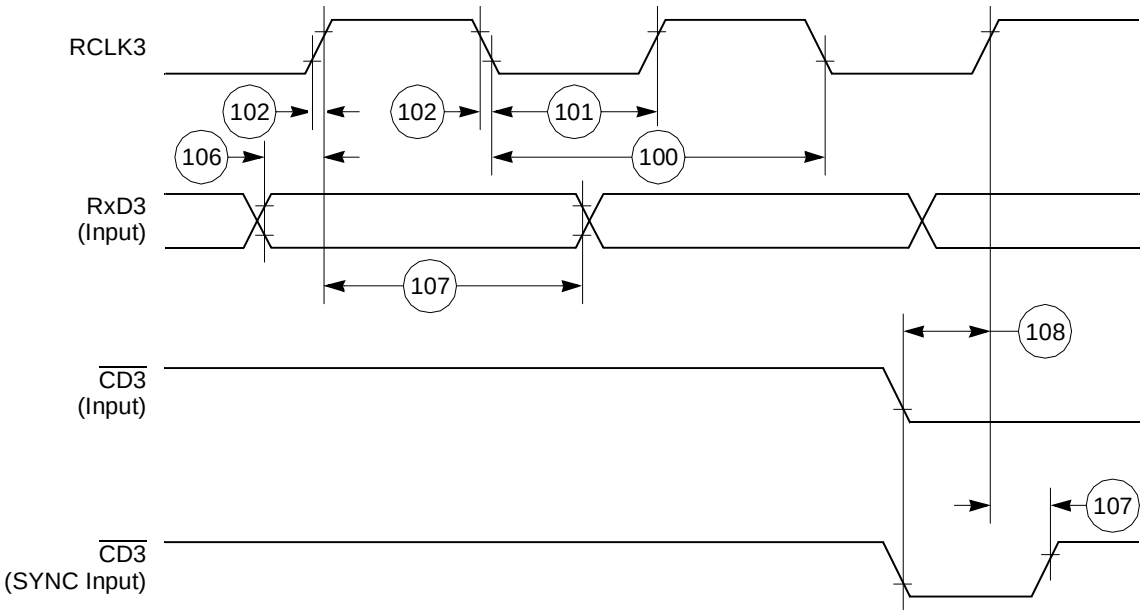

Figure 53. SCC NMSI Receive Timing Diagram

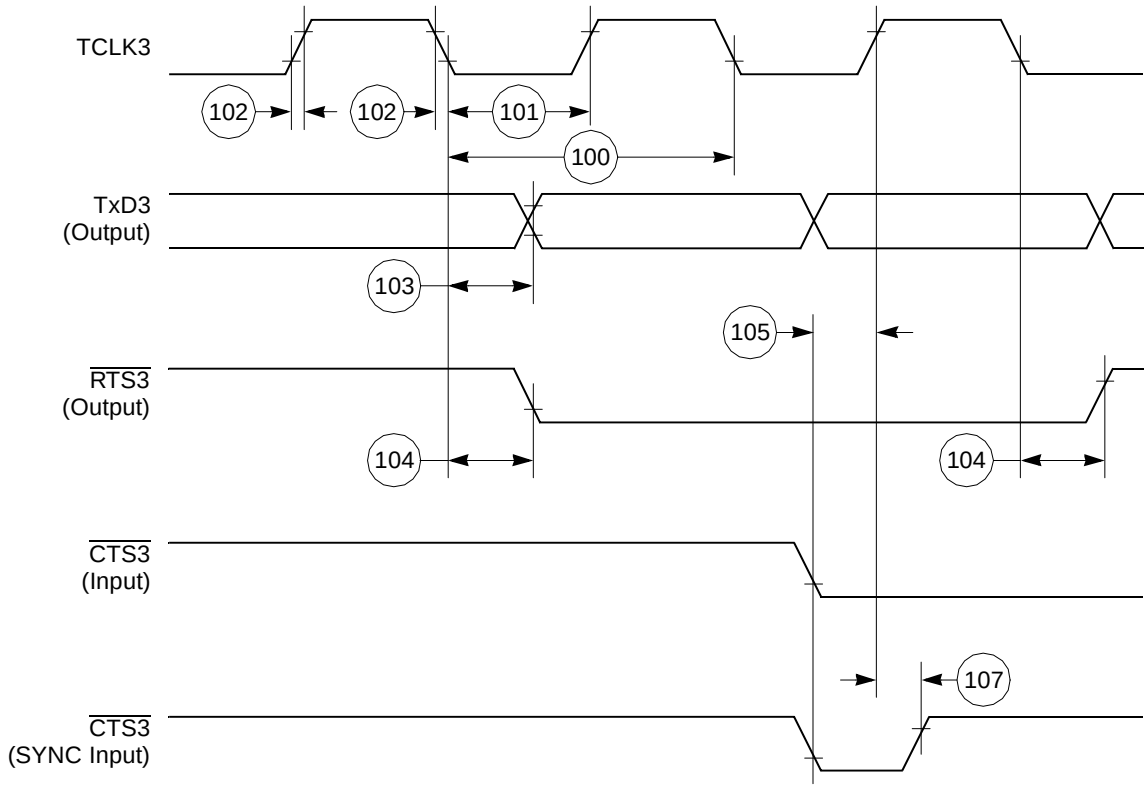

Figure 54. SCC NMSI Transmit Timing Diagram

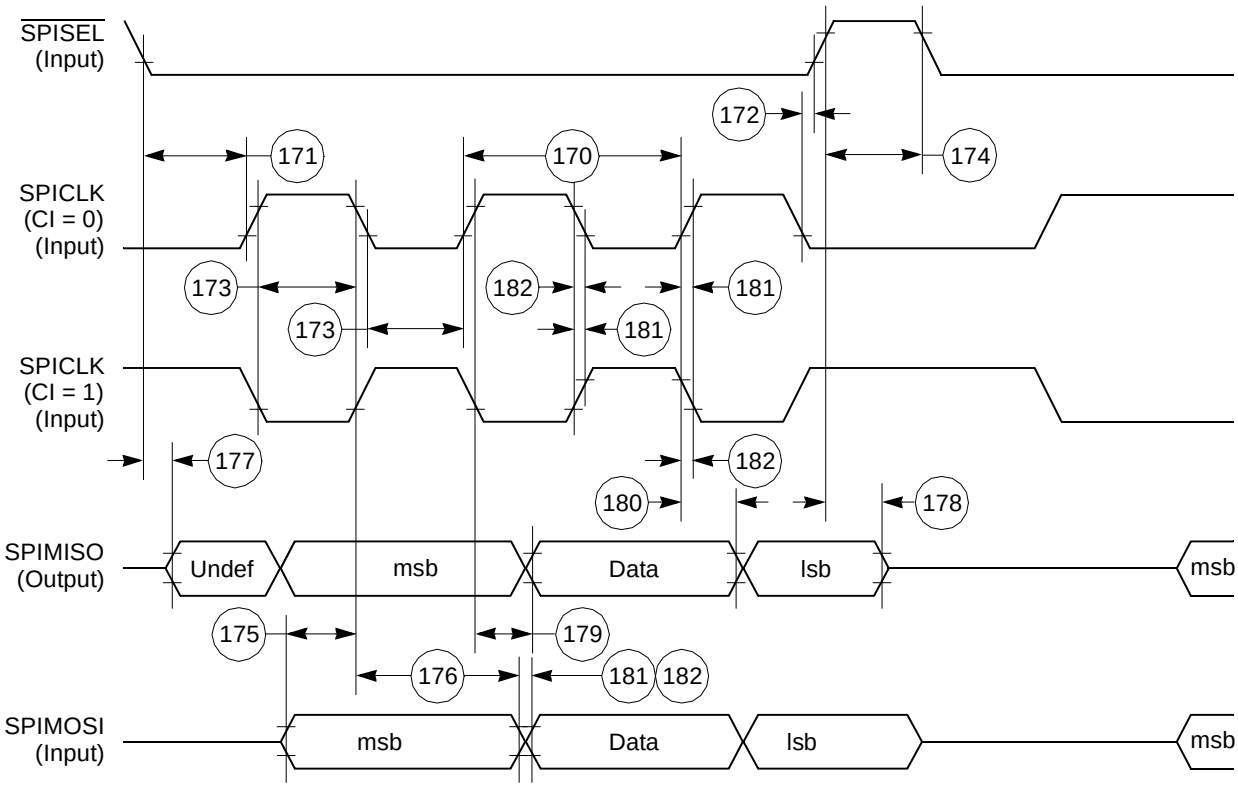

Figure 63. SPI Slave (CP = 1) Timing Diagram

13.11 I²C AC Electrical Specifications

Table 28 provides the I²C (SCL < 100 kHz) timings.

Table 28. I²C Timing (SCL < 100 kHz)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
200	SCL clock frequency (slave)	0	100	kHz
200	SCL clock frequency (master)[1]	1.5	100	kHz
202	Bus free time between transmissions	4.7	—	µs
203	Low period of SCL	4.7	—	µs
204	High period of SCL	4.0	—	µs
205	Start condition setup time	4.7	—	µs
206	Start condition hold time	4.0	—	µs
207	Data hold time	0	—	µs
208	Data setup time	250	—	ns
209	SDL/SCL rise time	—	1	µs

Table 28. I²C Timing (SCL < 100 kHz) (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
210	SDL/SCL fall time	—	300	ns
211	Stop condition setup time	4.7	—	µs

1 SCL frequency is given by SCL = BRGCLK_frequency/((BRG register + 3) × pre_scalar × 2).
The ratio SYNCCLK/(BRGCLK/pre_scalar) must be greater than or equal to 4/1.

Table 29 provides the I²C (SCL > 100 kHz) timings.

Table 29. I²C Timing (SCL > 100 kHz)

Num	Characteristic	Expression	All Frequencies		Unit
			Min	Max	
200	SCL clock frequency (slave)	fSCL	0	BRGCLK/48	Hz
200	SCL clock frequency (master)[1]	fSCL	BRGCLK/16512	BRGCLK/48	Hz
202	Bus free time between transmissions	—	1/(2.2 × fSCL)	—	s
203	Low period of SCL	—	1/(2.2 × fSCL)	—	s
204	High period of SCL	—	1/(2.2 × fSCL)	—	s
205	Start condition setup time	—	1/(2.2 × fSCL)	—	s
206	Start condition hold time	—	1/(2.2 × fSCL)	—	s
207	Data hold time	—	0	—	s
208	Data setup time	—	1/(40 × fSCL)	—	s
209	SDL/SCL rise time	—	—	1/(10 × fSCL)	s
210	SDL/SCL fall time	—	—	1/(33 × fSCL)	s
211	Stop condition setup time	—	1/2(2.2 × fSCL)	—	s

1 SCL frequency is given by SCL = BRGCLK_frequency/((BRG register + 3) × pre_scalar × 2).
The ratio SYNCCLK/(BRGCLK/pre_scalar) must be greater than or equal to 4/1.

Figure 64 shows the I²C bus timing.

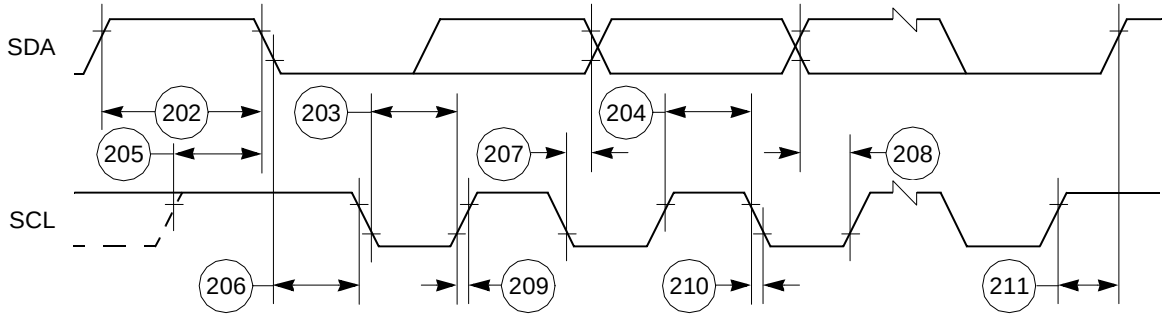

Figure 64. I²C Bus Timing Diagram

14 USB Electrical Characteristics

This section provides the AC timings for the USB interface.

14.1 USB Interface AC Timing Specifications

The USB Port uses the transmit clock on SCC1. Table 30 lists the USB interface timings.

Table 30. USB Interface AC Timing Specifications

Name	Characteristic	All Frequencies		Unit
		Min	Max	
US1	USBCLK frequency of operation[1] Low speed Full speed	 6 48		MHz
US4	USBCLK duty cycle (measured at 1.5 V)	45	55	%

1 USBCLK accuracy should be ±500 ppm or better. USBCLK may be stopped to conserve power.

15 FEC Electrical Characteristics

This section provides the AC electrical specifications for the Fast Ethernet controller (FEC). Note that the timing specifications for the MII signals are independent of system clock frequency (part speed designation). Also, MII signals use TTL signal levels compatible with devices operating at either 5.0 or 3.3 V.

15.1 MII and Reduced MII Receive Signal Timing

The receiver functions correctly up to a MII_RX_CLK maximum frequency of 25 MHz + 1%. The reduced MII (RMII) receiver functions correctly up to a RMII_REFCLK maximum frequency of 50 MHz + 1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_RX_CLK frequency – 1%.

Table 31 provides information on the MII receive signal timing.

Table 31. MII Receive Signal Timing

Num	Characteristic	Min	Max	Unit
M1	MII_RXD[3:0], MII_RX_DV, MII_RX_ER to MII_RX_CLK setup	5	—	ns
M2	MII_RX_CLK to MII_RXD[3:0], MII_RX_DV, MII_RX_ER hold	5	—	ns
M3	MII_RX_CLK pulse width high	35%	65%	MII_RX_CLK period
M4	MII_RX_CLK pulse width low	35%	65%	MII_RX_CLK period
M1_RMII	RMII_RXD[1:0], RMII_CRS_DV, RMII_RX_ERR to RMII_REFCLK setup	4	—	ns
M2_RMII	RMII_REFCLK to RMII_RXD[1:0], RMII_CRS_DV, RMII_RX_ERR hold	2	—	ns

Figure 68 shows the MII serial management channel timing diagram.

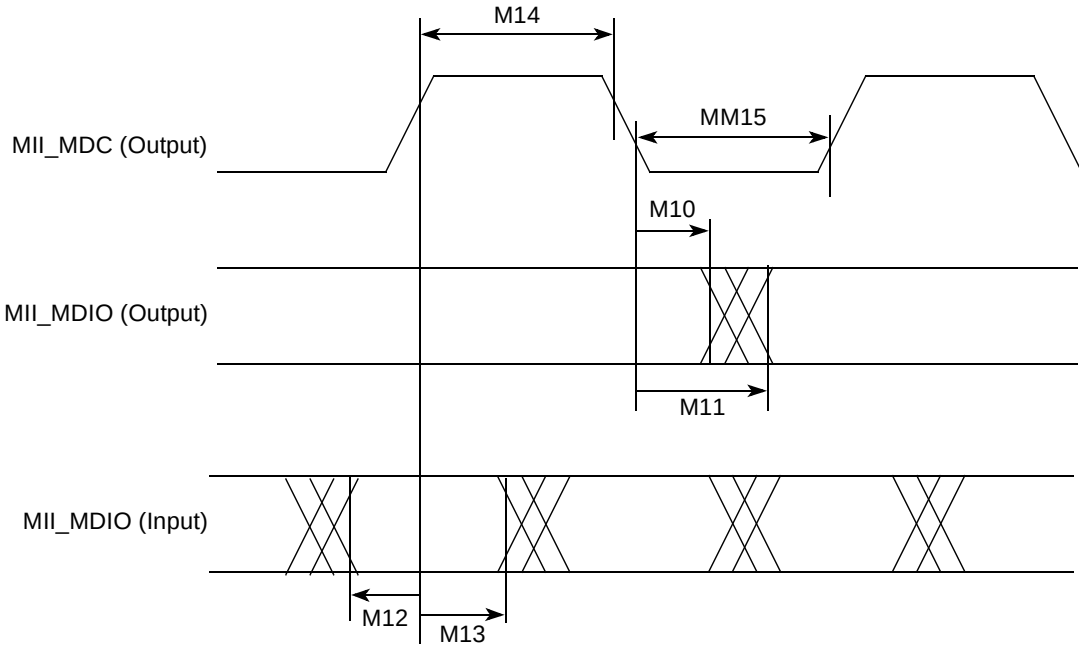

Figure 68. MII Serial Management Channel Timing Diagram

16 Mechanical Data and Ordering Information

Table 35 identifies the packages and operating frequencies available for the MPC875/MPC870.

Table 35. Available MPC875/MPC870 Packages/Frequencies

Package Type	Temperature (T_J)	Frequency (MHz)	Order Number
Plastic ball grid array ZT suffix—Leaded VR suffix—Lead-Free are available as needed	0°C to 95°C	66	KMPC875ZT66 KMPC870ZT66 MPC875ZT66 MPC870ZT66
		80	KMPC875ZT80 KMPC870ZT80 MPC875ZT80 MPC870ZT80
		133	KMPC875ZT133 KMPC870ZT133 MPC875ZT133 MPC870ZT133
Plastic ball grid array CZT suffix—Leaded CVR suffix—Lead-Free are available as needed	-40°C to 100°C	66	KMPC875CZT66 KMPC870CZT66 MPC875CZT66 MPC870CZT66
		133	KMPC875CZT133 KMPC870CZT133 MPC875CZT133 MPC870CZT133

Table 36. Pin Assignments—JEDEC Standard (continued)

Name	Pin Number	Type
IP_A6	F4	Input (3.3 V only)
IP_A7	C2	Input (3.3 V only)
ALE_B, DSCK	C8	Bidirectional Three-state (3.3 V only)
IP_B[0:1], IWP[0:1], VFLS[0:1]	B8, D9	Bidirectional (3.3 V only)
OP0	B6	Bidirectional (3.3 V only)
OP1	C6	Output
OP2, MODCK1, $\overline{\text{STS}}$	B5	Bidirectional (3.3 V only)
OP3, MODCK2, DSDO	B2	Bidirectional (3.3 V only)
BADDR[28:29]	E8, C5	Output
BADDR30, $\overline{\text{REG}}$	D8	Output
$\overline{\text{AS}}$	C7	Input (3.3 V only)
PA15, USBRXD	P14	Bidirectional
PA14, USBOE	U16	Bidirectional (Optional: open-drain)
PA11, RXD4, MII1-TXD0, RMII1-TXD0	R9	Bidirectional (Optional: open-drain) (5-V tolerant)
PA10, MII1-TXERR, TIN4, CLK7	R12	Bidirectional (Optional: open-drain) (5-V tolerant)
PA7, CLK1, BRGO1, TIN1	R11	Bidirectional
PA6, CLK2, $\overline{\text{TOUT1}}$	P11	Bidirectional
PA4, $\overline{\text{CTS4}}$, MII1-TXD1, RMII-TXD1	P7	Bidirectional
PA3, MII1-RXER, RMII1-RXER, BRGO3	R5	Bidirectional (5-V tolerant)
PA2, MII1-RXDV, RMII1-CRS_DV, TXD4	N6	Bidirectional (5-V tolerant)
PA1, MII1-RXD0, RMII1-RXD0, BRGO4	T4	Bidirectional (5-V tolerant)
PA0, MII1-RXD1, RMII1-RXD1, TOUT4	P6	Bidirectional (5-V tolerant)
PB31, $\overline{\text{SPISEL}}$, MII1-TXCLK, RMII1-REFCLK	T5	Bidirectional (Optional: open-drain) (5-V tolerant)

17 Document Revision History

Table 37 lists significant changes between revisions of this hardware specification.

Table 37. Document Revision History

Revision Number	Date	Changes
0	2/2003	Initial release.
0.1	3/2003	Took out the time-slot assigner and changed the SCC for SCC3 to SCC4.
0.2	5/2003	Changed the package drawing, removed all references to Data Parity. Changed the SPI Master Timing Specs. 162 and 164. Added the RMII and USB timing. Added the 80-MHz timing.
0.3	5/2003	Made sure the pin types were correct. Changed the Features list to agree with the MPC885.
0.4	5/2003	Corrected the signals that had overlines on them. Made corrections on two pins that were typos.
0.5	5/2003	Changed the pin descriptions for PD8 and PD9.
0.6	5/2003	Changed a few typos. Put back the I^2C. Put in the new reset configuration, corrected the USB timing.
0.7	6/2003	Changed the pin descriptions per the June 22 spec, removed Utopia from the pin descriptions, changed PADIR, PBDIR, PCDIR and PDDIR to be 0 in the Mandatory Reset Config.
0.8	8/2003	Added the reference to USB 2.0 to the Features list and removed 1.1 from USB on the block diagrams.
0.9	8/2003	Changed the USB description to full-/low-speed compatible.
1.0	9/2003	Added the DSP information in the Features list. Put a new sentence under Mechanical Dimensions. Fixed table formatting. Nontechnical edits. Released to the external web.
1.1	10/2003	Added TDMb to the MPC875 Features list, the MPC875 Block Diagram, added 13.5 Serial Interface AC Electrical Specifications, and removed TDMa from the pin descriptions.
2.0	12/2003	Changed DBGC in the Mandatory Reset Configuration to X1. Changed the maximum operating frequency to 133 MHz. Put the timing in the 80 MHz column. Put in the orderable part numbers. Rounded the timings to hundredths in the 80 MHz column. Put the pin numbers in footnotes by the maximum currents in Table 6. Changed 22 and 41 in the Timing. Put TBD in the Thermal table.