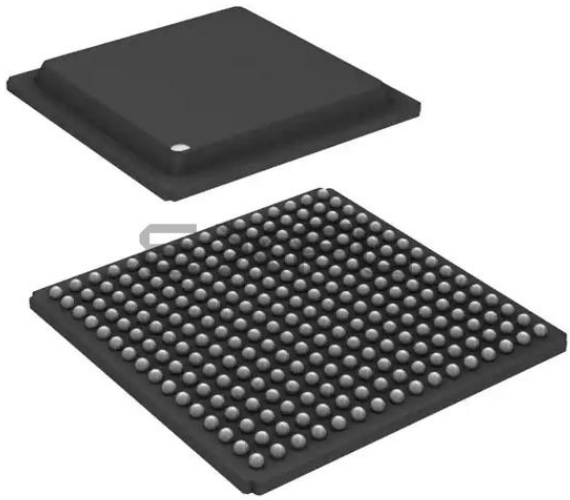

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	66MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (2)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 100°C (TA)
Security Features	-
Package / Case	256-BBGA
Supplier Device Package	256-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc870cvr66

The MPC875 block diagram is shown in Figure 1.

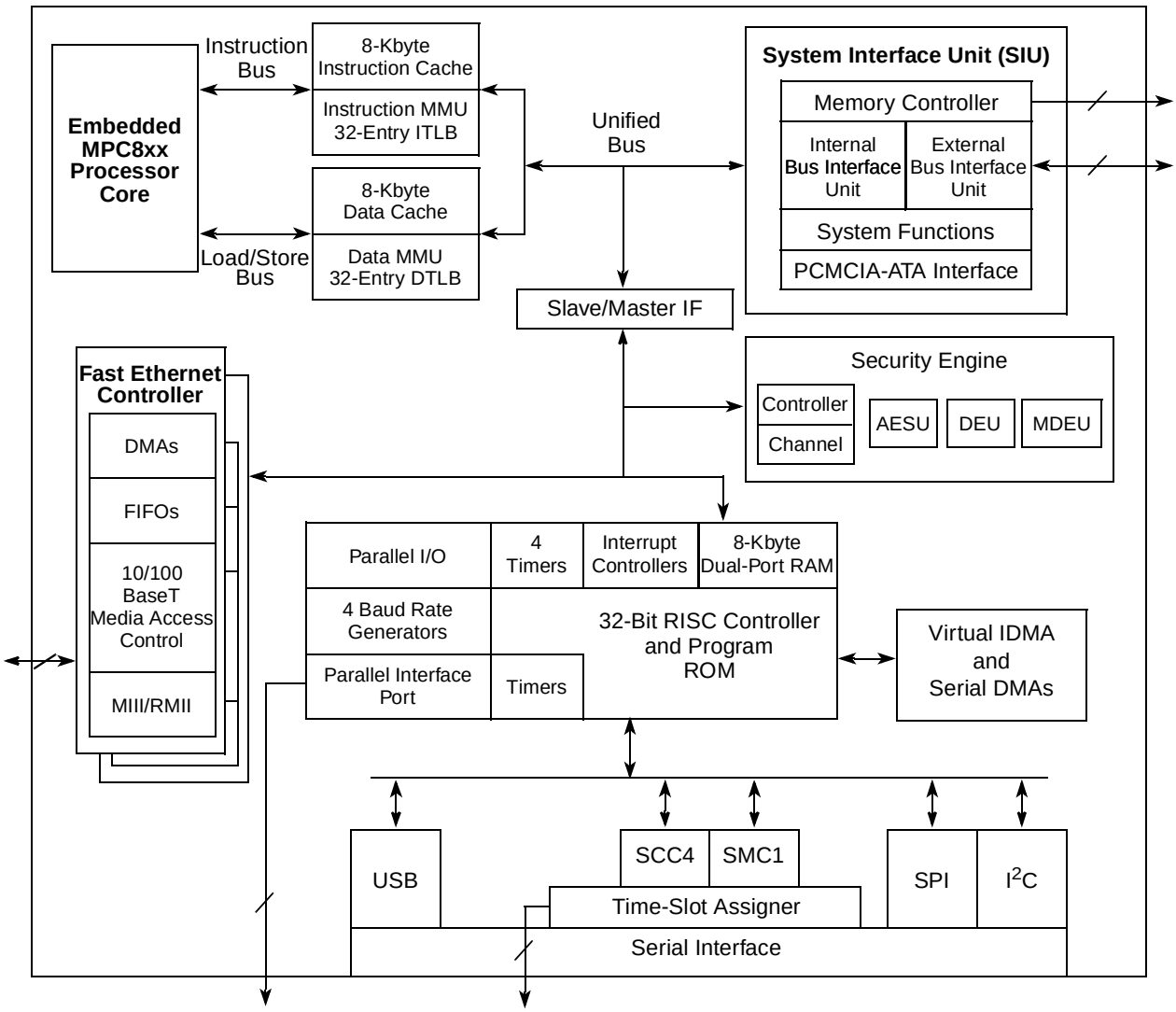

Figure 1. MPC875 Block Diagram

Table 7. Mandatory Reset Configuration of MPC875/MPC870 (continued)

Register/Configuration	Field	Value (Binary)
PADIR (Port A data direction register)	PADIR[5:9] PADIR[12:13]	0
PBPAR (Port B pin assignment register)	PBPAR[14:18] PBPAR[20:22]	0
PBDIR (Port B data direction register)	PBDIR[14:8] PBDIR[20:22]	0
PCPAR (Port C pin assignment register)	PCPAR[4:5] PCPAR[8:9] PCPAR[14]	0
PCDIR (Port C data direction register)	PCDIR[4:5] PCDIR[8:9] PCDIR[14]	0
PDPAR (Port D pin assignment register)	PDPAR[3:7] PDPAR[9:5]	0
PDDIR (Port D data direction register)	PDDIR[3:7] PDDIR[9:15]	0

10 Layout Practices

Each V_{DD} pin on the MPC875/MPC870 should be provided with a low-impedance path to the board's supply. Each GND pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The V_{DD} power supply should be bypassed to ground using at least four 0.1-µF bypass capacitors located as close as possible to the four sides of the package. Each board designed should be characterized and additional appropriate decoupling capacitors should be used if required. The capacitor leads and associated printed-circuit traces connecting to chip V_{DD} and GND should be kept to less than half an inch per capacitor lead. At a minimum, a four-layer board employing two inner layers as V_{DD} and GND planes should be used.

All output pins on the MPC875/MPC870 have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses. Maximum PC trace lengths of 6 inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the V_{DD} and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins. For more information, refer to Section 14.4.3, "Clock Synthesizer Power (V_{DDSYN}, V_{SSSYN}, V_{SSSYN1})," in the *MPC885 PowerQUICC™ Family Reference Manual*.

Table 10. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B2	CLKOUT pulse width low (MIN = 0.4 × B1, MAX = 0.6 × B1)	12.1	18.2	10.0	15.0	6.1	9.1	5.0	7.5	ns
B3	CLKOUT pulse width high (MIN = 0.4 × B1, MAX = 0.6 × B1)	12.1	18.2	10.0	15.0	6.1	9.1	5.0	7.5	ns
B4	CLKOUT rise time	—	4.00	—	4.00	—	4.00	—	4.00	ns
B5	CLKOUT fall time	—	4.00	—	4.00	—	4.00	—	4.00	ns
B7	CLKOUT to A(0:31), BADDR(28:30), RD/$\overline{WR}$, $\overline{BURST}$, D(0:31) output hold (MIN = 0.25 × B1)	7.60	—	6.30	—	3.80	—	3.13	—	ns
B7a	CLKOUT to TSIZ(0:1), $\overline{REG}$, $\overline{RSV}$, $\overline{BDIP}$, PTR output hold (MIN = 0.25 × B1)	7.60	—	6.30	—	3.80	—	3.13	—	ns
B7b	CLKOUT to $\overline{BR}$, $\overline{BG}$, FRZ, VFLS(0:1), VF(0:2) IWP(0:2), LWP(0:1), $\overline{STS}$ output hold (MIN = 0.25 × B1)	7.60	—	6.30	—	3.80	—	3.13	—	ns
B8	CLKOUT to A(0:31), BADDR(28:30), RD/$\overline{WR}$, $\overline{BURST}$, D(0:31) valid (MAX = 0.25 × B1 + 6.3)	—	13.80	—	12.50	—	10.00	—	9.43	ns
B8a	CLKOUT to TSIZ(0:1), $\overline{REG}$, $\overline{RSV}$, $\overline{BDIP}$, PTR valid (MAX = 0.25 × B1 + 6.3)	—	13.80	—	12.50	—	10.00	—	9.43	ns
B8b	CLKOUT to $\overline{BR}$, $\overline{BG}$, VFLS(0:1), VF(0:2), IWP(0:2), FRZ, LWP(0:1), $\overline{STS}$ valid [2] (MAX = 0.25 × B1 + 6.3)	—	13.80	—	12.50	—	10.00	—	9.43	ns
B9	CLKOUT to A(0:31), BADDR(28:30), RD/$\overline{WR}$, $\overline{BURST}$, D(0:31), TSIZ(0:1), $\overline{REG}$, $\overline{RSV}$, PTR High-Z (MAX = 0.25 × B1 + 6.3)	7.60	13.80	6.30	12.50	3.80	10.00	3.13	9.43	ns
B11	CLKOUT to $\overline{TS}$, $\overline{BB}$ assertion (MAX = 0.25 × B1 + 6.0)	7.60	13.60	6.30	12.30	3.80	9.80	3.13	9.13	ns
B11a	CLKOUT to $\overline{TA}$, $\overline{BI}$ assertion (when driven by the memory controller or PCMCIA interface) (MAX = 0.00 × B1 + 9.30[1])	2.50	9.30	2.50	9.30	2.50	9.80	2.5	9.3	ns
B12	CLKOUT to $\overline{TS}$, $\overline{BB}$ negation (MAX = 0.25 × B1 + 4.8)	7.60	12.30	6.30	11.00	3.80	8.50	3.13	7.92	ns
B12a	CLKOUT to $\overline{TA}$, $\overline{BI}$ negation (when driven by the memory controller or PCMCIA interface) (MAX = 0.00 × B1 + 9.00)	2.50	9.00	2.50	9.00	2.50	9.00	2.5	9.00	ns
B13	CLKOUT to $\overline{TS}$, $\overline{BB}$ High-Z (MIN = 0.25 × B1)	7.60	21.60	6.30	20.30	3.80	14.00	3.13	12.93	ns
B13a	CLKOUT to $\overline{TA}$, $\overline{BI}$ High-Z (when driven by the memory controller or PCMCIA interface) (MIN = 0.00 × B1 + 2.5)	2.50	15.00	2.50	15.00	2.50	15.00	2.5	15.00	ns
B14	CLKOUT to $\overline{TEA}$ assertion (MAX = 0.00 × B1 + 9.00)	2.50	9.00	2.50	9.00	2.50	9.00	2.50	9.00	ns

Table 10. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B15	CLKOUT to $\overline{\text{TEA}}$ High-Z (MIN = 0.00 × B1 + 2.50)	2.50	15.00	2.50	15.00	2.50	15.00	2.50	15.00	ns
B16	$\overline{\text{TA}}$, $\overline{\text{BI}}$ valid to CLKOUT (setup time) (MIN = 0.00 × B1 + 6.00)	6.00	—	6.00	—	6.00	—	6	—	ns
B16a	$\overline{\text{TEA}}$, $\overline{\text{KR}}$, $\overline{\text{RETRY}}$, $\overline{\text{CR}}$ valid to CLKOUT (setup time) (MIN = 0.00 × B1 + 4.5)	4.50	—	4.50	—	4.50	—	4.50	—	ns
B16b	$\overline{\text{BB}}$, $\overline{\text{BG}}$, $\overline{\text{BR}}$, valid to CLKOUT (setup time)[2] (4MIN = 0.00 × B1 + 0.00)	4.00	—	4.00	—	4.00	—	4.00	—	ns
B17	CLKOUT to $\overline{\text{TA}}$, $\overline{\text{TEA}}$, $\overline{\text{BI}}$, $\overline{\text{BB}}$, $\overline{\text{BG}}$, $\overline{\text{BR}}$ valid (hold time) (MIN = 0.00 × B1 + 1.00[3])	1.00	—	1.00	—	2.00	—	2.00	—	ns
B17a	CLKOUT to $\overline{\text{KR}}$, $\overline{\text{RETRY}}$, $\overline{\text{CR}}$ valid (hold time) (MIN = 0.00 × B1 + 2.00)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B18	D(0:31) valid to CLKOUT rising edge (setup time)[4] (MIN = 0.00 × B1 + 6.00)	6.00	—	6.00	—	6.00	—	6.00	—	ns
B19	CLKOUT rising edge to D(0:31) valid (hold time)[4] (MIN = 0.00 × B1 + 1.00[5])	1.00	—	1.00	—	2.00	—	2.00	—	ns
B20	D(0:31) valid to CLKOUT falling edge (setup time)[6] (MIN = 0.00 × B1 + 4.00)	4.00	—	4.00	—	4.00	—	4.00	—	ns
B21	CLKOUT falling edge to D(0:31) valid (hold time)[6] (MIN = 0.00 × B1 + 2.00)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B22	CLKOUT rising edge to $\overline{\text{CS}}$ asserted GPCM ACS = 00 (MAX = 0.25 × B1 + 6.3)	7.60	13.80	6.30	12.50	3.80	10.00	3.13	9.43	ns
B22a	CLKOUT falling edge to $\overline{\text{CS}}$ asserted GPCM ACS = 10, TRLX = 0 (MAX = 0.00 × B1 + 8.00)	—	8.00	—	8.00	—	8.00	—	8.00	ns
B22b	CLKOUT falling edge to $\overline{\text{CS}}$ asserted GPCM ACS = 11, TRLX = 0, EBDF = 0 (MAX = 0.25 × B1 + 6.3)	7.60	13.80	6.30	12.50	3.80	10.00	3.13	9.43	ns
B22c	CLKOUT falling edge to $\overline{\text{CS}}$ asserted GPCM ACS = 11, TRLX = 0, EBDF = 1 (MAX = 0.375 × B1 + 6.6)	10.90	18.00	10.90	16.00	5.20	12.30	4.69	10.93	ns
B23	CLKOUT rising edge to $\overline{\text{CS}}$ negated GPCM read access, GPCM write access ACS = 00, TRLX = 0 and CSNT = 0 (MAX = 0.00 × B1 + 8.00)	2.00	8.00	2.00	8.00	2.00	8.00	2.00	8.00	ns
B24	A(0:31) and BADDR(28:30) to $\overline{\text{CS}}$ asserted GPCM ACS = 10, TRLX = 0 (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	1.80	—	1.13	—	ns
B24a	A(0:31) and BADDR(28:30) to $\overline{\text{CS}}$ asserted GPCM ACS = 11, TRLX = 0 (MIN = 0.50 × B1 – 2.00)	13.20	—	10.50	—	5.60	—	4.25	—	ns

Table 10. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B30d	$\overline{WE}$(0:3)/BS_B[0:3] negated to A(0:31), BADDR(28:30) invalid GPCM write access TRLX = 1, CSNT =1, $\overline{CS}$ negated to A(0:31) invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10 or 11, EBDF = 1	38.67	—	31.38	—	17.83	—	14.19	—	ns
B31	CLKOUT falling edge to $\overline{CS}$ valid as requested by control bit CST4 in the corresponding word in the UPM (MAX = 0.00 × B1 + 6.00)	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B31a	CLKOUT falling edge to $\overline{CS}$ valid as requested by control bit CST1 in the corresponding word in the UPM (MAX = 0.25 × B1 + 6.80)	7.60	14.30	6.30	13.00	3.80	10.50	3.13	10.00	ns
B31b	CLKOUT rising edge to $\overline{CS}$ valid, as requested by control bit CST2 in the corresponding word in the UPM (MAX = 0.00 × B1 + 8.00)	1.50	8.00	1.50	8.00	1.50	8.00	1.50	8.00	ns
B31c	CLKOUT rising edge to $\overline{CS}$ valid, as requested by control bit CST3 in the corresponding word in the UPM (MAX = 0.25 × B1 + 6.30)	7.60	13.80	6.30	12.50	3.80	10.00	3.13	9.40	ns
B31d	CLKOUT falling edge to $\overline{CS}$ valid as requested by control bit CST1 in the corresponding word in the UPM EBDF = 1 (MAX = 0.375 × B1 + 6.6)	13.30	18.00	11.30	16.00	7.60	12.30	4.69	11.30	ns
B32	CLKOUT falling edge to $\overline{BS}$ valid as requested by control bit BST4 in the corresponding word in the UPM (MAX = 0.00 × B1 + 6.00)	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B32a	CLKOUT falling edge to $\overline{BS}$ valid as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 0 (MAX = 0.25 × B1 + 6.80)	7.60	14.30	6.30	13.00	3.80	10.50	3.13	10.00	ns
B32b	CLKOUT rising edge to $\overline{BS}$ valid, as requested by control bit BST2 in the corresponding word in the UPM (MAX = 0.00 × B1 + 8.00)	1.50	8.00	1.50	8.00	1.50	8.00	1.50	8.00	ns
B32c	CLKOUT rising edge to $\overline{BS}$ valid, as requested by control bit BST3 in the corresponding word in the UPM (MAX = 0.25 × B1 + 6.80)	7.60	14.30	6.30	13.00	3.80	10.50	3.13	10.00	ns
B32d	CLKOUT falling edge to $\overline{BS}$ valid as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 1 (MAX = 0.375 × B1 + 6.60)	13.30	18.00	11.30	16.00	7.60	12.30	4.49	11.30	ns
B33	CLKOUT falling edge to $\overline{GPL}$ valid as requested by control bit GxT4 in the corresponding word in the UPM (MAX = 0.00 × B1 + 6.00)	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns

Figure 9 provides the timing for the synchronous input signals.

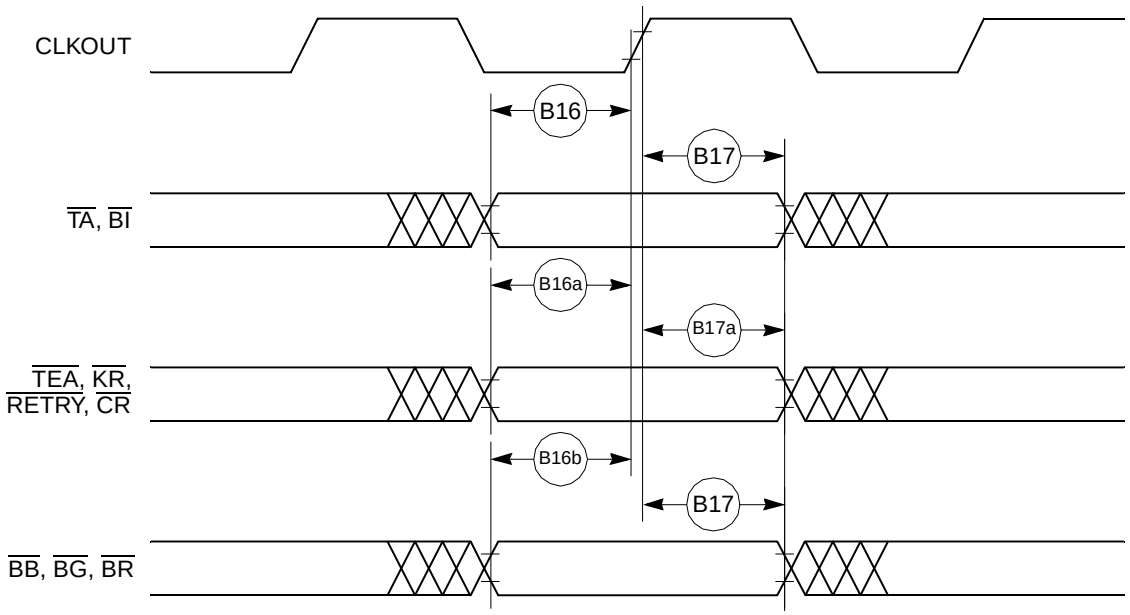

Figure 9. Synchronous Input Signals Timing

Figure 10 provides normal case timing for input data. It also applies to normal read accesses under the control of the user-programmable machine (UPM) in the memory controller.

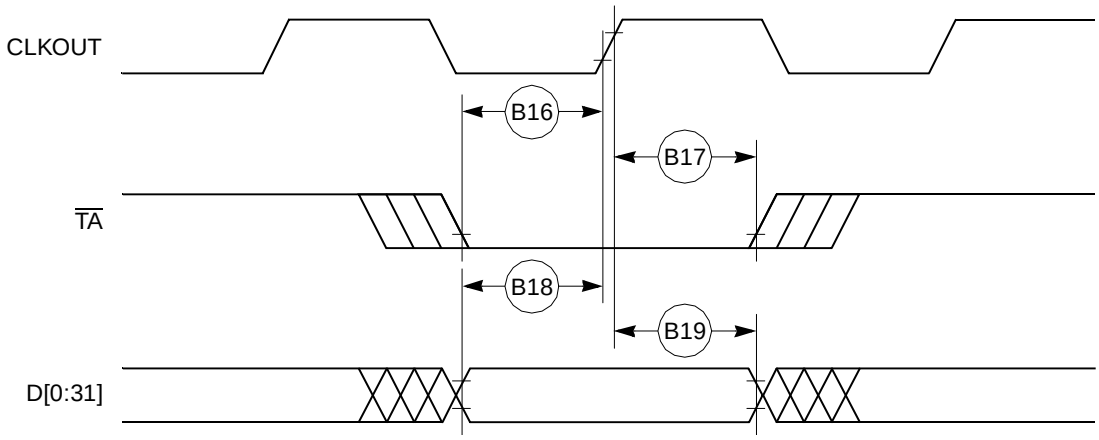

Figure 10. Input Data Timing in Normal Case

Figure 16 through Figure 18 provide the timing for the external bus write controlled by various GPCM factors.

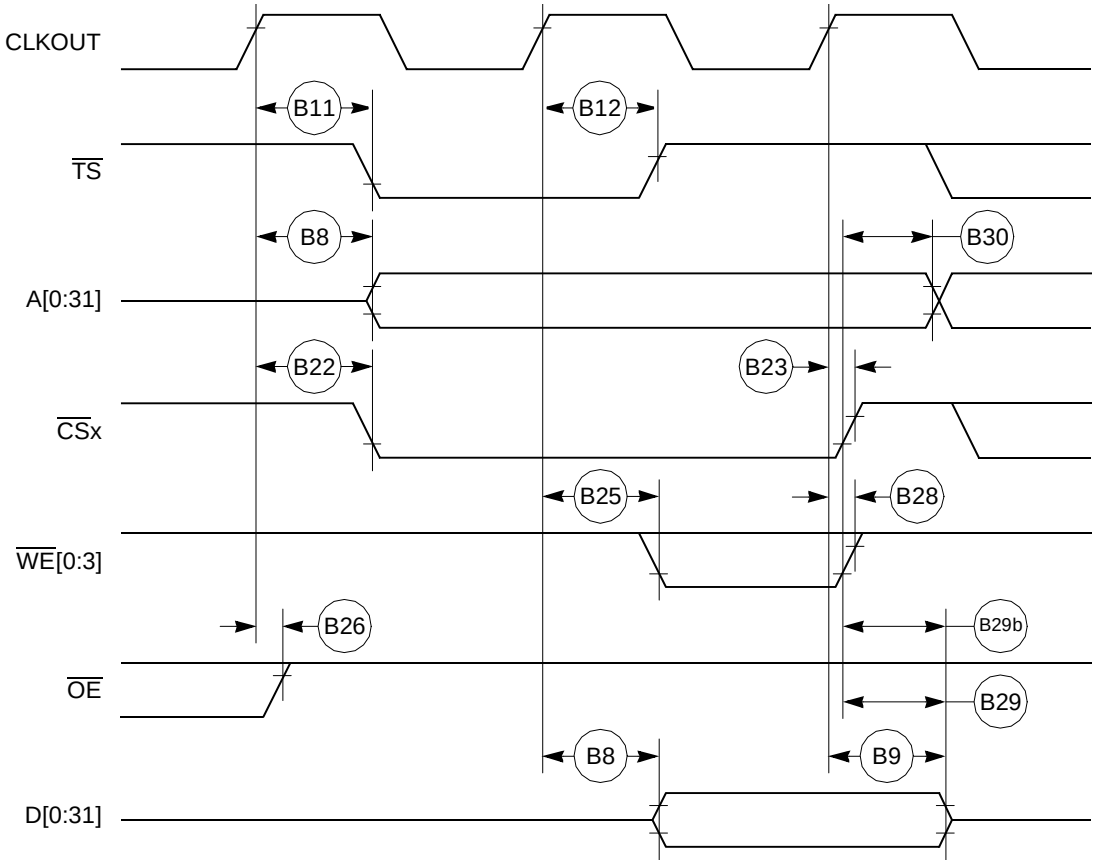

Figure 16. External Bus Write Timing (GPCM Controlled—TRLX = 0, CSNT = 0)

Figure 20 provides the timing for the asynchronous asserted UPWAIT signal controlled by the UPM.

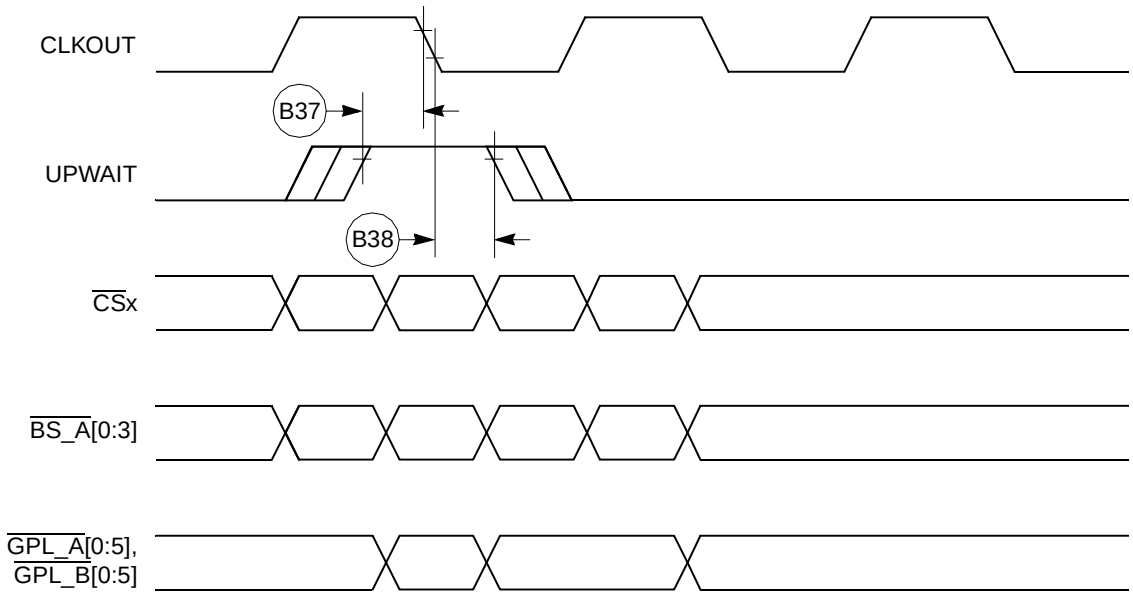

Figure 20. Asynchronous UPWAIT Asserted Detection in UPM Handled Cycles Timing

Figure 21 provides the timing for the asynchronous negated UPWAIT signal controlled by the UPM.

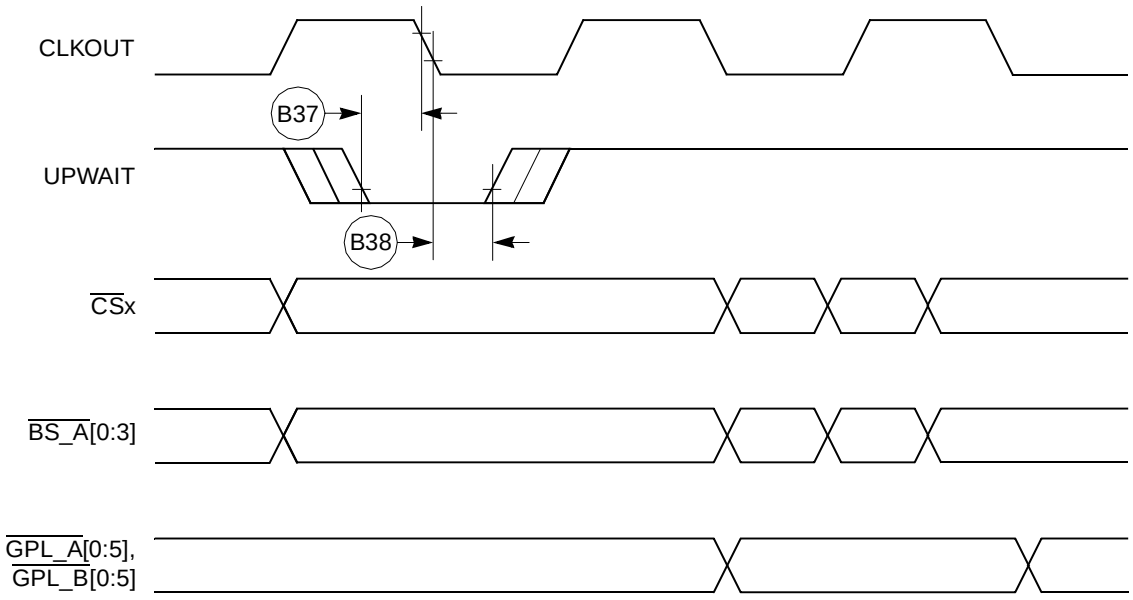

Figure 21. Asynchronous UPWAIT Negated Detection in UPM Handled Cycles Timing

Table 11 provides the interrupt timing for the MPC875/MPC870.

Table 11. Interrupt Timing

Num	Characteristic[1]	All Frequencies		Unit
		Min	Max	
I39	$\overline{\text{IRQ}}$x valid to CLKOUT rising edge (setup time)	6.00		ns
I40	$\overline{\text{IRQ}}$x hold time after CLKOUT	2.00		ns
I41	$\overline{\text{IRQ}}$x pulse width low	3.00		ns
I42	$\overline{\text{IRQ}}$x pulse width high	3.00		ns
I43	$\overline{\text{IRQ}}$x edge-to-edge time	$4 \times T_{CLOCKOUT}$		—

1 The I39 and I40 timings describe the testing conditions under which the $\overline{\text{IRQ}}$ lines are tested when being defined as level sensitive. The $\overline{\text{IRQ}}$ lines are synchronized internally and do not have to be asserted or negated with reference to the CLKOUT. The I41, I42, and I43 timings are specified to allow correct functioning of the $\overline{\text{IRQ}}$ lines detection circuitry and have no direct relation with the total system interrupt latency that the MPC875/MPC870 is able to support.

Figure 25 provides the interrupt detection timing for the external level-sensitive lines.

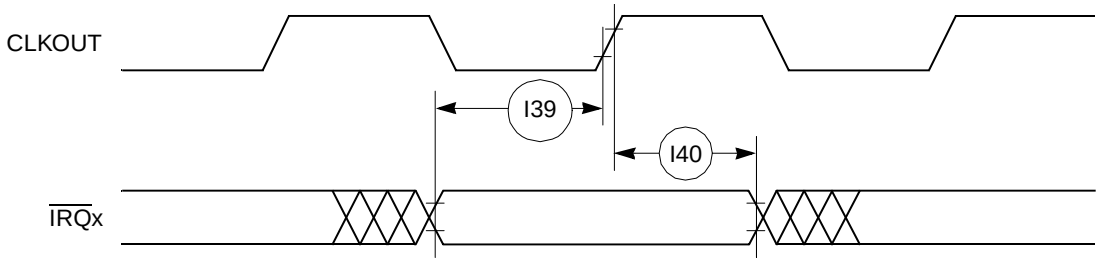

Figure 25. Interrupt Detection Timing for External Level Sensitive Lines

Figure 26 provides the interrupt detection timing for the external edge-sensitive lines.

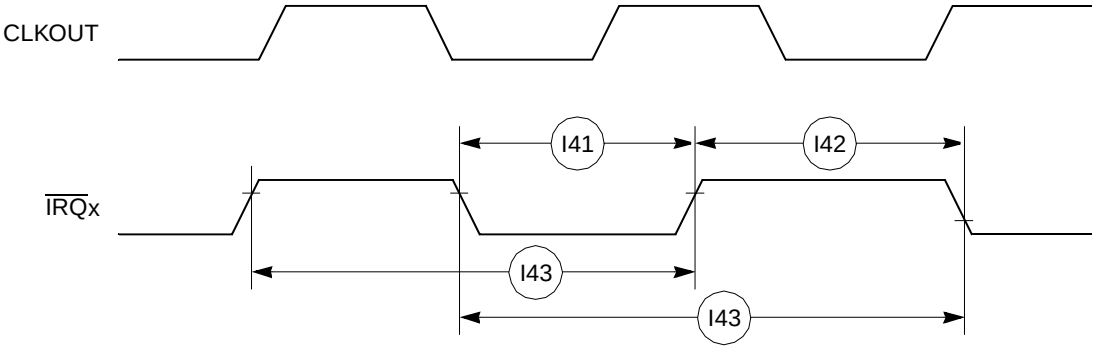

Figure 26. Interrupt Detection Timing for External Edge-Sensitive Lines

Figure 27 provides the PCMCIA access cycle timing for the external bus read.

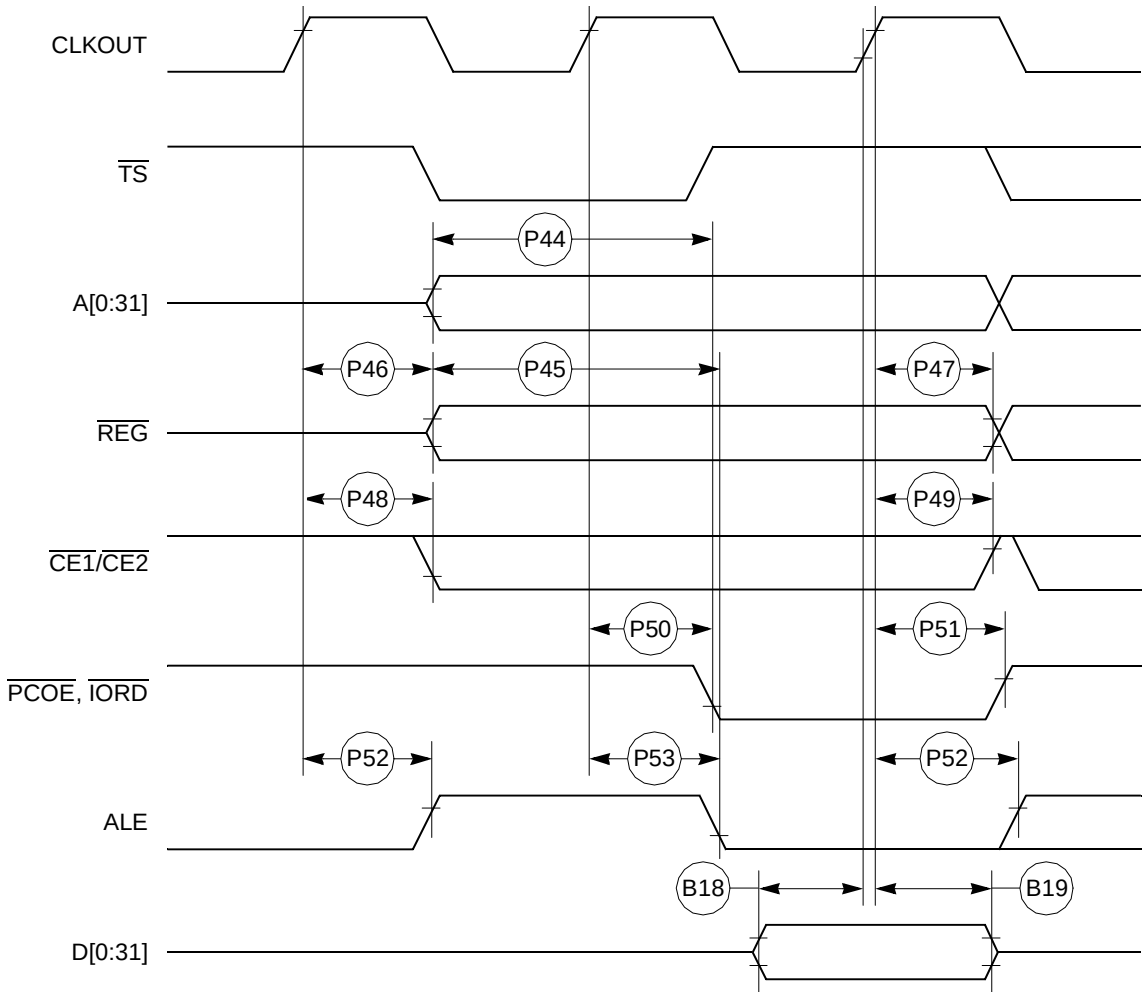

Figure 27. PCMCIA Access Cycles Timing External Bus Read

Table 13 shows the PCMCIA port timing for the MPC875/MPC870.

Table 13. PCMCIA Port Timing

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
P57	CLKOUT to OPx valid (MAX = 0.00 × B1 + 19.00)	—	19.00	—	19.00	—	19.00	—	19.00	ns
P58	$\overline{\text{HRESET}}$ negated to OPx drive[1] (MIN = 0.75 × B1 + 3.00)	25.70	—	21.70	—	14.40	—	12.40	—	ns
P59	IP_Xx valid to CLKOUT rising edge (MIN = 0.00 × B1 + 5.00)	5.00	—	5.00	—	5.00	—	5.00	—	ns
P60	CLKOUT rising edge to IP_Xx invalid (MIN = 0.00 × B1 + 1.00)	1.00	—	1.00	—	1.00	—	1.00	—	ns

1 OP2 and OP3 only.

Figure 30 provides the PCMCIA output port timing for the MPC875/MPC870.

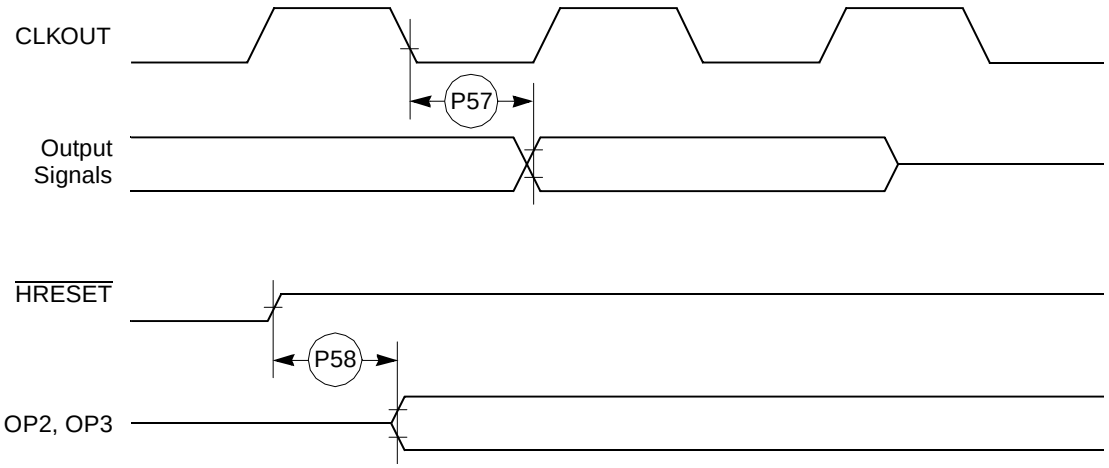

Figure 30. PCMCIA Output Port Timing

Figure 31 provides the PCMCIA input port timing for the MPC875/MPC870.

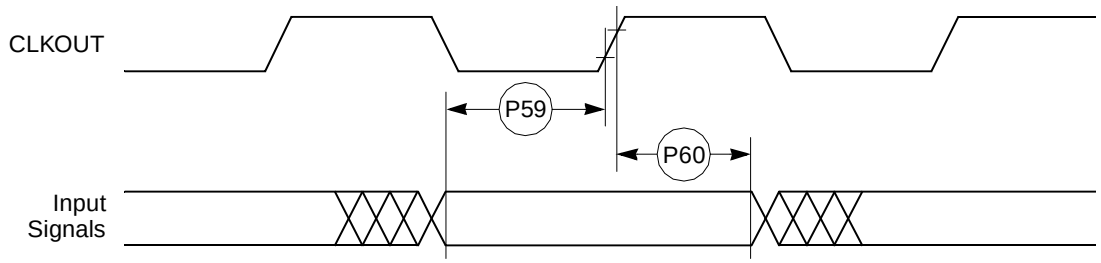

Figure 31. PCMCIA Input Port Timing

Table 21. SI Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
83a	L1RCLKB, L1TCLKB width high (DSC = 1)[3]	P + 10	—	ns
84	L1CLKB edge to L1CLKOB valid (DSC = 1)	—	30.00	ns
85	$\overline{\text{L1RQB}}$ valid before falling edge of L1TSYNCB[4]	1.00	—	L1TCLK
86	L1GRB setup time[2]	42.00	—	ns
87	L1GRB hold time	42.00	—	ns
88	L1CLKB edge to L1SYNCB valid (FSD = 00) CNT = 0000, BYT = 0, DSC = 0)	—	0.00	ns

1 The ratio SYNCCLK/L1RCLKB must be greater than 2.5/1.
2 These specs are valid for IDL mode only.
3 Where P = 1/CLKOUT. Thus, for a 25-MHz CLKO1 rate, P = 40 ns.
4 These strobes and TxD on the first bit of the frame become valid after the L1CLKB edge or L1SYNCB, whichever comes later.

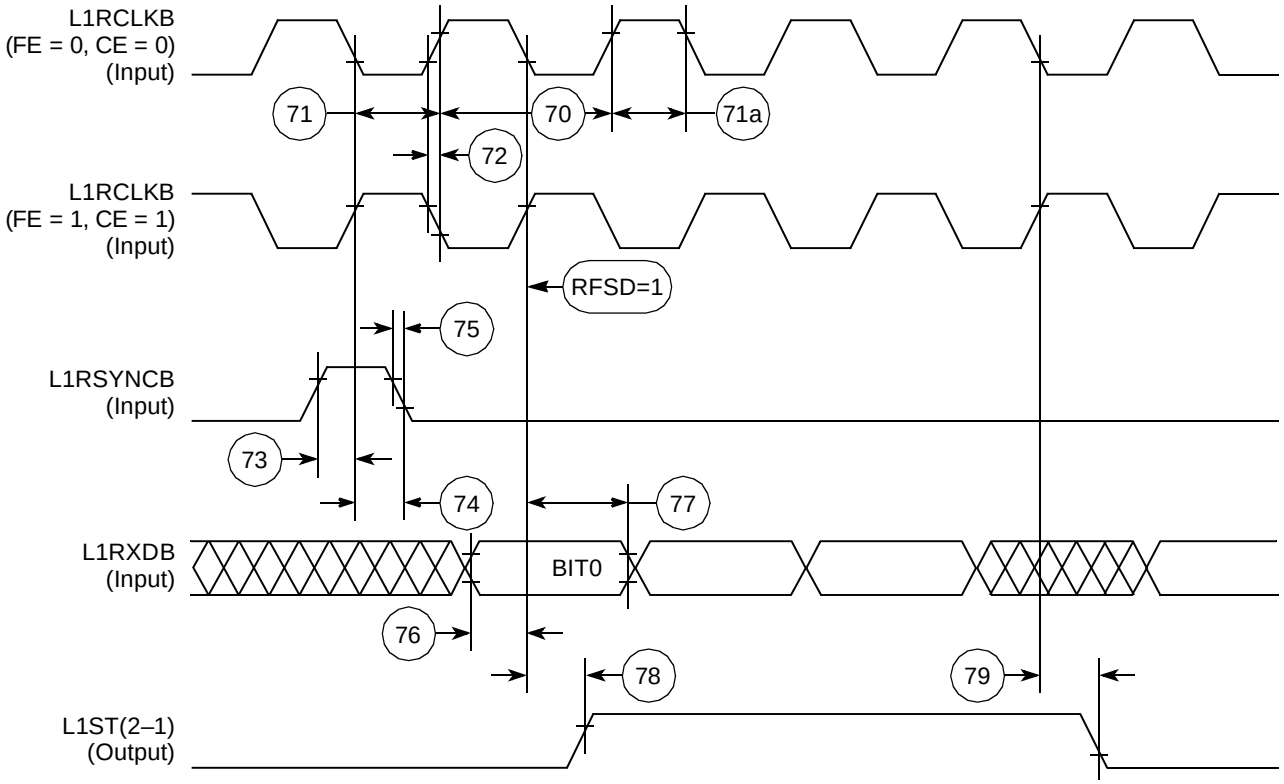

Figure 48. SI Receive Timing Diagram with Normal Clocking (DSC = 0)

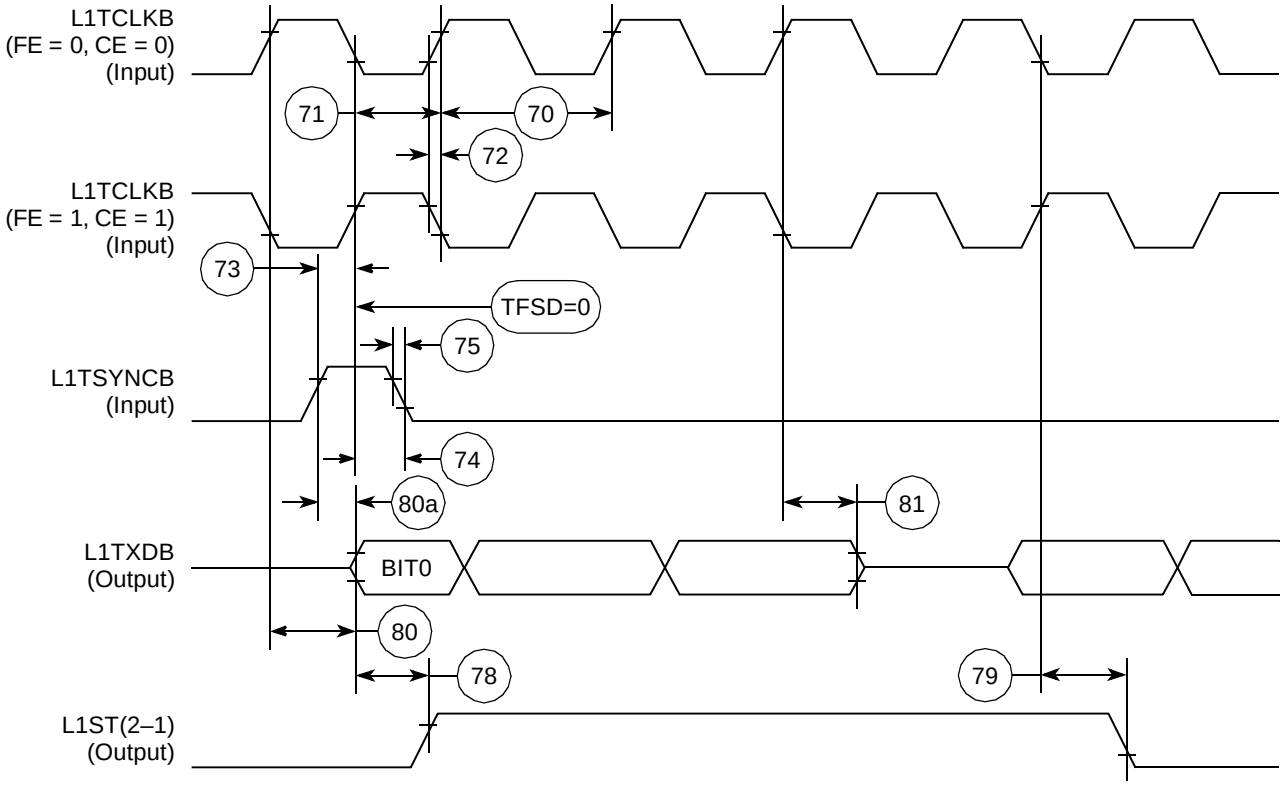

Figure 50. SI Transmit Timing Diagram (DSC = 0)

Table 28. I²C Timing (SCL < 100 kHz) (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
210	SDL/SCL fall time	—	300	ns
211	Stop condition setup time	4.7	—	µs

1 SCL frequency is given by SCL = BRGCLK_frequency/((BRG register + 3) × pre_scalar × 2).
The ratio SYNCCLK/(BRGCLK/pre_scalar) must be greater than or equal to 4/1.

Table 29 provides the I²C (SCL > 100 kHz) timings.

Table 29. I²C Timing (SCL > 100 kHz)

Num	Characteristic	Expression	All Frequencies		Unit
			Min	Max	
200	SCL clock frequency (slave)	fSCL	0	BRGCLK/48	Hz
200	SCL clock frequency (master)[1]	fSCL	BRGCLK/16512	BRGCLK/48	Hz
202	Bus free time between transmissions	—	1/(2.2 × fSCL)	—	s
203	Low period of SCL	—	1/(2.2 × fSCL)	—	s
204	High period of SCL	—	1/(2.2 × fSCL)	—	s
205	Start condition setup time	—	1/(2.2 × fSCL)	—	s
206	Start condition hold time	—	1/(2.2 × fSCL)	—	s
207	Data hold time	—	0	—	s
208	Data setup time	—	1/(40 × fSCL)	—	s
209	SDL/SCL rise time	—	—	1/(10 × fSCL)	s
210	SDL/SCL fall time	—	—	1/(33 × fSCL)	s
211	Stop condition setup time	—	1/2(2.2 × fSCL)	—	s

1 SCL frequency is given by SCL = BRGCLK_frequency/((BRG register + 3) × pre_scalar × 2).
The ratio SYNCCLK/(BRGCLK/pre_scalar) must be greater than or equal to 4/1.

Figure 64 shows the I²C bus timing.

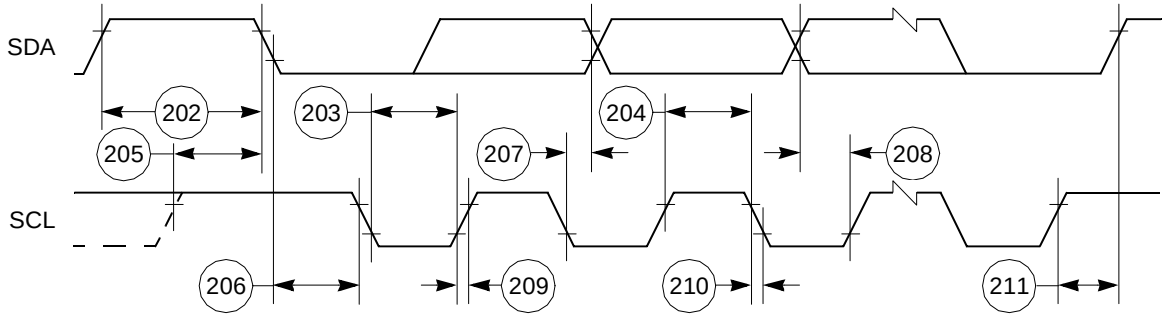

Figure 64. I²C Bus Timing Diagram

Figure 65 shows MII receive signal timing.

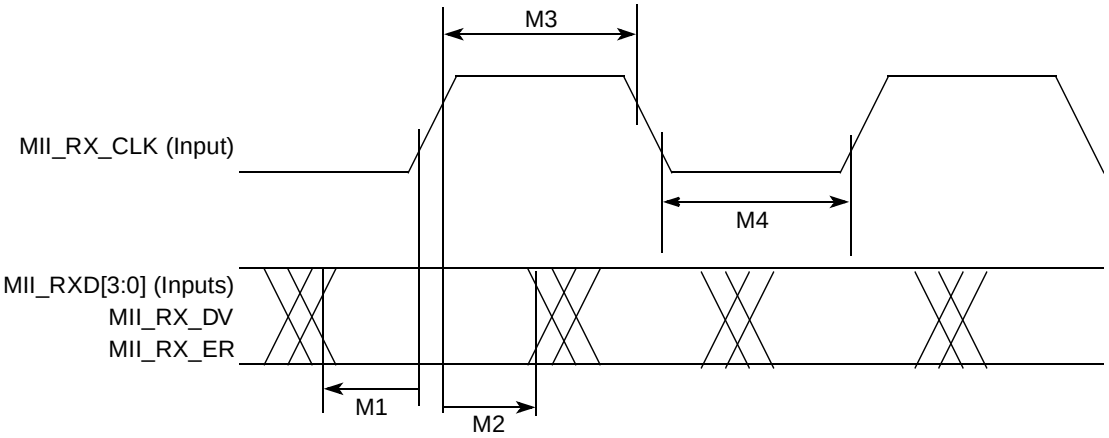

Figure 65. MII Receive Signal Timing Diagram

15.2 MII and Reduced MII Transmit Signal Timing

The transmitter functions correctly up to a MII_TX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_TX_CLK frequency – 1%.

Table 32 provides information on the MII transmit signal timing.

Table 32. MII Transmit Signal Timing

Num	Characteristic	Min	Max	Unit
M5	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER invalid	5	—	ns
M6	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER valid	—	25	ns
M7	MII_TX_CLK pulse width high	35%	65%	MII_TX_CLK period
M8	MII_TX_CLK pulse width low	35%	65%	MII_TX_CLK period
M20_RMII	RMII_TXD[1:0], RMII_TX_EN to RMII_REFCLK setup	4	—	ns
M21_RMII	RMII_TXD[1:0], RMII_TX_EN data hold from RMII_REFCLK rising edge	2	—	ns

Figure 66 shows the MII transmit signal timing diagram.

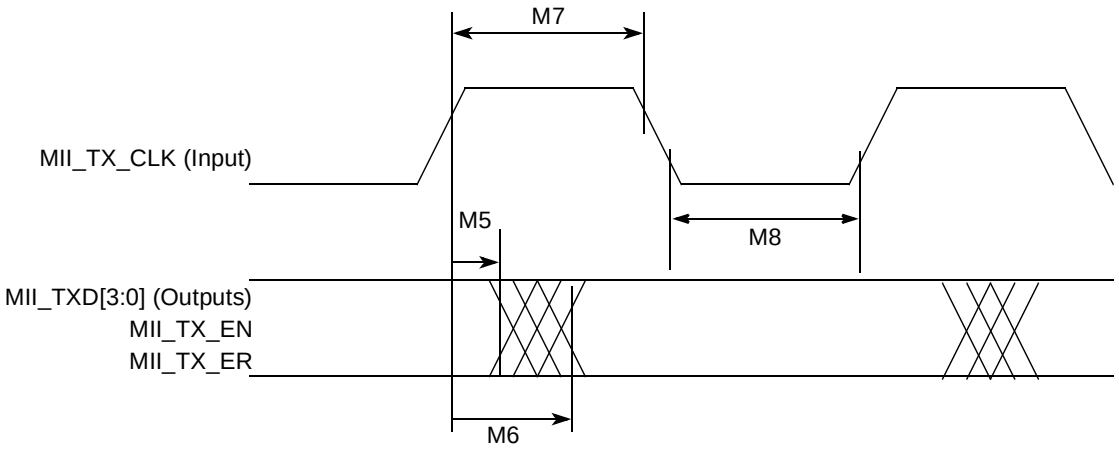

Figure 66. MII Transmit Signal Timing Diagram

15.3 MII Async Inputs Signal Timing (MII_CRS, MII_COL)

Table 33 provides information on the MII async inputs signal timing.

Table 33. MII Async Inputs Signal Timing

Num	Characteristic	Min	Max	Unit
M9	MII_CRS, MII_COL minimum pulse width	1.5	—	MII_TX_CLK period

Figure 67 shows the MII asynchronous inputs signal timing diagram.

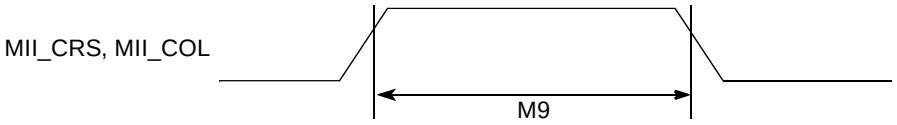

Figure 67. MII Async Inputs Timing Diagram

15.4 MII Serial Management Channel Timing (MII_MDIO, MII_MDC)

Table 34 provides information on the MII serial management channel signal timing. The FEC functions correctly with a maximum MDC frequency in excess of 2.5 MHz.

Table 34. MII Serial Management Channel Timing

Num	Characteristic	Min	Max	Unit
M10	MII_MDC falling edge to MII_MDIO output invalid (minimum propagation delay)	0	—	ns
M11	MII_MDC falling edge to MII_MDIO output valid (max prop delay)	—	25	ns
M12	MII_MDIO (input) to MII_MDC rising edge setup	10	—	ns
M13	MII_MDIO (input) to MII_MDC rising edge hold	0	—	ns
M14	MII_MDC pulse width high	40%	60%	MII_MDC period
M15	MII_MDC pulse width low	40%	60%	MII_MDC period

Table 36. Pin Assignments—JEDEC Standard (continued)

Name	Pin Number	Type
PE29, MII2-CRS	U7	Bidirectional (Optional: open-drain)
PE28, $\overline{\text{TOUT3}}$, MII2-COL	R7	Bidirectional (Optional: open-drain)
PE27, L1RQB, MII2-RXERR, RMII2-RXERR	T6	Bidirectional (Optional: open-drain)
PE26, L1CLKOB, MII2-RXDV, RMII2-CRS_DV	T2	Bidirectional (Optional: open-drain)
PE25, RXD4, MII2-RXD3, L1ST2	R4	Bidirectional (Optional: open-drain)
PE24, SMRXD1, BRGO1, MII2-RXD2	U8	Bidirectional (Optional: open-drain)
PE23, TXD4, MII2-RXCLK, L1ST1	U4	Bidirectional (Optional: open-drain)
PE22, TOUT2, MII2-RXD1, RMII2-RXD1, SDACK1	P4	Bidirectional (Optional: open-drain)
PE21, $\overline{\text{TOUT1}}$, MII2-RXD0, RMII2-RXD0	T9	Bidirectional (Optional: open-drain)
PE20, MII2-TXER	U3	Bidirectional (Optional: open-drain)
PE19, L1TXDB, MII2-TXEN, RMII2-TXEN	R6	Bidirectional (Optional: open-drain)
PE18, SMTXD1, MII2-TXD3	M5	Bidirectional (Optional: open-drain)
PE17, TIN3, CLK5, BRGO3, $\overline{\text{SMSYN1}}$, MII2-TXD2	T8	Bidirectional (Optional: open-drain)
PE16, L1RCLKB, CLK6, MII2-TXCLK, RMII2-REFCLK	U6	Bidirectional (Optional: open-drain)
PE15, $\overline{\text{TGATE1}}$, MII2-TXD1, RMII2-TXD1	T7	Bidirectional
PE14, MII2-TXD0, RMII2-TXD0	P8	Bidirectional
TMS	T14	Input (5-V tolerant)
TDI, DSDI	T13	Input (5-V tolerant)
TCK, DSCK	R13	Input (5-V tolerant)
$\overline{\text{TRST}}$	U14	Input (5-V tolerant)

Table 36. Pin Assignments—JEDEC Standard (continued)

Name	Pin Number	Type
TDO, DSDO	P13	Output (5-V tolerant)
MII1_CRS	U10	Input
MII_MDIO	M13	Bidirectional (5-V tolerant)
MII1_TX_EN, RMII1_TX_EN	U5	Output (5-V tolerant)
MII1_COL	R10	Input
V_{SSSYN}	E5	PLL analog GND
V_{SSSYN1}	F6	PLL analog GND
V_{DDSYN}	E6	PLL analog V_{DD}
GND	H8, H9, H10, H11, J8, J9, J10, J11, K8, K9, K10, K11, L8, L9, L10, L11, U15	Power
V_{DDL}	F7, F8, F9, F10, F11, H6, H13, J6, J13, K6, K13, L6, L13, N7, N8, N9, N10, N11	Power
V_{DDH}	G7, G8, G9, G10, G11, G12, H7, H12, J7, J12, K7, K12, L7, L12, M7, M8, M9, M10, M11, M12	Power
N/C	B17, T16, U2, U17	No connect

Table 37. Document Revision History (continued)

Revision Number	Date	Changes
3.0	1/07/2004 7/19/2004	• Added sentence to Spec B1A about EXTCLK and CLKOUT being in alignment for integer values. • Added a footnote to Spec 41 specifying that EDM = 1. • Added the thermal numbers to Table 4. • Added RMII1_EN under M1II_EN in Table 36, Pin Assignments. • Added a table footnote to Table 6, DC Electrical Specifications, about meeting the V_{IL} Max of the I^2C Standard. • Put the new part numbers in the Ordering Information Section.
4	08/2007	• Updated template. • On page 1, updated first paragraph and added a second paragraph. • After Table 2, inserted a new figure showing the undershoot/overshoot voltage (Figure 3) and renumbered the rest of the figures. • In Table 10, for reset timings B29f and B29g added footnote indicating that the formula only applies to bus operation up to 50 MHz. • In Figure 5, changed all reference voltage measurement points from 0.2 and 0.8 V to 50% level. • In Table 18, changed num 46 description to read, "$\overline{TA}$ assertion to rising edge ..." • In Figure 43, changed $\overline{TA}$ to reflect the rising edge of the clock.

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