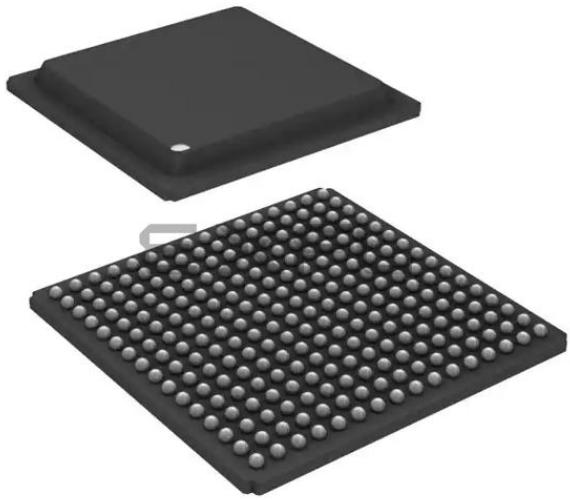

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	133MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (2)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 100°C (TA)
Security Features	-
Package / Case	256-BBGA
Supplier Device Package	256-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc870czt133

- Thirty-two address lines
- Memory controller (eight banks)
  - Contains complete dynamic RAM (DRAM) controller
  - Each bank can be a chip select or $\overline{\text{RAS}}$ to support a DRAM bank
  - Up to 30 wait states programmable per memory bank
  - Glueless interface to DRAM, SIMMS, SRAM, EPROMs, Flash EPROMs, and other memory devices
  - DRAM controller programmable to support most size and speed memory interfaces
  - Four $\overline{\text{CAS}}$ lines, four $\overline{\text{WE}}$ lines, and one $\overline{\text{OE}}$ line
  - Boot chip-select available at reset (options for 8-, 16-, or 32-bit memory)
  - Variable block sizes (32 Kbytes–256 Mbytes)
  - Selectable write protection
  - On-chip bus arbitration logic
- General-purpose timers
  - Four 16-bit timers or two 32-bit timers
  - Gate mode can enable/disable counting
  - Interrupt can be masked on reference match and event capture
- Two Fast Ethernet controllers (FEC)—Two 10/100 Mbps Ethernet/IEEE Std. 802.3® CDMA/CS that interface through MII and/or RMII interfaces
- System integration unit (SIU)
  - Bus monitor
  - Software watchdog
  - Periodic interrupt timer (PIT)
  - Clock synthesizer
  - Decrementer and time base
  - Reset controller
  - IEEE 1149.1™ Std. test access port (JTAG)
- Security engine is optimized to handle all the algorithms associated with IPsec, SSL/TLS, SRTP, IEEE 802.11i® standard, and iSCSI processing. Available on the MPC875, the security engine contains a crypto-channel, a controller, and a set of crypto hardware accelerators (CHAs). The CHAs are:
  - Data encryption standard execution unit (DEU)
    - DES, 3DES
    - Two key (K1, K2, K1) or three key (K1, K2, K3)
    - ECB and CBC modes for both DES and 3DES
  - Advanced encryption standard unit (AESU)
    - Implements the Rijndael symmetric key cipher

  - ECB, CBC, and counter modes
  - 128-, 192-, and 256-bit key lengths
- Message digest execution unit (MDEU)
  - SHA with 160- or 256-bit message digest
  - MD5 with 128-bit message digest
  - HMAC with either algorithm
- Master/slave logic, with DMA
  - 32-bit address/32-bit data
  - Operation at MPC8xx bus frequency
- Crypto-channel supporting multi-command descriptors
  - Integrated controller managing crypto-execution units
  - Buffer size of 256 bytes for each execution unit, with flow control for large data sizes

- Interrupts
  - Six external interrupt request (IRQ) lines
  - Twelve port pins with interrupt capability
  - Twenty-three internal interrupt sources
  - Programmable priority between SCCs
  - Programmable highest priority request
- Communications processor module (CPM)
  - RISC controller
  - Communication-specific commands (for example, GRACEFUL STOP TRANSMIT, ENTER HUNT MODE, and RESTART TRANSMIT)
  - Supports continuous mode transmission and reception on all serial channels
  - 8-Kbytes of dual-port RAM
  - Several serial DMA (SDMA) channels to support the CPM
  - Three parallel I/O registers with open-drain capability
- On-chip 16 × 16 multiply accumulate controller (MAC)
  - One operation per clock (two-clock latency, one-clock blockage)
  - MAC operates concurrently with other instructions
  - FIR loop—Four clocks per four multiplies
- Four baud-rate generators
  - Independent (can be connected to SCC or SMC)
  - Allows changes during operation
  - Autobaud support option
- SCC (serial communication controller)
  - Ethernet/IEEE 802.3® standard, supporting full 10-Mbps operation
  - HDLC/SDLC

Table 3. Operating Temperatures

Rating	Symbol	Value	Unit
Temperature [1] (standard)	$T_{A(min)}$	0	°C
	$T_{J(max)}$	95	°C
Temperature (extended)	$T_{A(min)}$	–40	°C
	$T_{J(max)}$	100	°C

1 Minimum temperatures are guaranteed as ambient temperature, T_A. Maximum temperatures are guaranteed as junction temperature, T_J.

This device contains circuitry protecting against damage due to high-static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{DDH}).

4 Thermal Characteristics

Table 4 shows the thermal characteristics for the MPC875/MPC870.

Table 4. MPC875/MPC870 Thermal Resistance Data

Rating	Environment		Symbol	Value	Unit
Junction-to-ambient[1]	Natural convection	Single-layer board (1s)	$R_{\theta JA}$[2]	43	°C/W
		Four-layer board (2s2p)	$R_{\theta JMA}$[3]	29	
	Airflow (200 ft/min)	Single-layer board (1s)	$R_{\theta JMA}$[3]	36	
		Four-layer board (2s2p)	$R_{\theta JMA}$[3]	26	
Junction-to-board[4]			$R_{\theta JB}$	20	
Junction-to-case [5]			$R_{\theta JC}$	10	
Junction-to-package top[6]	Natural convection		Ψ_{JT}	2	
	Airflow (200 ft/min)		Ψ_{JT}	2	

1 Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.
2 Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.
3 Per JEDEC JESD51-6 with the board horizontal.
4 Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5 Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature. For exposed pad packages where the pad would be expected to be soldered, junction-to-case thermal resistance is a simulated value from the junction to the exposed pad without contact resistance.
6 Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2.

5 Power Dissipation

Table 5 provides information on power dissipation. The modes are 1:1, where CPU and bus speeds are equal, and 2:1, where CPU frequency is twice bus speed.

Table 5. Power Dissipation (P_D)

Die Revision	Bus Mode	Frequency	Typical[1]	Maximum[2]	Unit
0	1:1	66 MHz	310	390	mW
		80 MHz	350	430	mW
	2:1	133 MHz	430	495	mW

1 Typical power dissipation is measured at $V_{DDL} = V_{DDSYN} = 1.8$ V, and V_{DDH} is at 3.3 V.
2 Maximum power dissipation at $V_{DDL} = V_{DDSYN} = 1.9$ V, and V_{DDH} is at 3.5 V.

NOTE

The values in Table 5 represent V_{DDL}-based power dissipation and do not include I/O power dissipation over V_{DDH}. I/O power dissipation varies widely by application due to buffer current, depending on external circuitry.

The V_{DDSYN} power dissipation is negligible.

6 DC Characteristics

Table 6 provides the DC electrical characteristics for the MPC875/MPC870.

Table 6. DC Electrical Specifications

Characteristic	Symbol	Min	Max	Unit
Operating voltage	V_{DDH} (I/O)	3.135	3.465	V
	V_{DDL} (core)	1.7	1.9	V
	V_{DDSYN}[1]	1.7	1.9	V
	Difference between V_{DDL} and V_{DDSYN}	—	100	mV
Input high voltage (all inputs except EXTAL and EXTCLK)[2]	V_{IH}	2.0	3.465	V
Input low voltage[3]	V_{IL}	GND	0.8	V
EXTAL, EXTCLK input high voltage	V_{IHC}	$0.7 \times V_{DDH}$	V_{DDH}	V
Input leakage current, $V_{in} = 5.5$ V (except TMS, $\overline{\text{TRST}}$, DSCK, and DSDI pins) for 5-V tolerant pins[1]	I_{in}	—	100	µA
Input leakage current, $V_{in} = V_{DDH}$ (except TMS, $\overline{\text{TRST}}$, DSCK, and DSDI)	I_{In}	—	10	µA
Input leakage current, $V_{in} = 0$ V (except TMS, $\overline{\text{TRST}}$, DSCK, and DSDI pins)	I_{In}	—	10	µA
Input capacitance[4]	C_{in}	—	20	pF

Figure 9 provides the timing for the synchronous input signals.

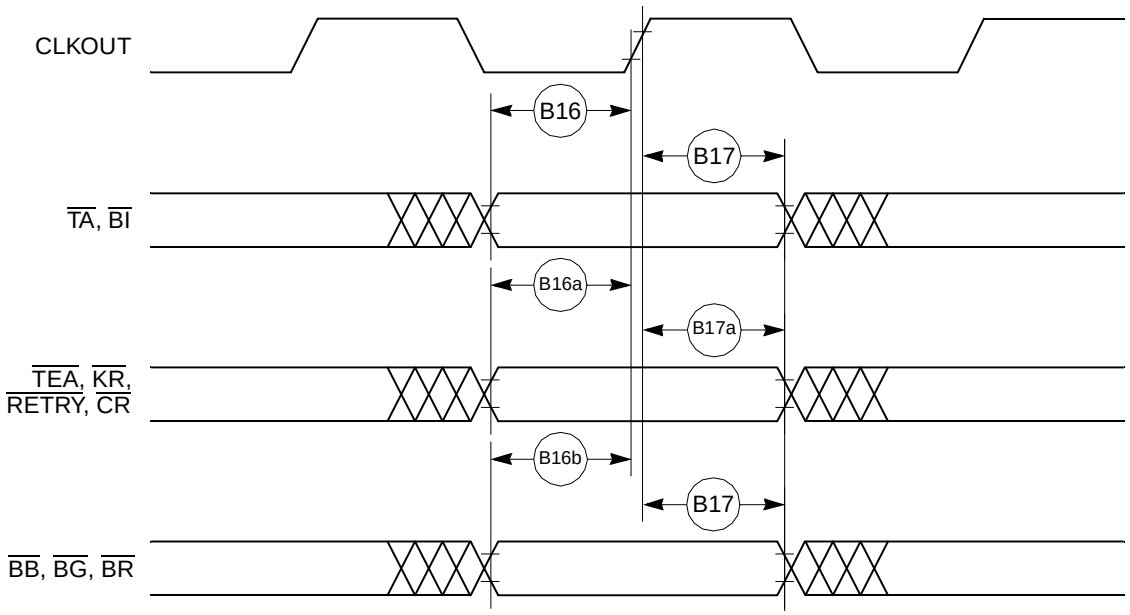


Figure 9. Synchronous Input Signals Timing

Figure 10 provides normal case timing for input data. It also applies to normal read accesses under the control of the user-programmable machine (UPM) in the memory controller.

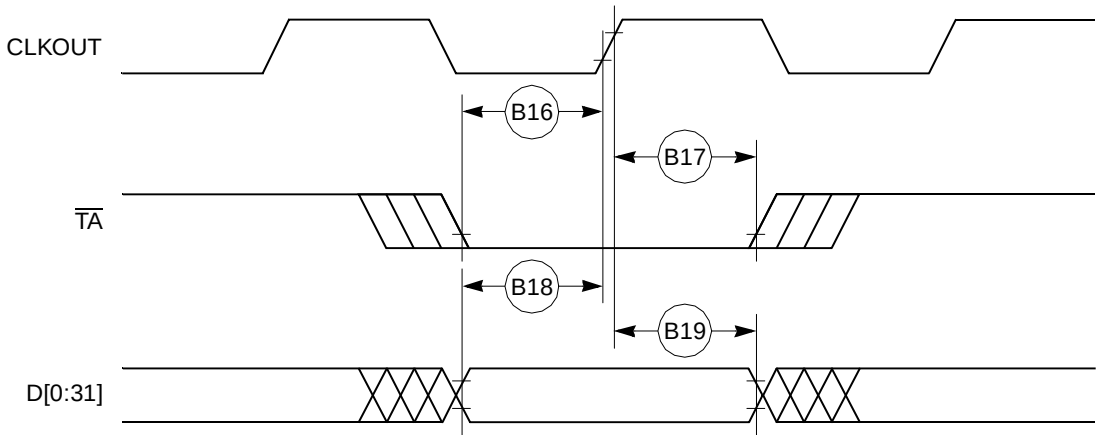


Figure 10. Input Data Timing in Normal Case

Figure 16 through Figure 18 provide the timing for the external bus write controlled by various GPCM factors.

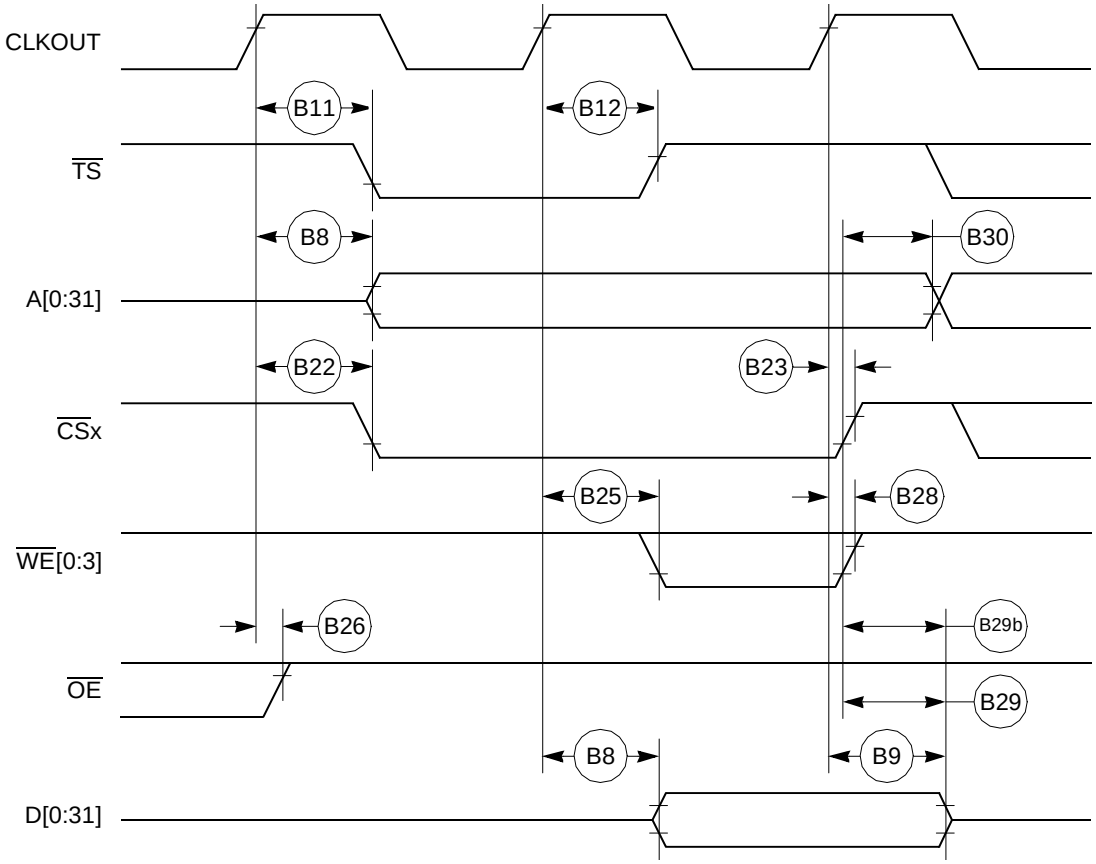


Figure 16. External Bus Write Timing (GPCM Controlled—TRLX = 0, CSNT = 0)

Table 12 shows the PCMCIA timing for the MPC875/MPC870.

Table 12. PCMCIA Timing

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
P44	A(0:31), $\overline{\text{REG}}$ valid to PCMCIA strobe asserted[1] (MIN = 0.75 × B1 – 2.00)	20.70	—	16.70	—	9.40	—	7.40	—	ns
P45	A(0:31), $\overline{\text{REG}}$ valid to ALE negation[1] (MIN = 1.00 × B1 – 2.00)	28.30	—	23.00	—	13.20	—	10.50	—	ns
P46	CLKOUT to $\overline{\text{REG}}$ valid (MAX = 0.25 × B1 + 8.00)	7.60	15.60	6.30	14.30	3.80	11.80	3.13	11.13	ns
P47	CLKOUT to $\overline{\text{REG}}$ invalid (MIN = 0.25 × B1 + 1.00)	8.60	—	7.30	—	4.80	—	4.125	—	ns
P48	CLKOUT to $\overline{\text{CE1}}$, $\overline{\text{CE2}}$ asserted (MAX = 0.25 × B1 + 8.00)	7.60	15.60	6.30	14.30	3.80	11.80	3.13	11.13	ns
P49	CLKOUT to $\overline{\text{CE1}}$, $\overline{\text{CE2}}$ negated (MAX = 0.25 × B1 + 8.00)	7.60	15.60	6.30	14.30	3.80	11.80	3.13	11.13	ns
P50	CLKOUT to $\overline{\text{PCOE}}$, $\overline{\text{IORD}}$, $\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ assert time (MAX = 0.00 × B1 + 11.00)	—	11.00	—	11.00	—	11.00	—	11.00	ns
P51	CLKOUT to $\overline{\text{PCOE}}$, $\overline{\text{IORD}}$, $\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ negate time (MAX = 0.00 × B1 + 11.00)	2.00	11.00	2.00	11.00	2.00	11.00	2.00	11.00	ns
P52	CLKOUT to ALE assert time (MAX = 0.25 × B1 + 6.30)	7.60	13.80	6.30	12.50	3.80	10.00	3.13	9.40	ns
P53	CLKOUT to ALE negate time (MAX = 0.25 × B1 + 8.00)	—	15.60	—	14.30	—	11.80	—	11.13	ns
P54	$\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ negated to D(0:31) invalid[1] (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	1.80	—	1.125	—	ns
P55	$\overline{\text{WAITA}}$ and $\overline{\text{WAITB}}$ valid to CLKOUT rising edge[1] (MIN = 0.00 × B1 + 8.00)	8.00	—	8.00	—	8.00	—	8.00	—	ns
P56	CLKOUT rising edge to $\overline{\text{WAITA}}$ and $\overline{\text{WAITB}}$ invalid[1] (MIN = 0.00 × B1 + 2.00)	2.00	—	2.00	—	2.00	—	2.00	—	ns

1 PSST = 1. Otherwise add PSST times cycle time.
PSHT = 0. Otherwise add PSHT times cycle time.
These synchronous timings define when the $\overline{\text{WAITA}}$ signals are detected in order to freeze (or relieve) the PCMCIA current cycle. The $\overline{\text{WAITA}}$ assertion will be effective only if it is detected 2 cycles before the PSL timer expiration. See Chapter 16, “PCMCIA Interface,” in the *MPC885 PowerQUICC™ Family Reference Manual*.

Table 13 shows the PCMCIA port timing for the MPC875/MPC870.

Table 13. PCMCIA Port Timing

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
P57	CLKOUT to OPx valid (MAX = 0.00 × B1 + 19.00)	—	19.00	—	19.00	—	19.00	—	19.00	ns
P58	$\overline{\text{HRESET}}$ negated to OPx drive[1] (MIN = 0.75 × B1 + 3.00)	25.70	—	21.70	—	14.40	—	12.40	—	ns
P59	IP_Xx valid to CLKOUT rising edge (MIN = 0.00 × B1 + 5.00)	5.00	—	5.00	—	5.00	—	5.00	—	ns
P60	CLKOUT rising edge to IP_Xx invalid (MIN = 0.00 × B1 + 1.00)	1.00	—	1.00	—	1.00	—	1.00	—	ns

1 OP2 and OP3 only.

Figure 30 provides the PCMCIA output port timing for the MPC875/MPC870.

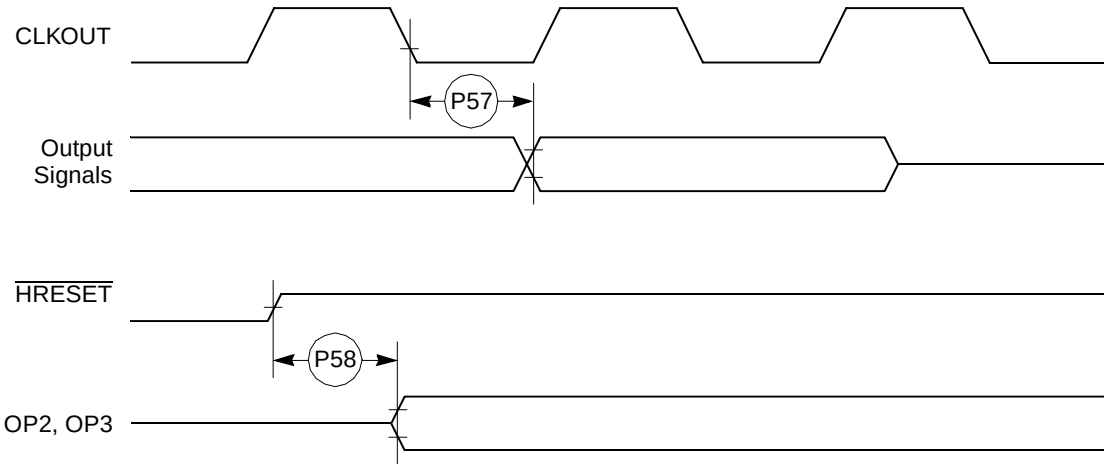


Figure 30. PCMCIA Output Port Timing

Figure 31 provides the PCMCIA input port timing for the MPC875/MPC870.

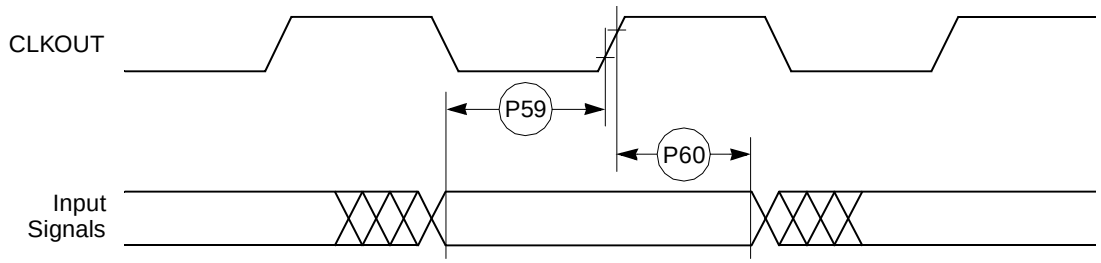


Figure 31. PCMCIA Input Port Timing

Table 14 shows the debug port timing for the MPC875/MPC870.

Table 14. Debug Port Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
D61	DSCK cycle time	$3 \times T_{CLOCKOUT}$		—
D62	DSCK clock pulse width	$1.25 \times T_{CLOCKOUT}$		—
D63	DSCK rise and fall times	0.00	3.00	ns
D64	DSDI input data setup time	8.00		ns
D65	DSDI data hold time	5.00		ns
D66	DSCK low to DSDO data valid	0.00	15.00	ns
D67	DSCK low to DSDO invalid	0.00	2.00	ns

Figure 32 provides the input timing for the debug port clock.

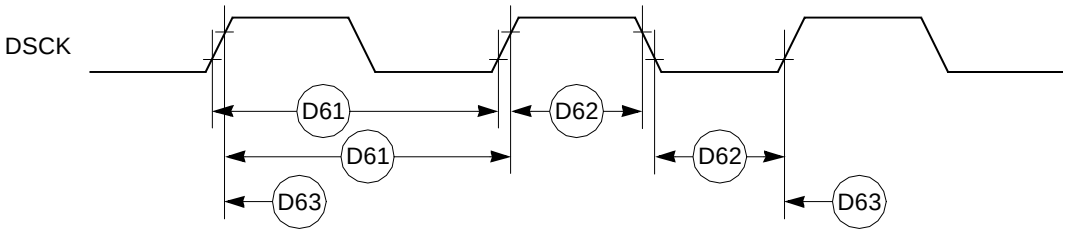


Figure 32. Debug Port Clock Input Timing

Figure 33 provides the timing for the debug port.

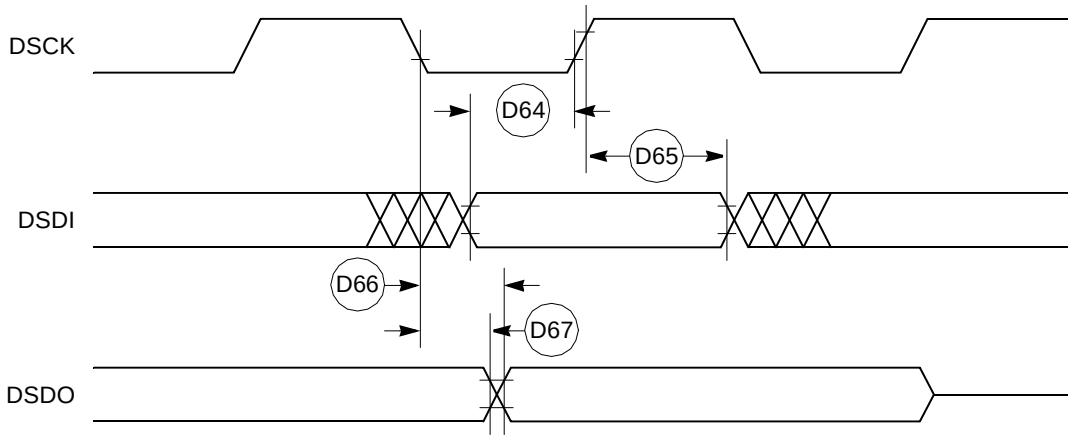


Figure 33. Debug Port Timings

Figure 34 shows the reset timing for the data bus configuration.

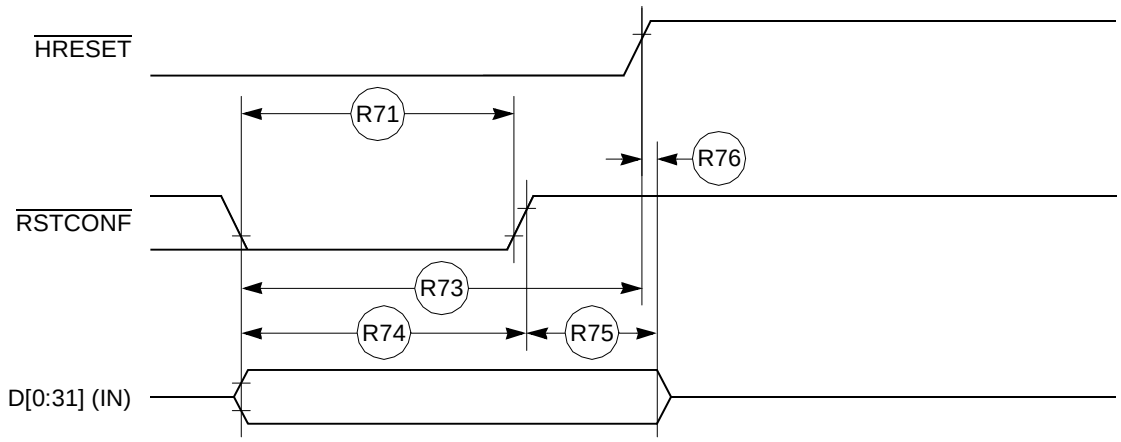


Figure 34. Reset Timing—Configuration from Data Bus

Figure 35 provides the reset timing for the data bus weak drive during configuration.

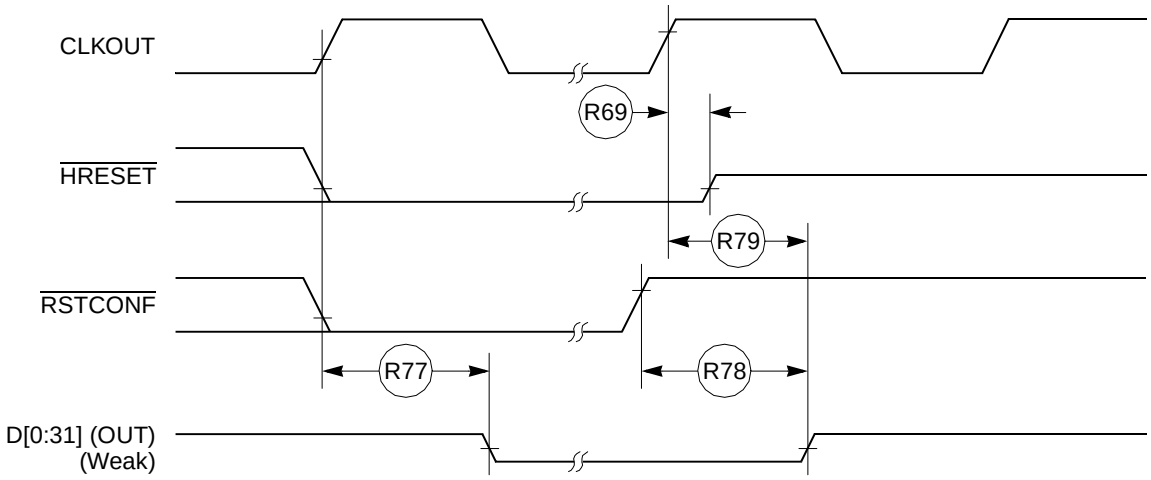


Figure 35. Reset Timing—Data Bus Weak Drive During Configuration

Figure 36 provides the reset timing for the debug port configuration.

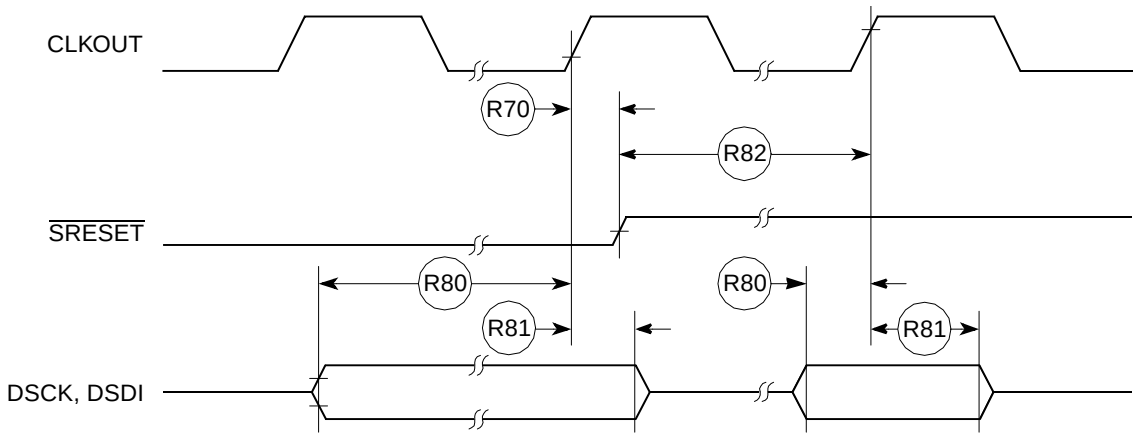


Figure 36. Reset Timing—Debug Port Configuration

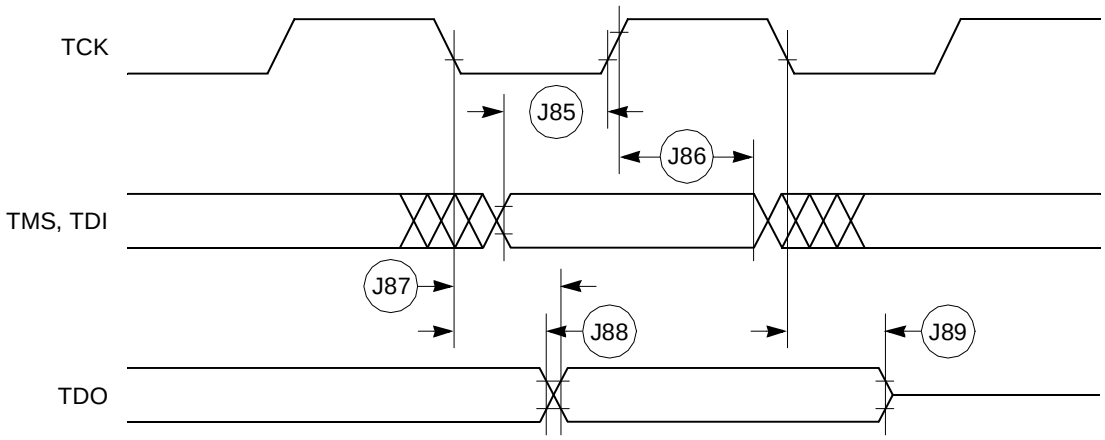


Figure 38. JTAG Test Access Port Timing Diagram

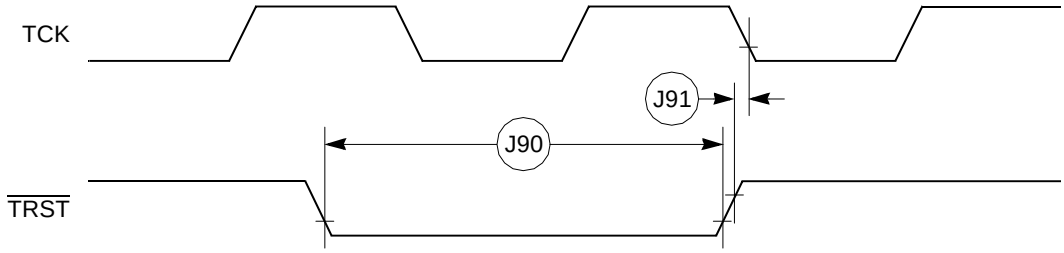


Figure 39. JTAG $\overline{\text{TRST}}$ Timing Diagram

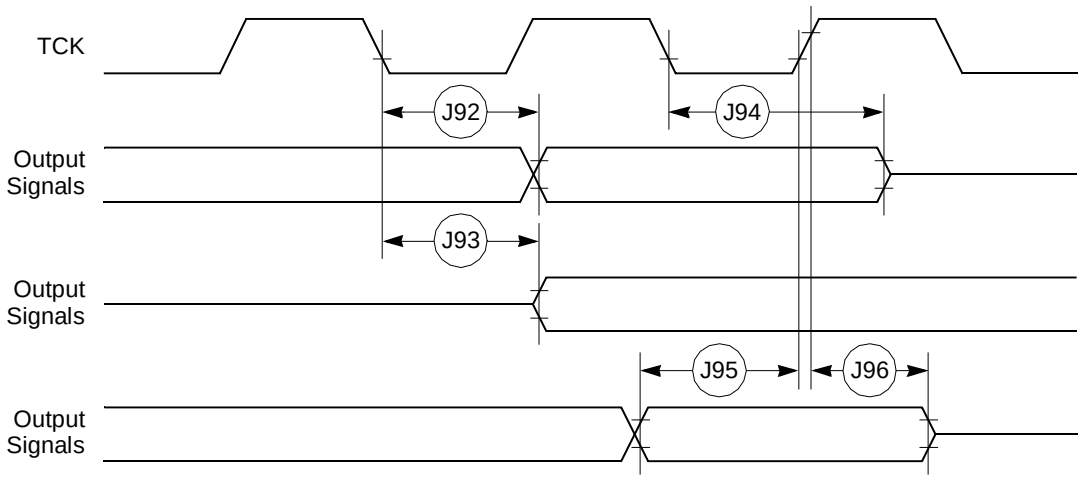


Figure 40. Boundary Scan (JTAG) Timing Diagram

13 CPM Electrical Characteristics

This section provides the AC and DC electrical specifications for the communications processor module (CPM) of the MPC875/MPC870.

13.1 Port C Interrupt AC Electrical Specifications

Table 17 provides the timings for Port C interrupts.

Table 17. Port C Interrupt Timing

Num	Characteristic	33.34 MHz		Unit
		Min	Max	
35	Port C interrupt pulse width low (edge-triggered mode)	55	—	ns
36	Port C interrupt minimum time between active edges	55	—	ns

Figure 41 shows the Port C interrupt detection timing.

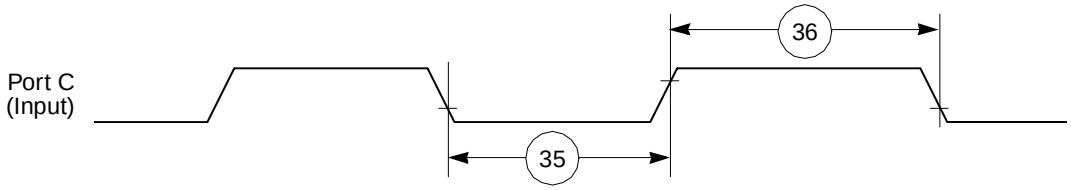


Figure 41. Port C Interrupt Detection Timing

13.2 IDMA Controller AC Electrical Specifications

Table 18 provides the IDMA controller timings as shown in Figure 42 through Figure 45.

Table 18. IDMA Controller Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
40	$\overline{\text{DREQ}}$ setup time to clock high	7	—	ns
41	$\overline{\text{DREQ}}$ hold time from clock high[1]	TBD	—	ns
42	$\overline{\text{SDACK}}$ assertion delay from clock high	—	12	ns
43	$\overline{\text{SDACK}}$ negation delay from clock low	—	12	ns
44	$\overline{\text{SDACK}}$ negation delay from $\overline{\text{TA}}$ low	—	20	ns
45	$\overline{\text{SDACK}}$ negation delay from clock high	—	15	ns
46	$\overline{\text{TA}}$ assertion to rising edge of the clock setup time (applies to external $\overline{\text{TA}}$)	7	—	ns

1 Applies to high-to-low mode (EDM = 1).

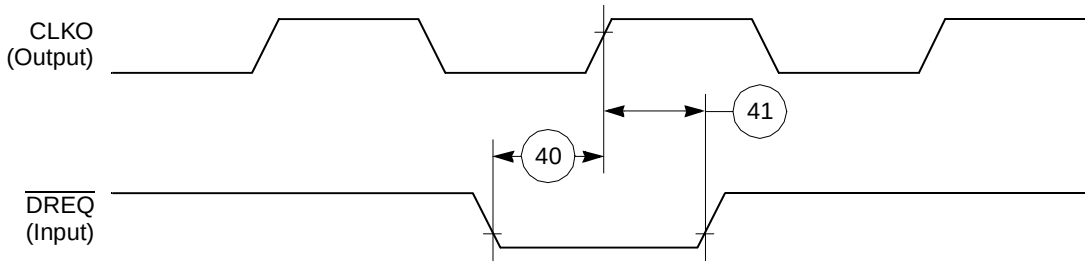


Figure 42. IDMA External Requests Timing Diagram

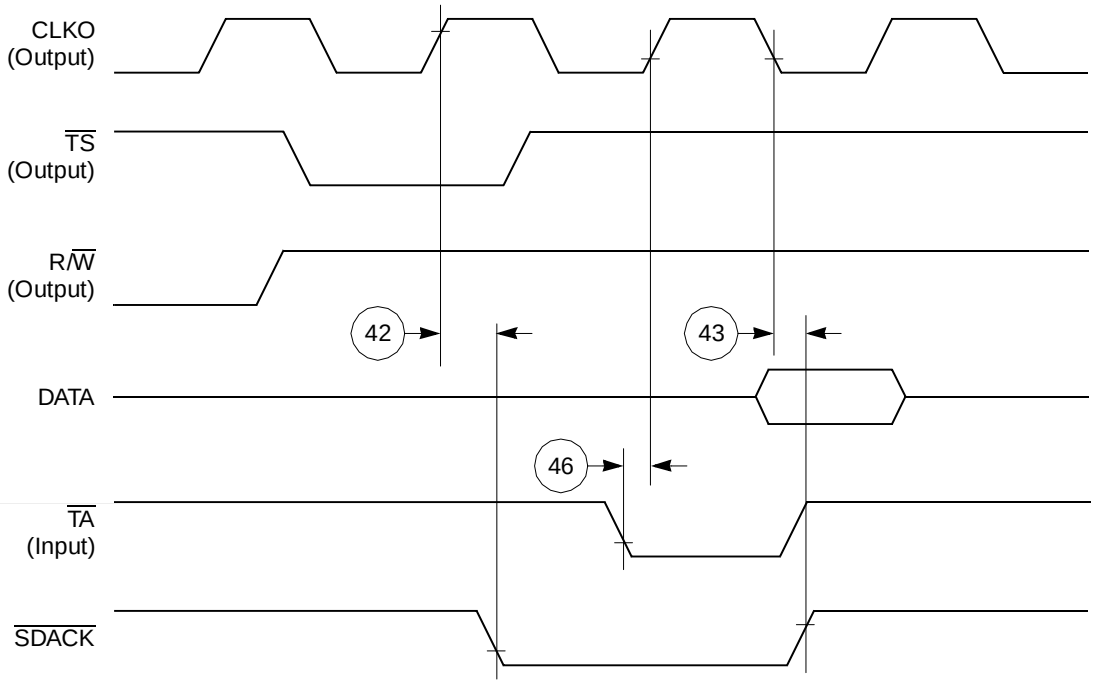


Figure 43. SDACK Timing Diagram—Peripheral Write, Externally-Generated TA

Table 21. SI Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
83a	L1RCLKB, L1TCLKB width high (DSC = 1)[3]	P + 10	—	ns
84	L1CLKB edge to L1CLKOB valid (DSC = 1)	—	30.00	ns
85	$\overline{\text{L1RQB}}$ valid before falling edge of L1TSYNCB[4]	1.00	—	L1TCLK
86	L1GRB setup time[2]	42.00	—	ns
87	L1GRB hold time	42.00	—	ns
88	L1CLKB edge to L1SYNCB valid (FSD = 00) CNT = 0000, BYT = 0, DSC = 0)	—	0.00	ns

1 The ratio SYNCCLK/L1RCLKB must be greater than 2.5/1.
2 These specs are valid for IDL mode only.
3 Where P = 1/CLKOUT. Thus, for a 25-MHz CLKO1 rate, P = 40 ns.
4 These strobes and TxD on the first bit of the frame become valid after the L1CLKB edge or L1SYNCB, whichever comes later.

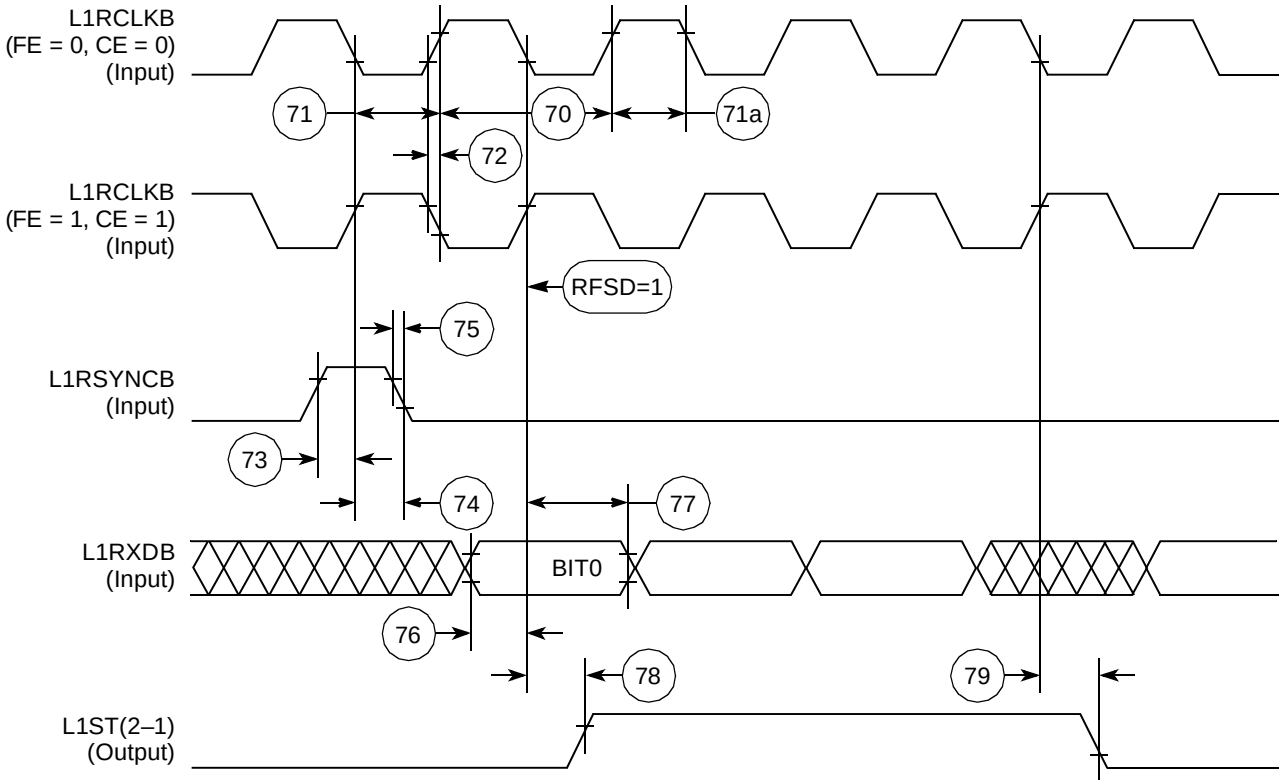


Figure 48. SI Receive Timing Diagram with Normal Clocking (DSC = 0)

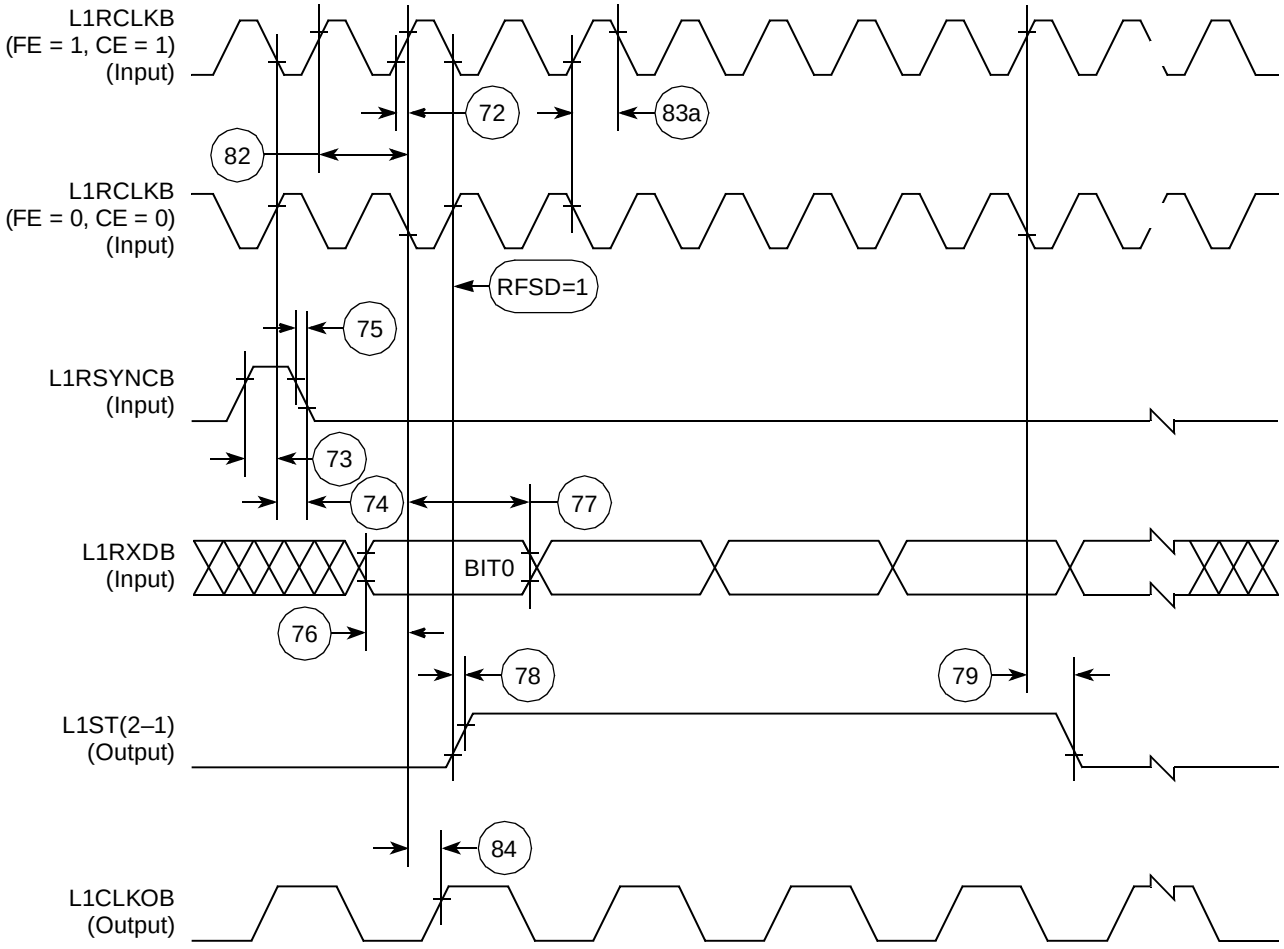


Figure 49. SI Receive Timing with Double-Speed Clocking (DSC = 1)

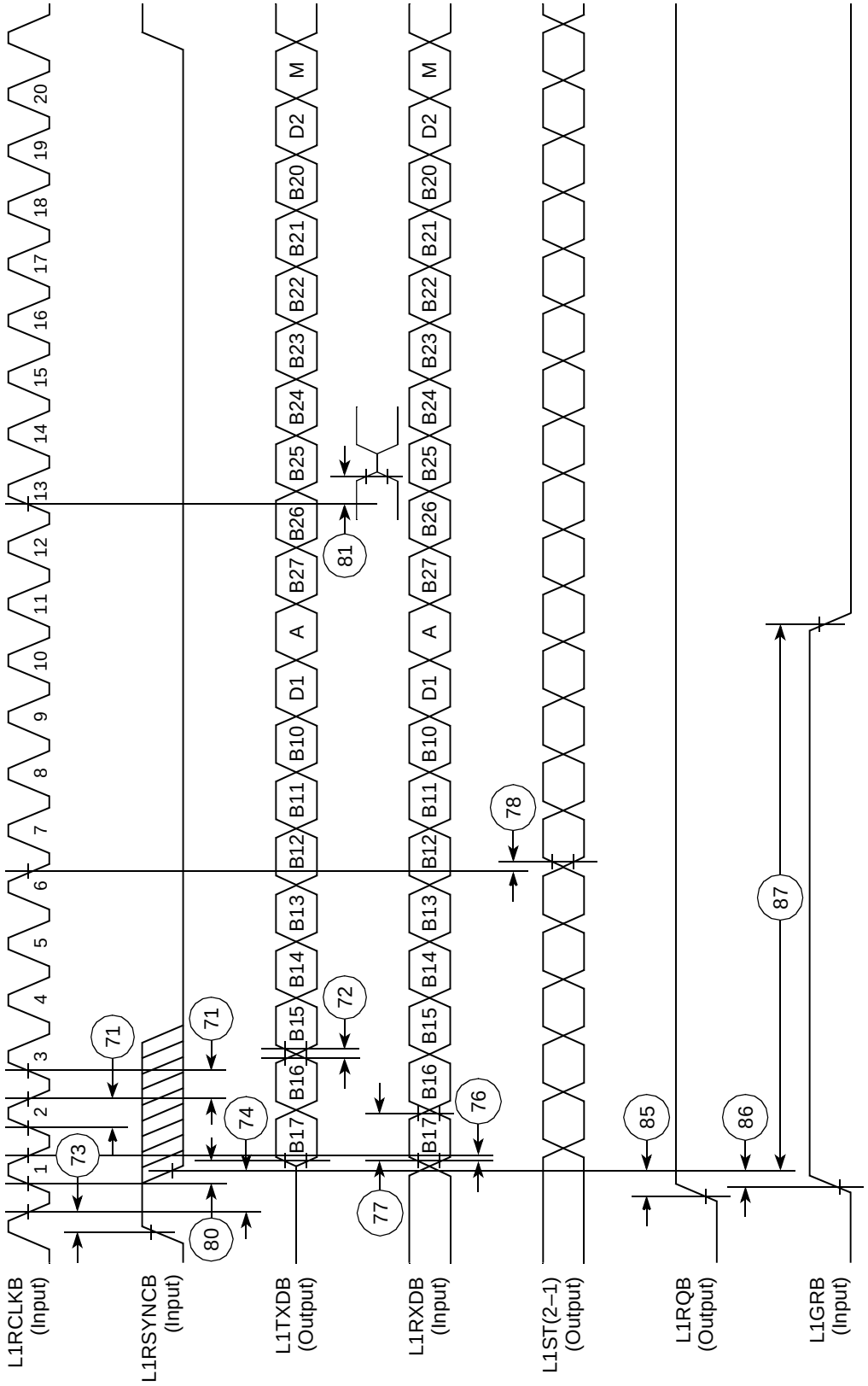


Figure 52. IDL Timing

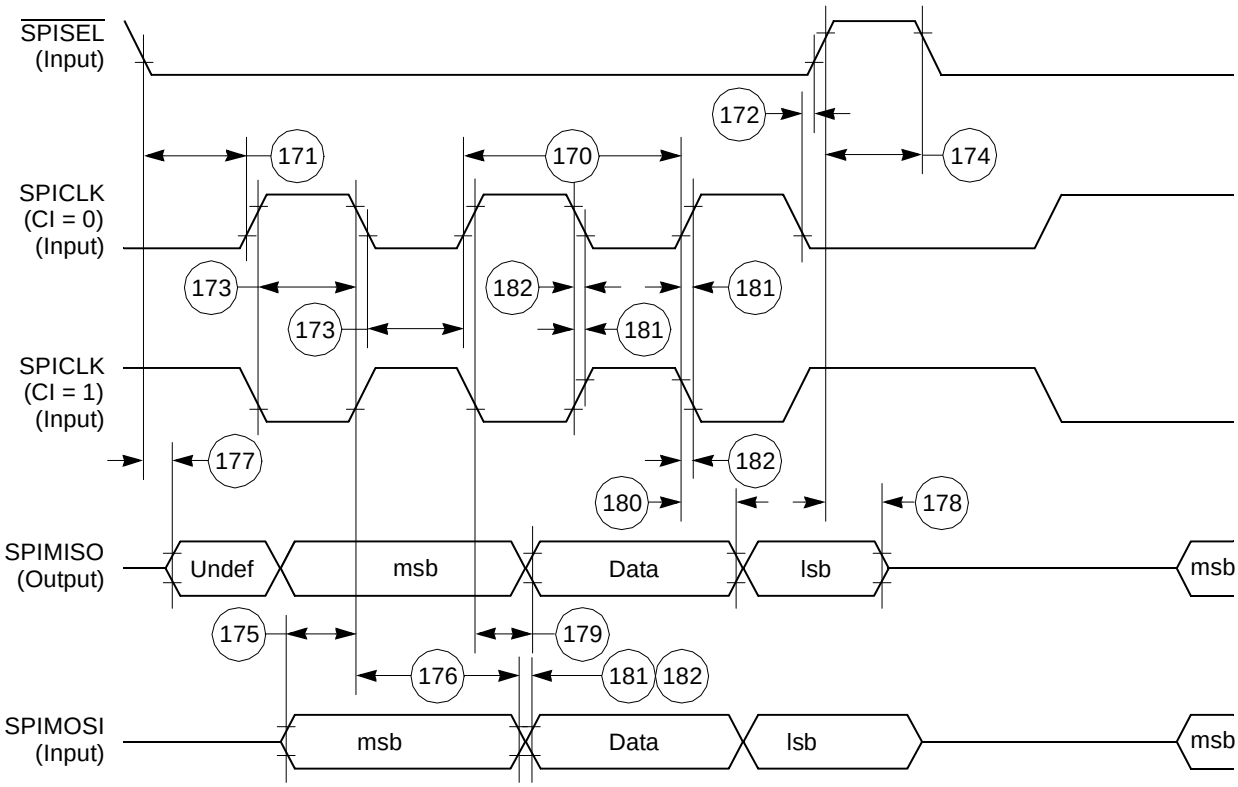


Figure 63. SPI Slave (CP = 1) Timing Diagram

13.11 I²C AC Electrical Specifications

Table 28 provides the I²C (SCL < 100 kHz) timings.

Table 28. I²C Timing (SCL < 100 kHz)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
200	SCL clock frequency (slave)	0	100	kHz
200	SCL clock frequency (master)[1]	1.5	100	kHz
202	Bus free time between transmissions	4.7	—	µs
203	Low period of SCL	4.7	—	µs
204	High period of SCL	4.0	—	µs
205	Start condition setup time	4.7	—	µs
206	Start condition hold time	4.0	—	µs
207	Data hold time	0	—	µs
208	Data setup time	250	—	ns
209	SDL/SCL rise time	—	1	µs

14 USB Electrical Characteristics

This section provides the AC timings for the USB interface.

14.1 USB Interface AC Timing Specifications

The USB Port uses the transmit clock on SCC1. Table 30 lists the USB interface timings.

Table 30. USB Interface AC Timing Specifications

Name	Characteristic	All Frequencies		Unit
		Min	Max	
US1	USBCLK frequency of operation[1] Low speed Full speed	 6 48		MHz
US4	USBCLK duty cycle (measured at 1.5 V)	45	55	%

1 USBCLK accuracy should be ±500 ppm or better. USBCLK may be stopped to conserve power.

15 FEC Electrical Characteristics

This section provides the AC electrical specifications for the Fast Ethernet controller (FEC). Note that the timing specifications for the MII signals are independent of system clock frequency (part speed designation). Also, MII signals use TTL signal levels compatible with devices operating at either 5.0 or 3.3 V.

15.1 MII and Reduced MII Receive Signal Timing

The receiver functions correctly up to a MII_RX_CLK maximum frequency of 25 MHz + 1%. The reduced MII (RMII) receiver functions correctly up to a RMII_REFCLK maximum frequency of 50 MHz + 1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_RX_CLK frequency – 1%.

Table 31 provides information on the MII receive signal timing.

Table 31. MII Receive Signal Timing

Num	Characteristic	Min	Max	Unit
M1	MII_RXD[3:0], MII_RX_DV, MII_RX_ER to MII_RX_CLK setup	5	—	ns
M2	MII_RX_CLK to MII_RXD[3:0], MII_RX_DV, MII_RX_ER hold	5	—	ns
M3	MII_RX_CLK pulse width high	35%	65%	MII_RX_CLK period
M4	MII_RX_CLK pulse width low	35%	65%	MII_RX_CLK period
M1_RMII	RMII_RXD[1:0], RMII_CRS_DV, RMII_RX_ERR to RMII_REFCLK setup	4	—	ns
M2_RMII	RMII_REFCLK to RMII_RXD[1:0], RMII_CRS_DV, RMII_RX_ERR hold	2	—	ns

16.1 Pin Assignments

Figure 69 shows the JEDEC pinout of the PBGA package as viewed from the top surface. For additional information, see the *MPC885 PowerQUICC Family User's Manual*.

NOTE

The pin numbering starts with B2 in order to conform to the JEDEC standard for 23-mm body size using a 16 × 16 array.

NOTE: This is the top view of the device.

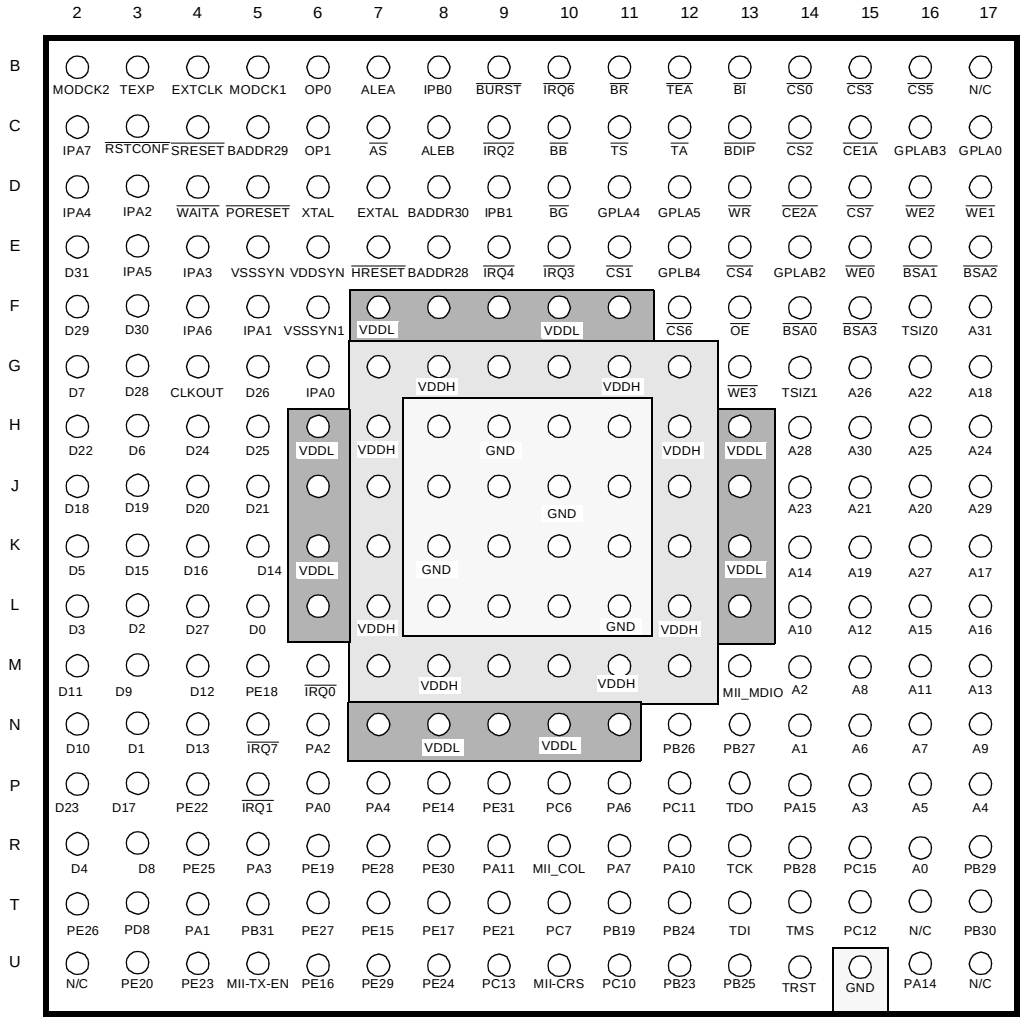
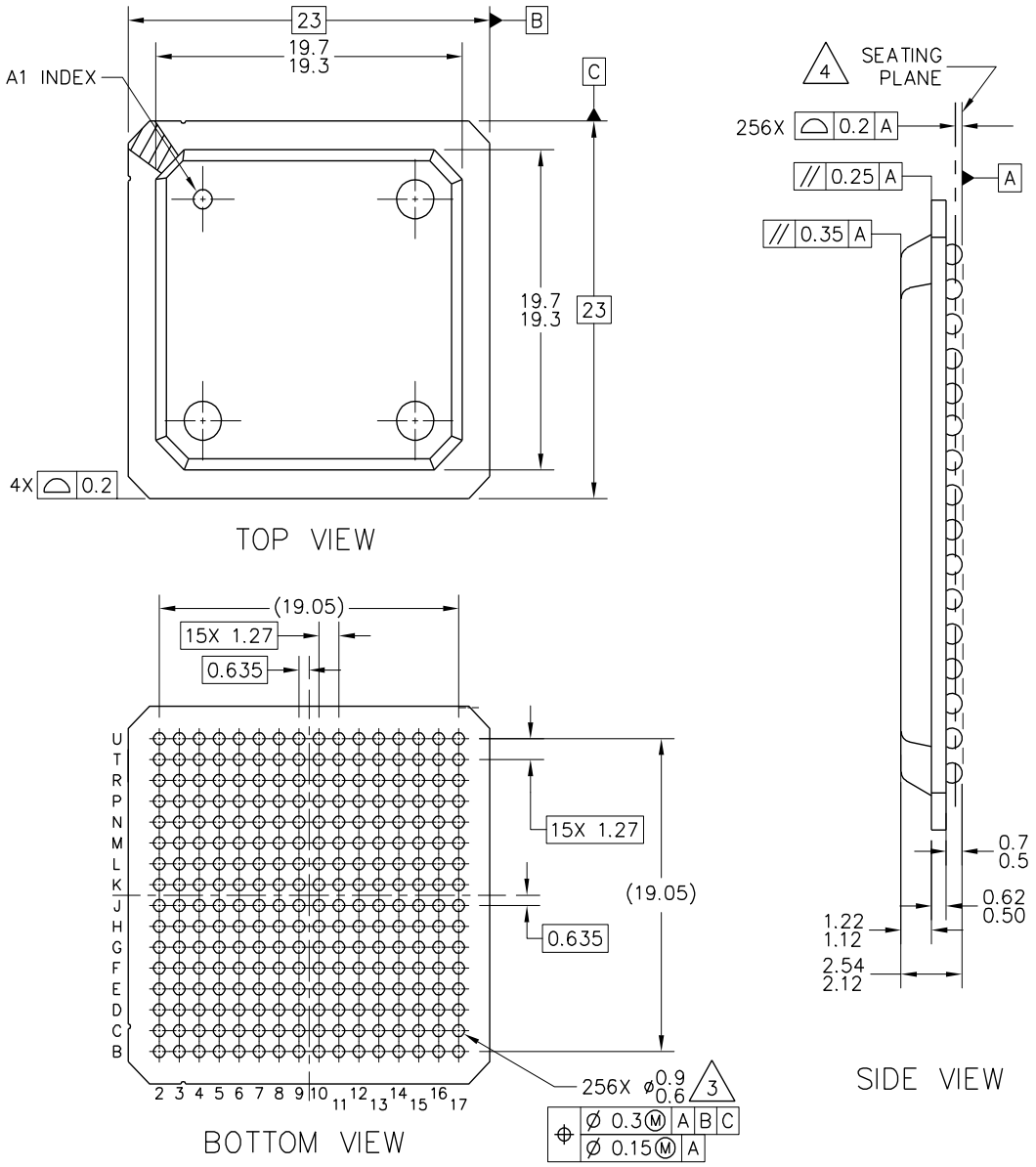


Figure 69. Pinout of the PBGA Package—JEDEC Standard

16.2 Mechanical Dimensions of the PBGA Package

Figure 70 shows the mechanical dimensions of the PBGA package.



NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M—1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

Note: Solder sphere composition is 95.5%Sn 45%Ag 0.5%Cu for MPC875/MPC870VRXXX.
Solder sphere composition is 62%Sn 36%Pb 2%Ag for MPC875/MPC870ZTXXX.

Figure 70. Mechanical Dimensions and Bottom Surface Nomenclature of the PBGA Package