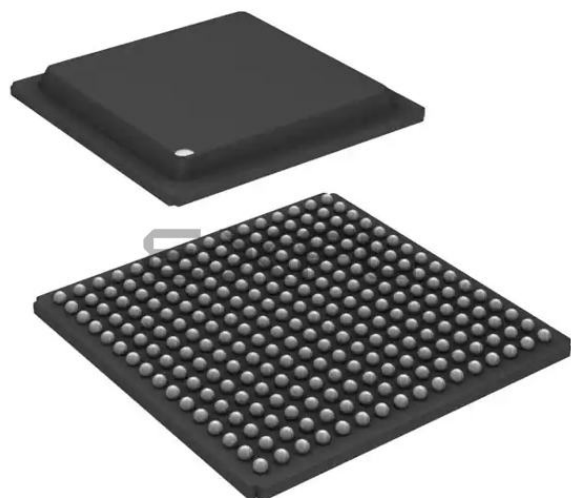




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Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	66MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (2)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 100°C (TA)
Security Features	-
Package / Case	256-BBGA
Supplier Device Package	256-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc870czt66

Table 10. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B2	CLKOUT pulse width low (MIN = $0.4 \times B1$, MAX = $0.6 \times B1$)	12.1	18.2	10.0	15.0	6.1	9.1	5.0	7.5	ns
B3	CLKOUT pulse width high (MIN = $0.4 \times B1$, MAX = $0.6 \times B1$)	12.1	18.2	10.0	15.0	6.1	9.1	5.0	7.5	ns
B4	CLKOUT rise time	—	4.00	—	4.00	—	4.00	—	4.00	ns
B5	CLKOUT fall time	—	4.00	—	4.00	—	4.00	—	4.00	ns
B7	CLKOUT to A(0:31), BADDR(28:30), RD/WR, BURST, D(0:31) output hold (MIN = $0.25 \times B1$)	7.60	—	6.30	—	3.80	—	3.13	—	ns
B7a	CLKOUT to TSIZ(0:1), REG, RSV, BDIP, PTR output hold (MIN = $0.25 \times B1$)	7.60	—	6.30	—	3.80	—	3.13	—	ns
B7b	CLKOUT to BR, BG, FRZ, VFLS(0:1), VF(0:2) IWP(0:2), LWP(0:1), STS output hold (MIN = $0.25 \times B1$)	7.60	—	6.30	—	3.80	—	3.13	—	ns
B8	CLKOUT to A(0:31), BADDR(28:30), RD/WR, BURST, D(0:31) valid (MAX = $0.25 \times B1 + 6.3$)	—	13.80	—	12.50	—	10.00	—	9.43	ns
B8a	CLKOUT to TSIZ(0:1), REG, RSV, BDIP, PTR valid (MAX = $0.25 \times B1 + 6.3$)	—	13.80	—	12.50	—	10.00	—	9.43	ns
B8b	CLKOUT to BR, BG, VFLS(0:1), VF(0:2), IWP(0:2), FRZ, LWP(0:1), STS valid ² (MAX = $0.25 \times B1 + 6.3$)	—	13.80	—	12.50	—	10.00	—	9.43	ns
B9	CLKOUT to A(0:31), BADDR(28:30), RD/WR, BURST, D(0:31), TSIZ(0:1), REG, RSV, PTR High-Z (MAX = $0.25 \times B1 + 6.3$)	7.60	13.80	6.30	12.50	3.80	10.00	3.13	9.43	ns
B11	CLKOUT to TS, BB assertion (MAX = $0.25 \times B1 + 6.0$)	7.60	13.60	6.30	12.30	3.80	9.80	3.13	9.13	ns
B11a	CLKOUT to TA, BI assertion (when driven by the memory controller or PCMCIA interface) (MAX = $0.00 \times B1 + 9.30^1$)	2.50	9.30	2.50	9.30	2.50	9.80	2.5	9.3	ns
B12	CLKOUT to TS, BB negation (MAX = $0.25 \times B1 + 4.8$)	7.60	12.30	6.30	11.00	3.80	8.50	3.13	7.92	ns
B12a	CLKOUT to TA, BI negation (when driven by the memory controller or PCMCIA interface) (MAX = $0.00 \times B1 + 9.00$)	2.50	9.00	2.50	9.00	2.50	9.00	2.5	9.00	ns
B13	CLKOUT to TS, BB High-Z (MIN = $0.25 \times B1$)	7.60	21.60	6.30	20.30	3.80	14.00	3.13	12.93	ns
B13a	CLKOUT to TA, BI High-Z (when driven by the memory controller or PCMCIA interface) (MIN = $0.00 \times B1 + 2.5$)	2.50	15.00	2.50	15.00	2.50	15.00	2.5	15.00	ns
B14	CLKOUT to TEA assertion (MAX = $0.00 \times B1 + 9.00$)	2.50	9.00	2.50	9.00	2.50	9.00	2.50	9.00	ns

Table 10. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B15	CLKOUT to $\overline{\text{TEA}}$ High-Z (MIN = $0.00 \times B1 + 2.50$)	2.50	15.00	2.50	15.00	2.50	15.00	2.50	15.00	ns
B16	$\overline{\text{TA}}$, $\overline{\text{BI}}$ valid to CLKOUT (setup time) (MIN = $0.00 \times B1 + 6.00$)	6.00	—	6.00	—	6.00	—	6	—	ns
B16a	$\overline{\text{TEA}}$, $\overline{\text{KR}}$, $\overline{\text{RETRY}}$, $\overline{\text{CR}}$ valid to CLKOUT (setup time) (MIN = $0.00 \times B1 + 4.5$)	4.50	—	4.50	—	4.50	—	4.50	—	ns
B16b	$\overline{\text{BB}}$, $\overline{\text{BG}}$, $\overline{\text{BR}}$, valid to CLKOUT (setup time) ² (4MIN = $0.00 \times B1 + 0.00$)	4.00	—	4.00	—	4.00	—	4.00	—	ns
B17	CLKOUT to $\overline{\text{TA}}$, $\overline{\text{TEA}}$, $\overline{\text{BI}}$, $\overline{\text{BB}}$, $\overline{\text{BG}}$, $\overline{\text{BR}}$ valid (hold time) (MIN = $0.00 \times B1 + 1.00^3$)	1.00	—	1.00	—	2.00	—	2.00	—	ns
B17a	CLKOUT to $\overline{\text{KR}}$, $\overline{\text{RETRY}}$, $\overline{\text{CR}}$ valid (hold time) (MIN = $0.00 \times B1 + 2.00$)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B18	D(0:31) valid to CLKOUT rising edge (setup time) ⁴ (MIN = $0.00 \times B1 + 6.00$)	6.00	—	6.00	—	6.00	—	6.00	—	ns
B19	CLKOUT rising edge to D(0:31) valid (hold time) ⁴ (MIN = $0.00 \times B1 + 1.00^5$)	1.00	—	1.00	—	2.00	—	2.00	—	ns
B20	D(0:31) valid to CLKOUT falling edge (setup time) ⁶ (MIN = $0.00 \times B1 + 4.00$)	4.00	—	4.00	—	4.00	—	4.00	—	ns
B21	CLKOUT falling edge to D(0:31) valid (hold time) ⁶ (MIN = $0.00 \times B1 + 2.00$)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B22	CLKOUT rising edge to $\overline{\text{CS}}$ asserted GPCM ACS = 00 (MAX = $0.25 \times B1 + 6.3$)	7.60	13.80	6.30	12.50	3.80	10.00	3.13	9.43	ns
B22a	CLKOUT falling edge to $\overline{\text{CS}}$ asserted GPCM ACS = 10, TRLX = 0 (MAX = $0.00 \times B1 + 8.00$)	—	8.00	—	8.00	—	8.00	—	8.00	ns
B22b	CLKOUT falling edge to $\overline{\text{CS}}$ asserted GPCM ACS = 11, TRLX = 0, EBDF = 0 (MAX = $0.25 \times B1 + 6.3$)	7.60	13.80	6.30	12.50	3.80	10.00	3.13	9.43	ns
B22c	CLKOUT falling edge to $\overline{\text{CS}}$ asserted GPCM ACS = 11, TRLX = 0, EBDF = 1 (MAX = $0.375 \times B1 + 6.6$)	10.90	18.00	10.90	16.00	5.20	12.30	4.69	10.93	ns
B23	CLKOUT rising edge to $\overline{\text{CS}}$ negated GPCM read access, GPCM write access ACS = 00, TRLX = 0 and CSNT = 0 (MAX = $0.00 \times B1 + 8.00$)	2.00	8.00	2.00	8.00	2.00	8.00	2.00	8.00	ns
B24	A(0:31) and BADDR(28:30) to $\overline{\text{CS}}$ asserted GPCM ACS = 10, TRLX = 0 (MIN = $0.25 \times B1 - 2.00$)	5.60	—	4.30	—	1.80	—	1.13	—	ns
B24a	A(0:31) and BADDR(28:30) to $\overline{\text{CS}}$ asserted GPCM ACS = 11, TRLX = 0 (MIN = $0.50 \times B1 - 2.00$)	13.20	—	10.50	—	5.60	—	4.25	—	ns

Table 10. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B25	CLKOUT rising edge to $\overline{OE}$, $\overline{WE}(0:3)/BS_B[0:3]$ asserted (MAX = $0.00 \times B1 + 9.00$)	—	9.00		9.00		9.00	—	9.00	ns
B26	CLKOUT rising edge to $\overline{OE}$ negated (MAX = $0.00 \times B1 + 9.00$)	2.00	9.00	2.00	9.00	2.00	9.00	2.00	9.00	ns
B27	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 1 (MIN = $1.25 \times B1 - 2.00$)	35.90	—	29.30	—	16.90	—	13.60	—	ns
B27a	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 1 (MIN = $1.50 \times B1 - 2.00$)	43.50	—	35.50	—	20.70	—	16.75	—	ns
B28	CLKOUT rising edge to $\overline{WE}(0:3)/BS_B[0:3]$ negated GPCM write access CSNT = 0 (MAX = $0.00 \times B1 + 9.00$)	—	9.00	—	9.00	—	9.00	—	9.00	ns
B28a	CLKOUT falling edge to $\overline{WE}(0:3)/BS_B[0:3]$ negated GPCM write access TRLX = 0, CSNT = 1, EBDF = 0 (MAX = $0.25 \times B1 + 6.80$)	7.60	14.30	6.30	13.00	3.80	10.50	3.13	9.93	ns
B28b	CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0, CSNT = 1 ACS = 10 or ACS = 11, EBDF = 0 (MAX = $0.25 \times B1 + 6.80$)	—	14.30	—	13.00	—	10.50	—	9.93	ns
B28c	CLKOUT falling edge to $\overline{WE}(0:3)/BS_B[0:3]$ negated GPCM write access TRLX = 0, CSNT = 1 write access TRLX = 0, CSNT = 1, EBDF = 1 (MAX = $0.375 \times B1 + 6.6$)	10.90	18.00	10.90	18.00	5.20	12.30	4.69	11.29	ns
B28d	CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1 (MAX = $0.375 \times B1 + 6.6$)	—	18.00	—	18.00	—	12.30	—	11.30	ns
B29	$\overline{WE}(0:3)/BS_B[0:3]$ negated to D(0:31) High-Z GPCM write access, CSNT = 0, EBDF = 0 (MIN = $0.25 \times B1 - 2.00$)	5.60	—	4.30	—	1.80	—	1.13	—	ns
B29a	$\overline{WE}(0:3)/BS_B[0:3]$ negated to D(0:31) High-Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 0 (MIN = $0.50 \times B1 - 2.00$)	13.20	—	10.50	—	5.60	—	4.25	—	ns
B29b	$\overline{CS}$ negated to D(0:31) High-Z GPCM write access, ACS = 00, TRLX = 0 and CSNT = 0 (MIN = $0.25 \times B1 - 2.00$)	5.60	—	4.30	—	1.80	—	1.13	—	ns
B29c	$\overline{CS}$ negated to D(0:31) High-Z GPCM write access, TRLX = 0, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 0 (MIN = $0.50 \times B1 - 2.00$)	13.20	—	10.50	—	5.60	—	4.25	—	ns

Table 10. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B29d	$\overline{WE}(0:3)/BS_B[0:3]$ negated to D(0:31) High-Z GPCM write access, $TRLX = 1$, $CSNT = 1$, $EBDF = 0$ (MIN = $1.50 \times B1 - 2.00$)	43.50	—	35.50	—	20.70	—	16.75	—	ns
B29e	$\overline{CS}$ negated to D(0:31) High-Z GPCM write access, $TRLX = 1$, $CSNT = 1$, $ACS = 10$ or $ACS = 11$, $EBDF = 0$ (MIN = $1.50 \times B1 - 2.00$)	43.50	—	35.50	—	20.70	—	16.75	—	ns
B29f	$\overline{WE}(0:3)/BS_B[0:3]$ negated to D(0:31) High-Z GPCM write access, $TRLX = 0$, $CSNT = 1$, $EBDF = 1$ (MIN = $0.375 \times B1 - 6.30$) ⁷	5.00	—	3.00	—	0.00	—	0.00	—	ns
B29g	$\overline{CS}$ negated to D(0:31) High-Z GPCM write access, $TRLX = 0$, $CSNT = 1$, $ACS = 10$ or $ACS = 11$, $EBDF = 1$ (MIN = $0.375 \times B1 - 6.30$) ⁷	5.00	—	3.00	—	0.00	—	0.00	—	ns
B29h	$\overline{WE}(0:3)/BS_B[0:3]$ negated to D(0:31) High-Z GPCM write access, $TRLX = 1$, $CSNT = 1$, $EBDF = 1$ (MIN = $0.375 \times B1 - 3.30$)	38.40	—	31.10	—	17.50	—	13.85	—	ns
B29i	$\overline{CS}$ negated to D(0:31) (0:3) High-Z GPCM write access, $TRLX = 1$, $CSNT = 1$, $ACS = 10$ or $ACS = 11$, $EBDF = 1$ (MIN = $0.375 \times B1 - 3.30$)	38.40	—	31.10	—	17.50	—	13.85	—	ns
B30	$\overline{CS}$, $\overline{WE}(0:3)/BS_B[0:3]$ negated to A(0:31), $BADDR(28:30)$ invalid GPCM write access ⁸ (MIN = $0.25 \times B1 - 2.00$)	5.60	—	4.30	—	1.80	—	1.13	—	ns
B30a	$\overline{WE}(0:3)/BS_B[0:3]$ negated to A(0:31), $BADDR(28:30)$ invalid GPCM, write access, $TRLX = 0$, $CSNT = 1$, $\overline{CS}$ negated to A(0:31), invalid GPCM write access $TRLX = 0$, $CSNT = 1$, $ACS = 10$ or $ACS = 11$, $EBDF = 0$ (MIN = $0.50 \times B1 - 2.00$)	13.20	—	10.50	—	5.60	—	4.25	—	ns
B30b	$\overline{WE}(0:3)/BS_B[0:3]$ negated to A(0:31), invalid GPCM $BADDR(28:30)$, invalid GPCM write access, $TRLX = 1$, $CSNT = 1$, $\overline{CS}$ negated to A(0:31), invalid GPCM write access $TRLX = 1$, $CSNT = 1$, $ACS = 10$ or $ACS = 11$, $EBDF = 0$ (MIN = $1.50 \times B1 - 2.00$)	43.50	—	35.50	—	20.70	—	16.75	—	ns
B30c	$\overline{WE}(0:3)/BS_B[0:3]$ negated to A(0:31), $BADDR(28:30)$ invalid GPCM write access, $TRLX = 0$, $CSNT = 1$, $\overline{CS}$ negated to A(0:31) invalid GPCM write access, $TRLX = 0$, $CSNT = 1$, $ACS = 10$ or $ACS = 11$, $EBDF = 1$ (MIN = $0.375 \times B1 - 3.00$)	8.40	—	6.40	—	2.70	—	1.70	—	ns

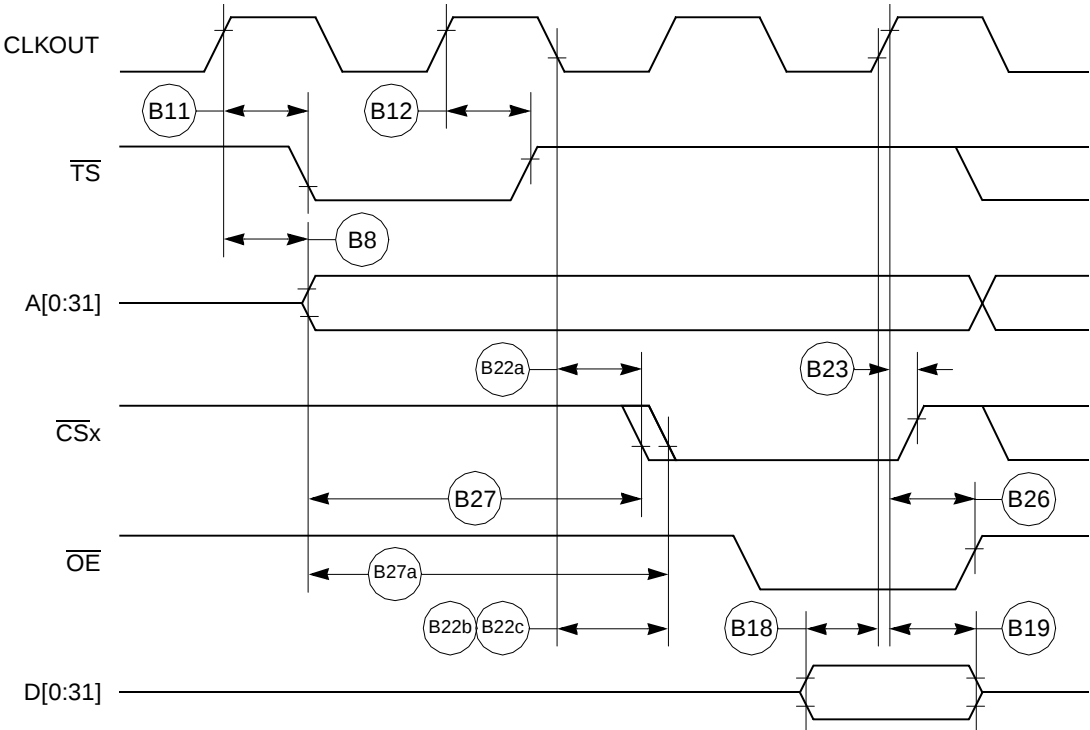


Figure 15. External Bus Read Timing (GPCM Controlled—TRLX = 1, ACS = 10, ACS = 11)

Figure 16 through Figure 18 provide the timing for the external bus write controlled by various GPCM factors.

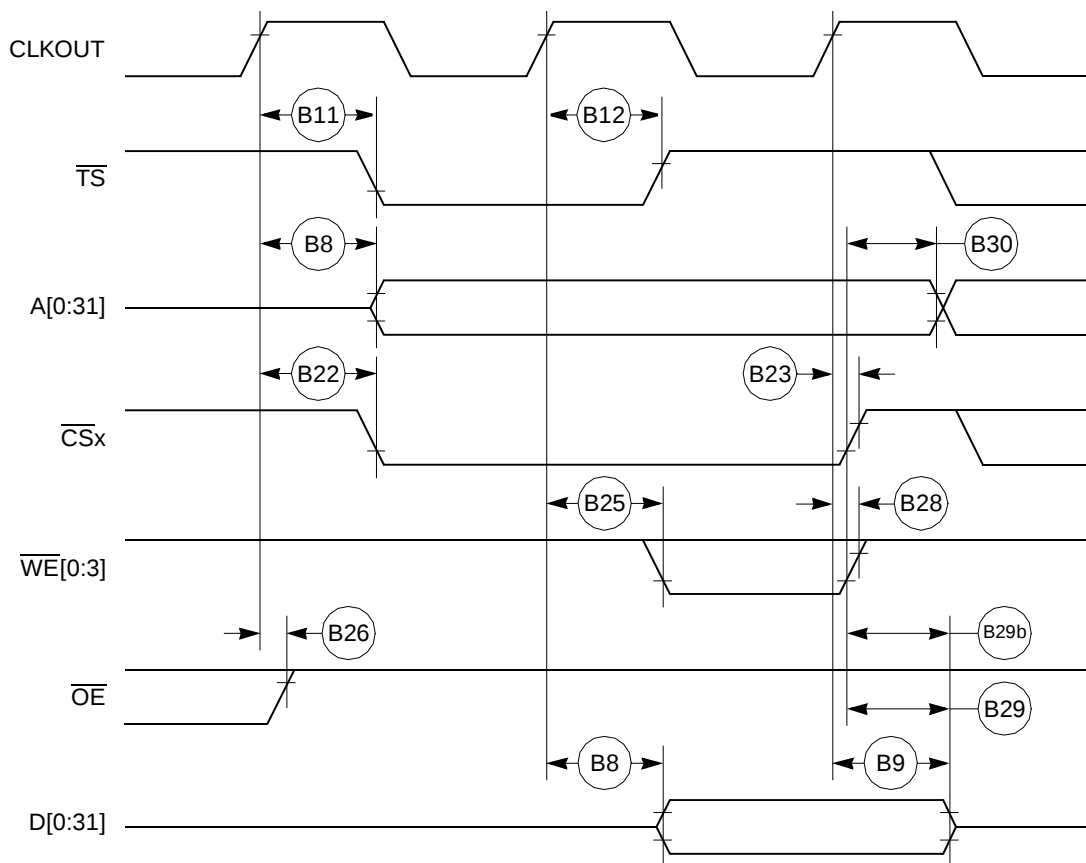


Figure 16. External Bus Write Timing (GPCM Controlled—TRLX = 0, CSNT = 0)

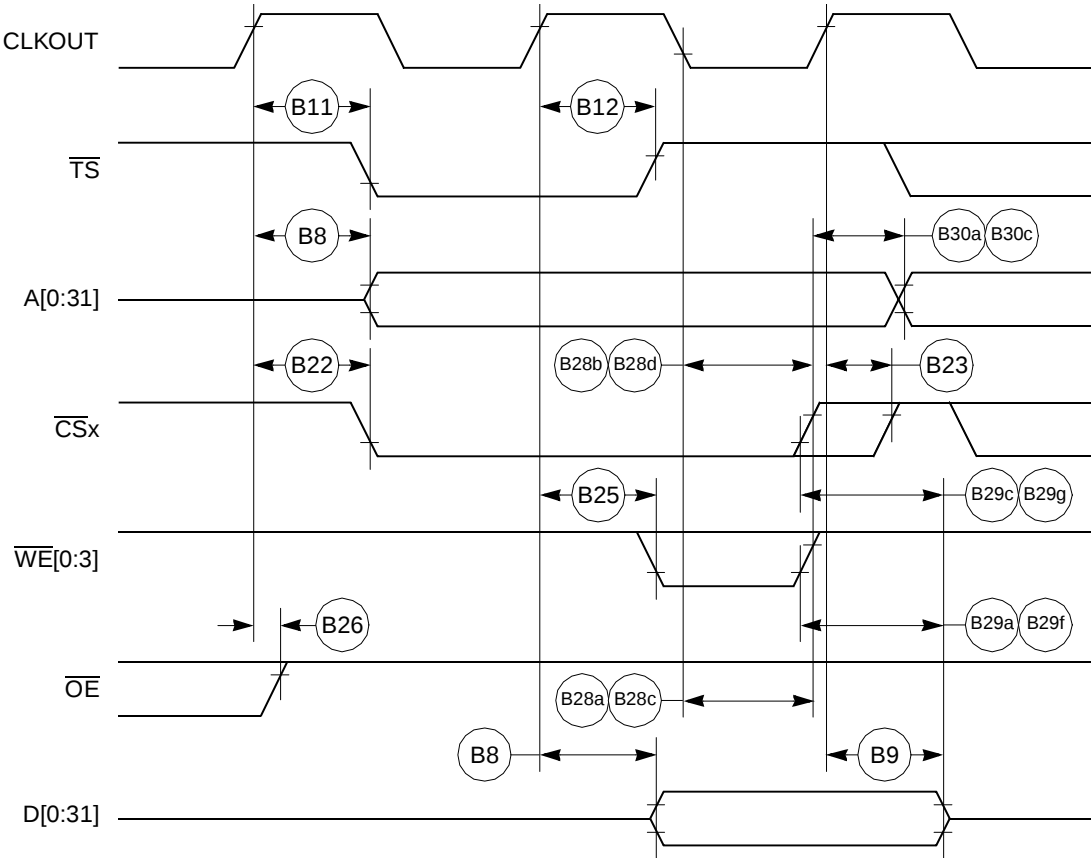


Figure 17. External Bus Write Timing (GPCM Controlled—TRLX = 0, CSNT = 1)

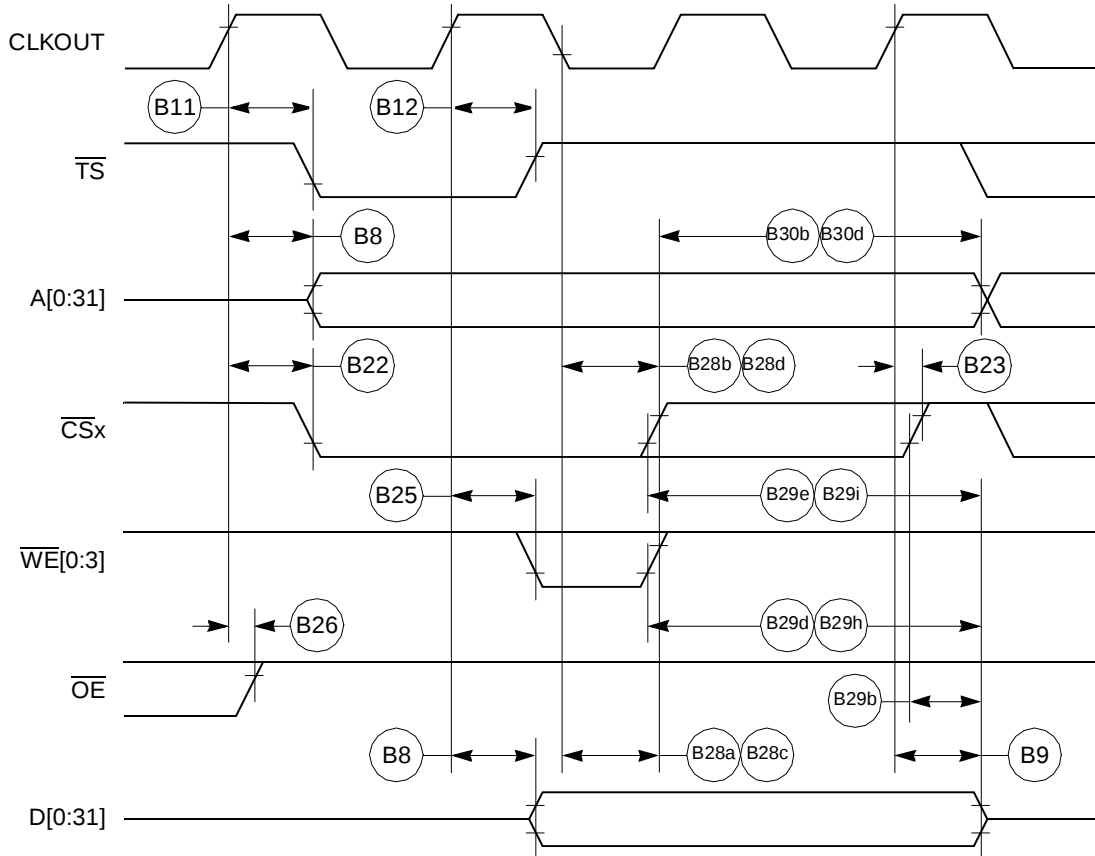


Figure 18. External Bus Write Timing (GPCM Controlled—TRLX = 1, CSNT = 1)

Figure 19 provides the timing for the external bus controlled by the UPM.

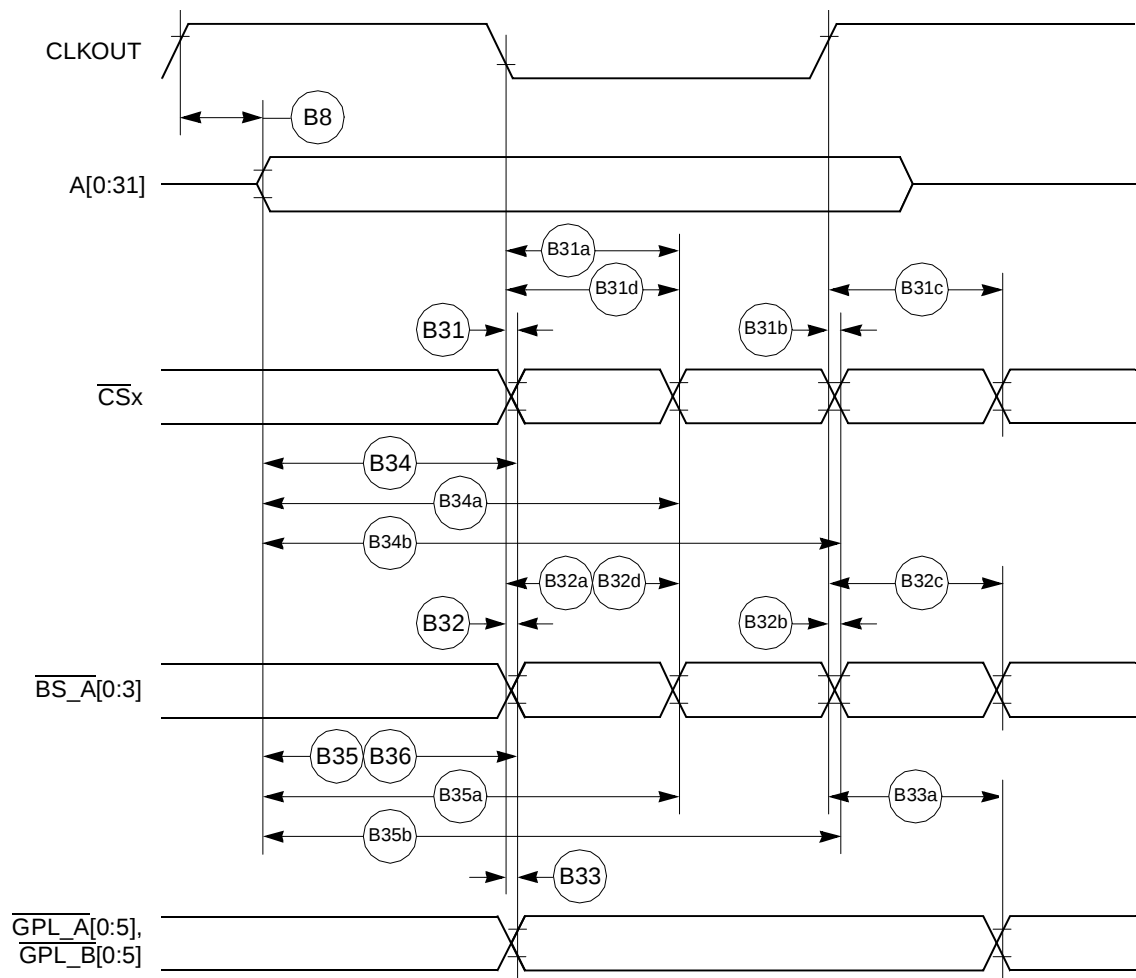


Figure 19. External Bus Timing (UPM Controlled Signals)

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Table 16 provides the JTAG timings for the MPC875/MPC870 shown in Figure 37 through Figure 40.

Table 16. JTAG Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
J82	TCK cycle time	100.00	—	ns
J83	TCK clock pulse width measured at 1.5 V	40.00	—	ns
J84	TCK rise and fall times	0.00	10.00	ns
J85	TMS, TDI data setup time	5.00	—	ns
J86	TMS, TDI data hold time	25.00	—	ns
J87	TCK low to TDO data valid	—	27.00	ns
J88	TCK low to TDO data invalid	0.00	—	ns
J89	TCK low to TDO high impedance	—	20.00	ns
J90	$\overline{\text{TRST}}$ assert time	100.00	—	ns
J91	$\overline{\text{TRST}}$ setup time to TCK low	40.00	—	ns
J92	TCK falling edge to output valid	—	50.00	ns
J93	TCK falling edge to output valid out of high impedance	—	50.00	ns
J94	TCK falling edge to output high impedance	—	50.00	ns
J95	Boundary scan input valid to TCK rising edge	50.00	—	ns
J96	TCK rising edge to boundary scan input invalid	50.00	—	ns

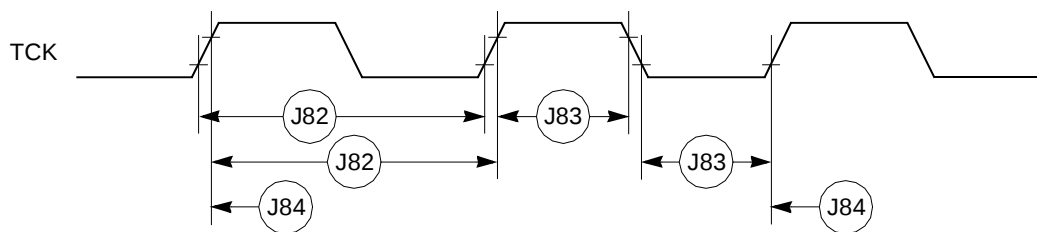
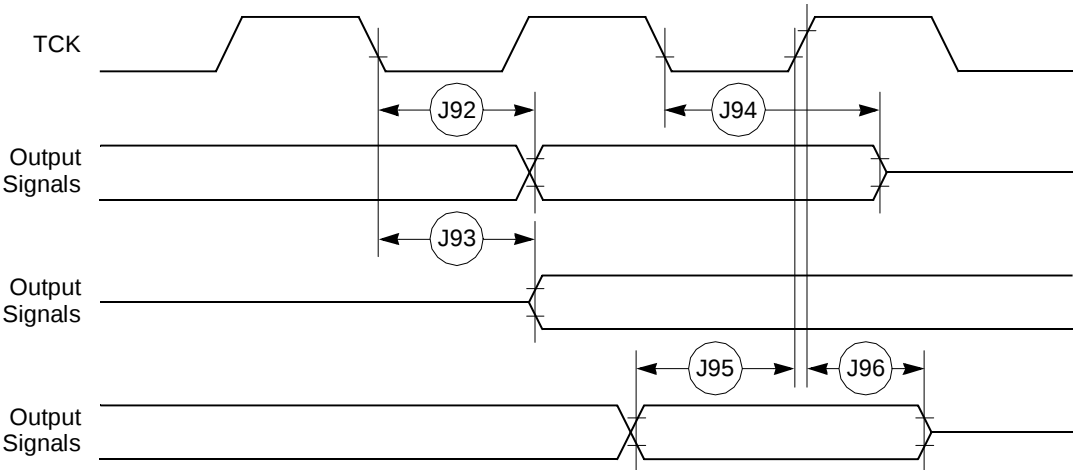
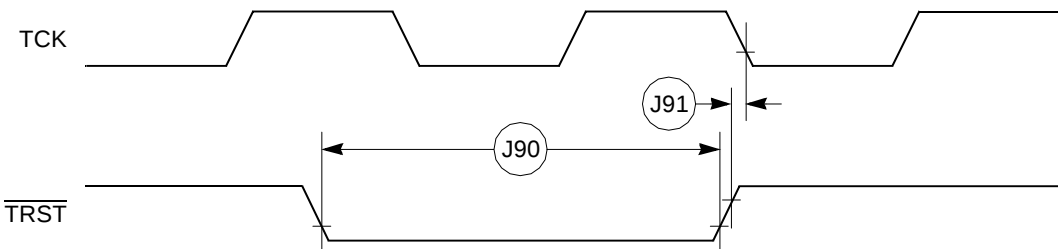
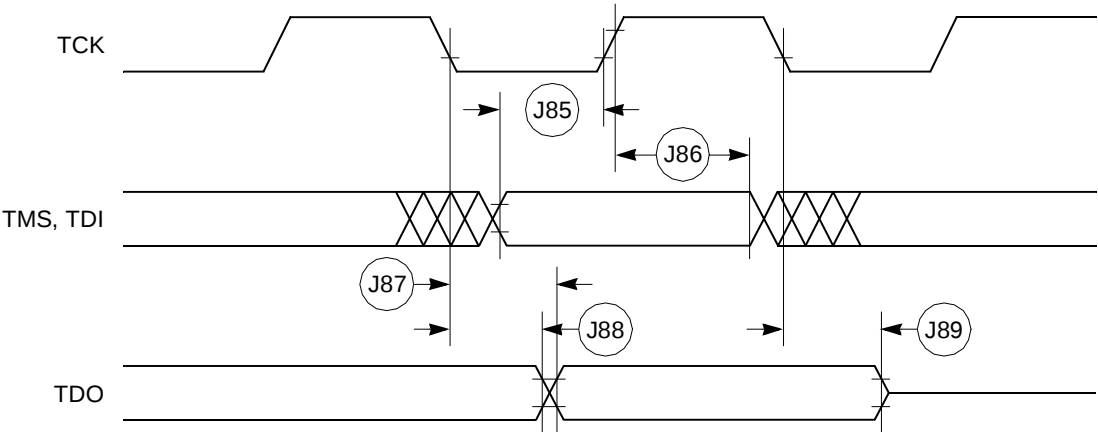


Figure 37. JTAG Test Clock Input Timing



13 CPM Electrical Characteristics

This section provides the AC and DC electrical specifications for the communications processor module (CPM) of the MPC875/MPC870.

13.1 Port C Interrupt AC Electrical Specifications

Table 17 provides the timings for Port C interrupts.

Table 17. Port C Interrupt Timing

Num	Characteristic	33.34 MHz		Unit
		Min	Max	
35	Port C interrupt pulse width low (edge-triggered mode)	55	—	ns
36	Port C interrupt minimum time between active edges	55	—	ns

Figure 41 shows the Port C interrupt detection timing.

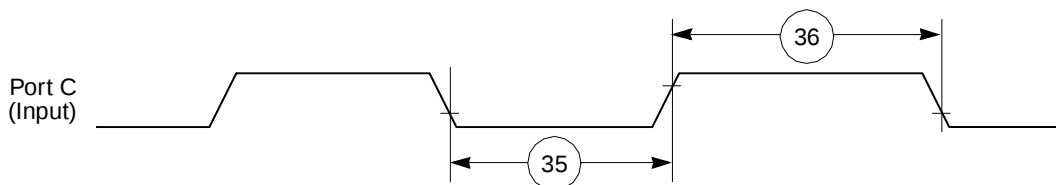


Figure 41. Port C Interrupt Detection Timing

13.2 IDMA Controller AC Electrical Specifications

Table 18 provides the IDMA controller timings as shown in Figure 42 through Figure 45.

Table 18. IDMA Controller Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
40	$\overline{DREQ}$ setup time to clock high	7	—	ns
41	$\overline{DREQ}$ hold time from clock high ¹	TBD	—	ns
42	$\overline{SDACK}$ assertion delay from clock high	—	12	ns
43	$\overline{SDACK}$ negation delay from clock low	—	12	ns
44	$\overline{SDACK}$ negation delay from $\overline{TA}$ low	—	20	ns
45	$\overline{SDACK}$ negation delay from clock high	—	15	ns
46	$\overline{TA}$ assertion to rising edge of the clock setup time (applies to external $\overline{TA}$)	7	—	ns

¹ Applies to high-to-low mode (EDM = 1).

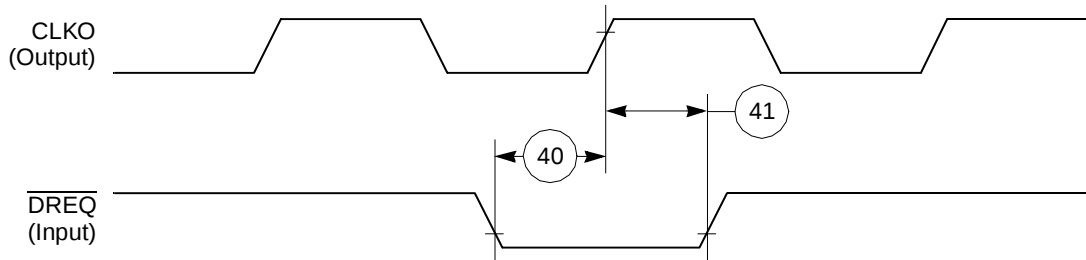


Figure 42. IDMA External Requests Timing Diagram

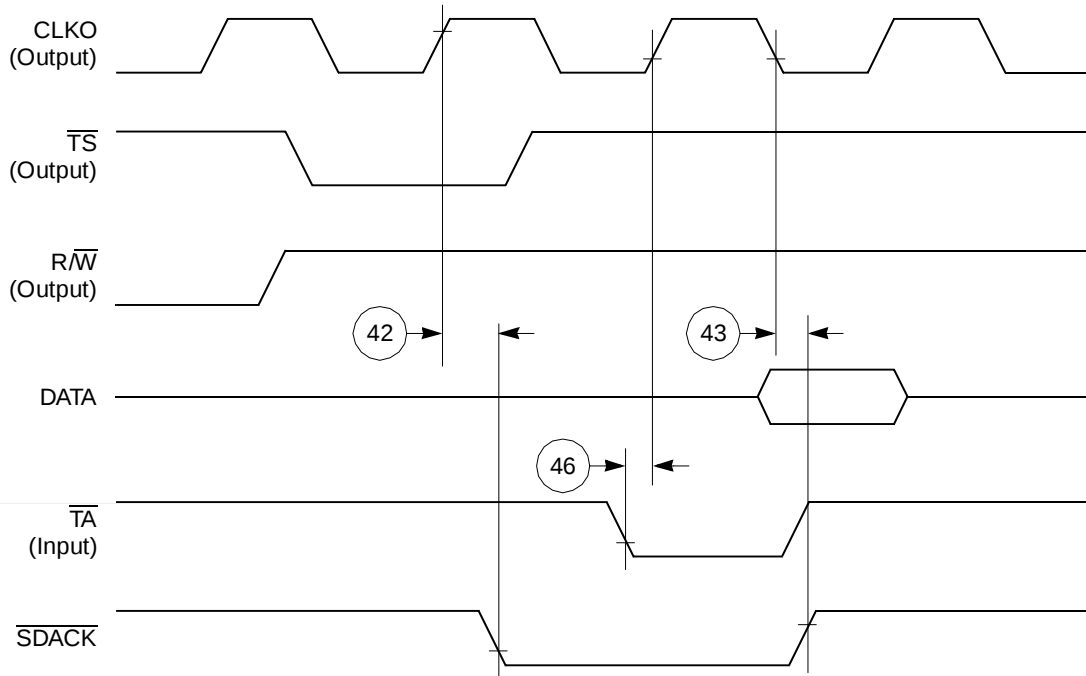


Figure 43. $\overline{SDACK}$ Timing Diagram—Peripheral Write, Externally-Generated $\overline{TA}$

Figure 53 through Figure 55 show the NMSI timings.

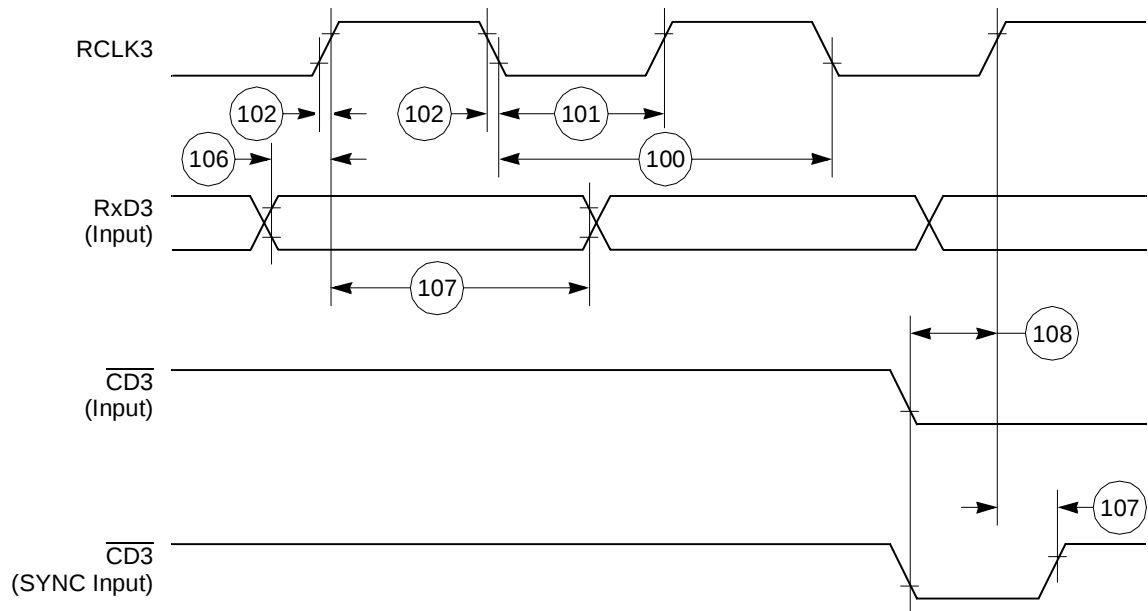


Figure 53. SCC NMSI Receive Timing Diagram

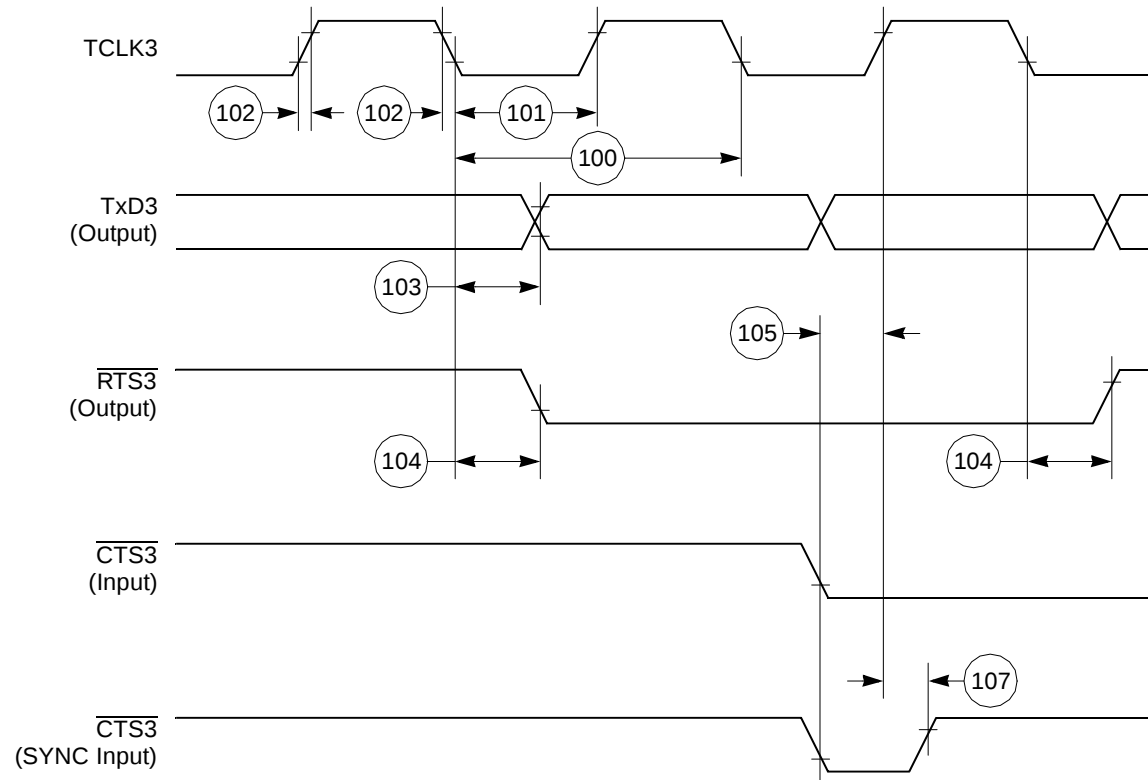


Figure 54. SCC NMSI Transmit Timing Diagram

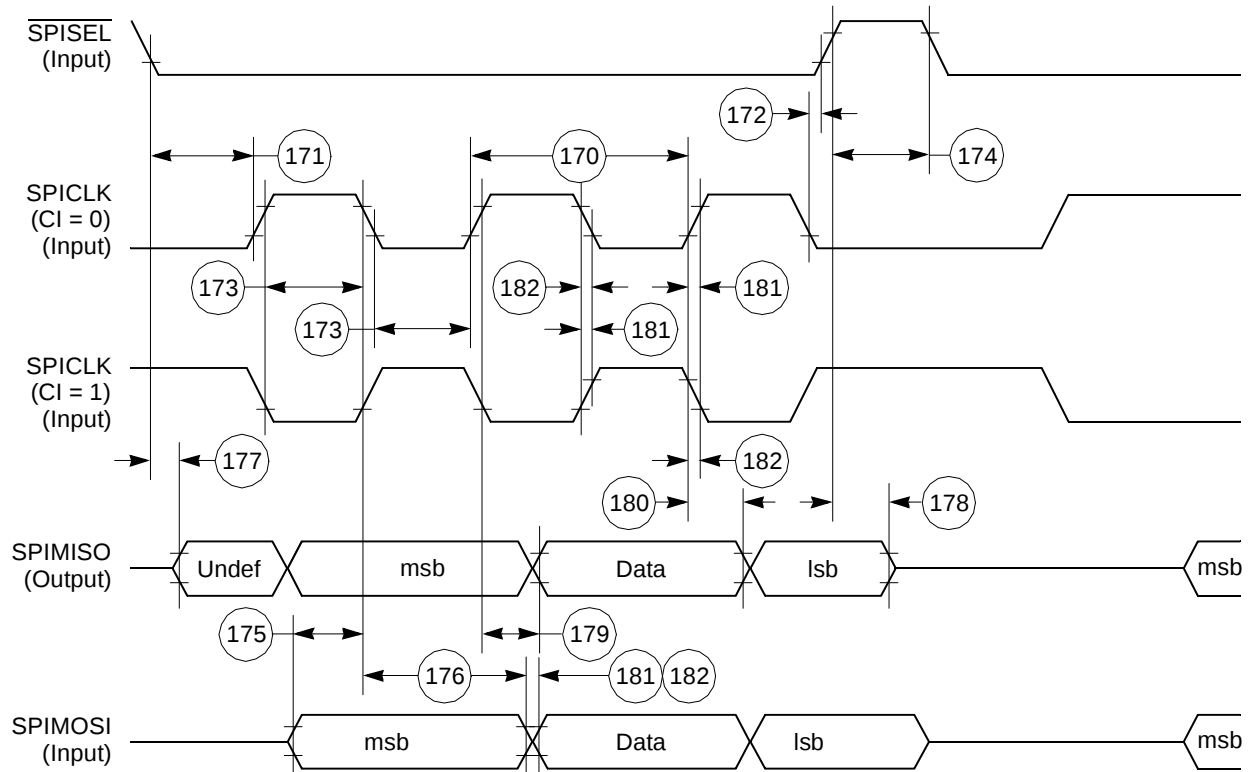


Figure 63. SPI Slave (CP = 1) Timing Diagram

13.11 I²C AC Electrical Specifications

Table 28 provides the I²C (SCL < 100 kHz) timings.

Table 28. I²C Timing (SCL < 100 kHz)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
200	SCL clock frequency (slave)	0	100	kHz
200	SCL clock frequency (master) ¹	1.5	100	kHz
202	Bus free time between transmissions	4.7	—	μs
203	Low period of SCL	4.7	—	μs
204	High period of SCL	4.0	—	μs
205	Start condition setup time	4.7	—	μs
206	Start condition hold time	4.0	—	μs
207	Data hold time	0	—	μs
208	Data setup time	250	—	ns
209	SDL/SCL rise time	—	1	μs

Table 28. I²C Timing (SCL < 100 kHz) (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
210	SDL/SCL fall time	—	300	ns
211	Stop condition setup time	4.7	—	μs

¹ SCL frequency is given by $SCL = BRGCLK_frequency / ((BRG_register + 3) \times pre_scalar \times 2)$.
The ratio $SYNCCLK / (BRGCLK / pre_scalar)$ must be greater than or equal to 4/1.

Table 29 provides the I²C (SCL > 100 kHz) timings.

Table 29. I²C Timing (SCL > 100 kHz)

Num	Characteristic	Expression	All Frequencies		Unit
			Min	Max	
200	SCL clock frequency (slave)	fSCL	0	BRGCLK/48	Hz
200	SCL clock frequency (master) ¹	fSCL	BRGCLK/16512	BRGCLK/48	Hz
202	Bus free time between transmissions	—	$1/(2.2 \times fSCL)$	—	s
203	Low period of SCL	—	$1/(2.2 \times fSCL)$	—	s
204	High period of SCL	—	$1/(2.2 \times fSCL)$	—	s
205	Start condition setup time	—	$1/(2.2 \times fSCL)$	—	s
206	Start condition hold time	—	$1/(2.2 \times fSCL)$	—	s
207	Data hold time	—	0	—	s
208	Data setup time	—	$1/(40 \times fSCL)$	—	s
209	SDL/SCL rise time	—	—	$1/(10 \times fSCL)$	s
210	SDL/SCL fall time	—	—	$1/(33 \times fSCL)$	s
211	Stop condition setup time	—	$1/2(2.2 \times fSCL)$	—	s

¹ SCL frequency is given by $SCL = BRGCLK_frequency / ((BRG_register + 3) \times pre_scalar \times 2)$.
The ratio $SYNCCLK / (BRGCLK / pre_scalar)$ must be greater than or equal to 4/1.

Figure 64 shows the I²C bus timing.

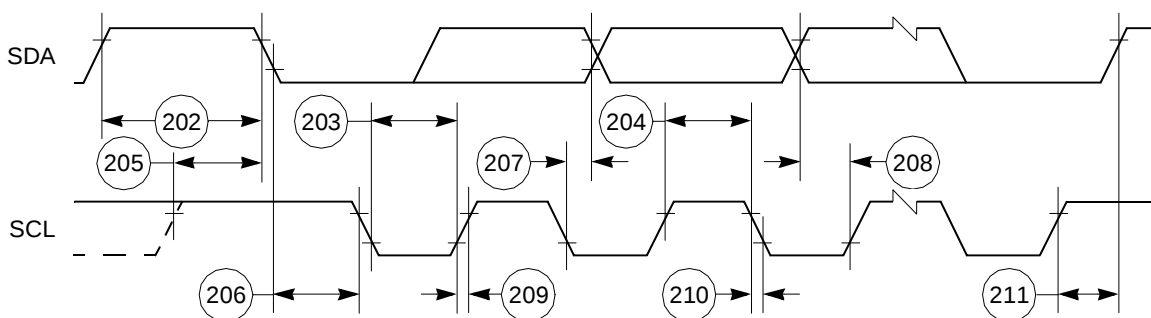

Figure 64. I²C Bus Timing Diagram

Figure 68 shows the MII serial management channel timing diagram.

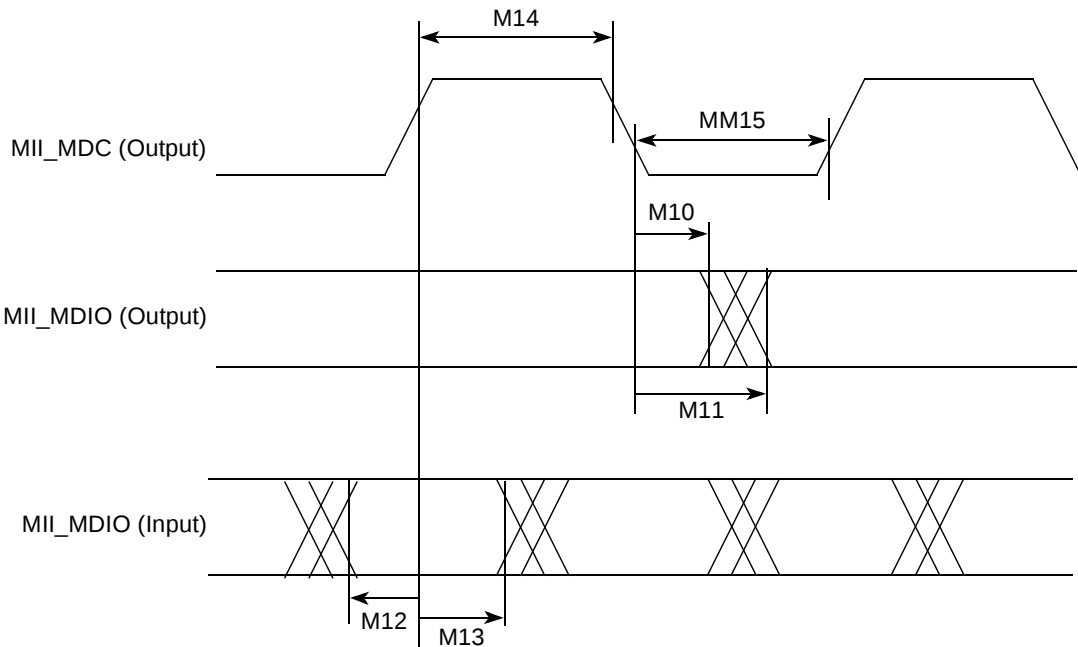


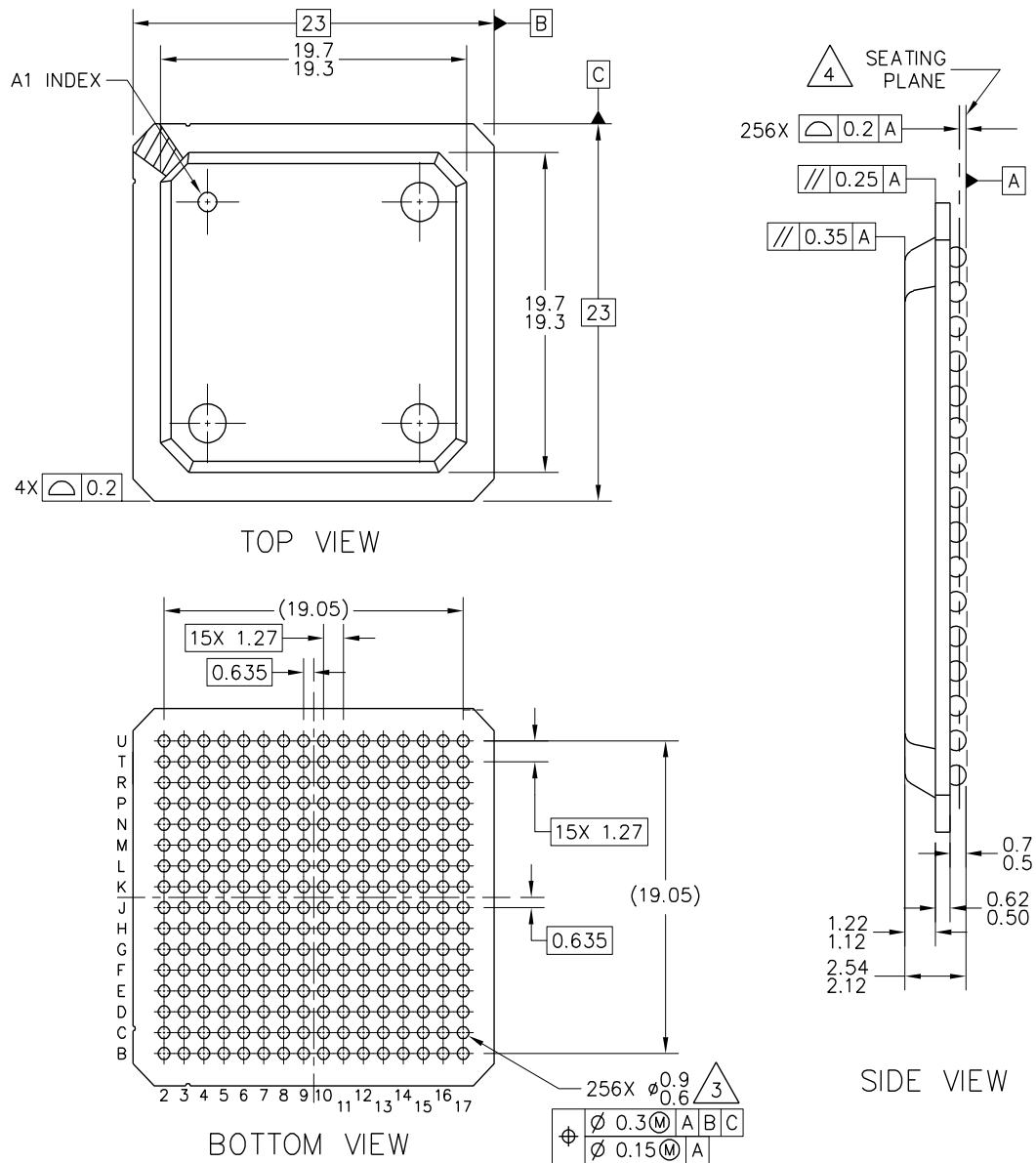
Figure 68. MII Serial Management Channel Timing Diagram

Table 36. Pin Assignments—JEDEC Standard (continued)

Name	Pin Number	Type
$\overline{\text{CS6}}$, CE1_B	F12	Output
$\overline{\text{CS7}}$, CE2_B	D15	Output
$\overline{\text{WE0}}$, BS_B0, $\overline{\text{IORD}}$	E15	Output
$\overline{\text{WE1}}$, BS_B1, $\overline{\text{IOWR}}$	D17	Output
$\overline{\text{WE2}}$, BS_B2, $\overline{\text{PCOE}}$	D16	Output
$\overline{\text{WE3}}$, BS_B3, $\overline{\text{PCWE}}$	G13	Output
$\overline{\text{BS_A}}[0:3]$	F14, E16, E17, F15	Output
$\overline{\text{GPL_A0}}$, $\overline{\text{GPL_B0}}$	C17	Output
$\overline{\text{OE}}$, $\overline{\text{GPL_A1}}$, $\overline{\text{GPL_B1}}$	F13	Output
$\overline{\text{GPL_A}}[2:3]$, $\overline{\text{GPL_B}}[2:3]$, $\overline{\text{CS}}[2-3]$	E14, C16	Output
UPWAITA, $\overline{\text{GPL_A4}}$	D11	Bidirectional (3.3 V only)
UPWAITB, $\overline{\text{GPL_B4}}$	E12	Bidirectional
$\overline{\text{GPL_A5}}$	D12	Output
$\overline{\text{PORESET}}$	D5	Input (3.3 V only)
$\overline{\text{RSTCONF}}$	C3	Input (3.3 V only)
$\overline{\text{HRESET}}$	E7	Open-drain
$\overline{\text{SRESET}}$	C4	Open-drain
XTAL	D6	Analog output
EXTAL	D7	Analog input (3.3 V only)
CLKOUT	G4	Output
EXTCLK	B4	Input (3.3 V only)
TEXP	B3	Output
ALE_A	B7	Output
$\overline{\text{CE1_A}}$	C15	Output
$\overline{\text{CE2_A}}$	D14	Output
$\overline{\text{WAIT_A}}$	D4	Input (3.3 V only)
IP_A0	G6	Input (3.3 V only)
IP_A1	F5	Input (3.3 V only)
IP_A2, $\overline{\text{IOIS16_A}}$	D3	Input (3.3 V only)
IP_A3	E4	Input (3.3 V only)
IP_A4	D2	Input (3.3 V only)
IP_A5	E3	Input (3.3 V only)

16.2 Mechanical Dimensions of the PBGA Package

Figure 70 shows the mechanical dimensions of the PBGA package.



NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M—1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

Note: Solder sphere composition is 95.5%Sn 45%Ag 0.5%Cu for MPC875/MPC870VRXXX.

Solder sphere composition is 62%Sn 36%Pb 2%Ag for MPC875/MPC870ZTXXX.

Figure 70. Mechanical Dimensions and Bottom Surface Nomenclature of the PBGA Package



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