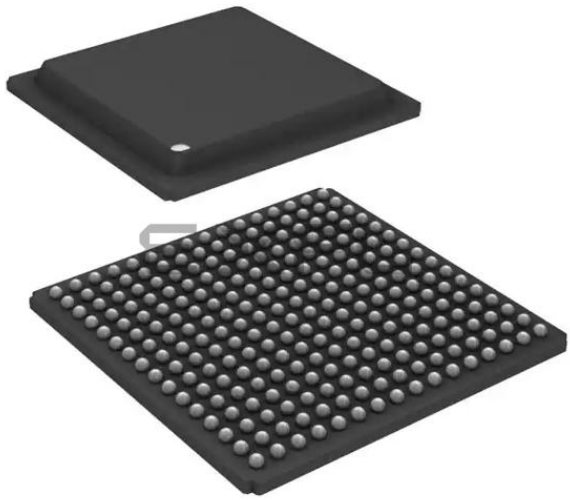

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	66MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (2)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TA)
Security Features	-
Package / Case	256-BBGA
Supplier Device Package	256-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc870vr66

The MPC875 block diagram is shown in Figure 1.

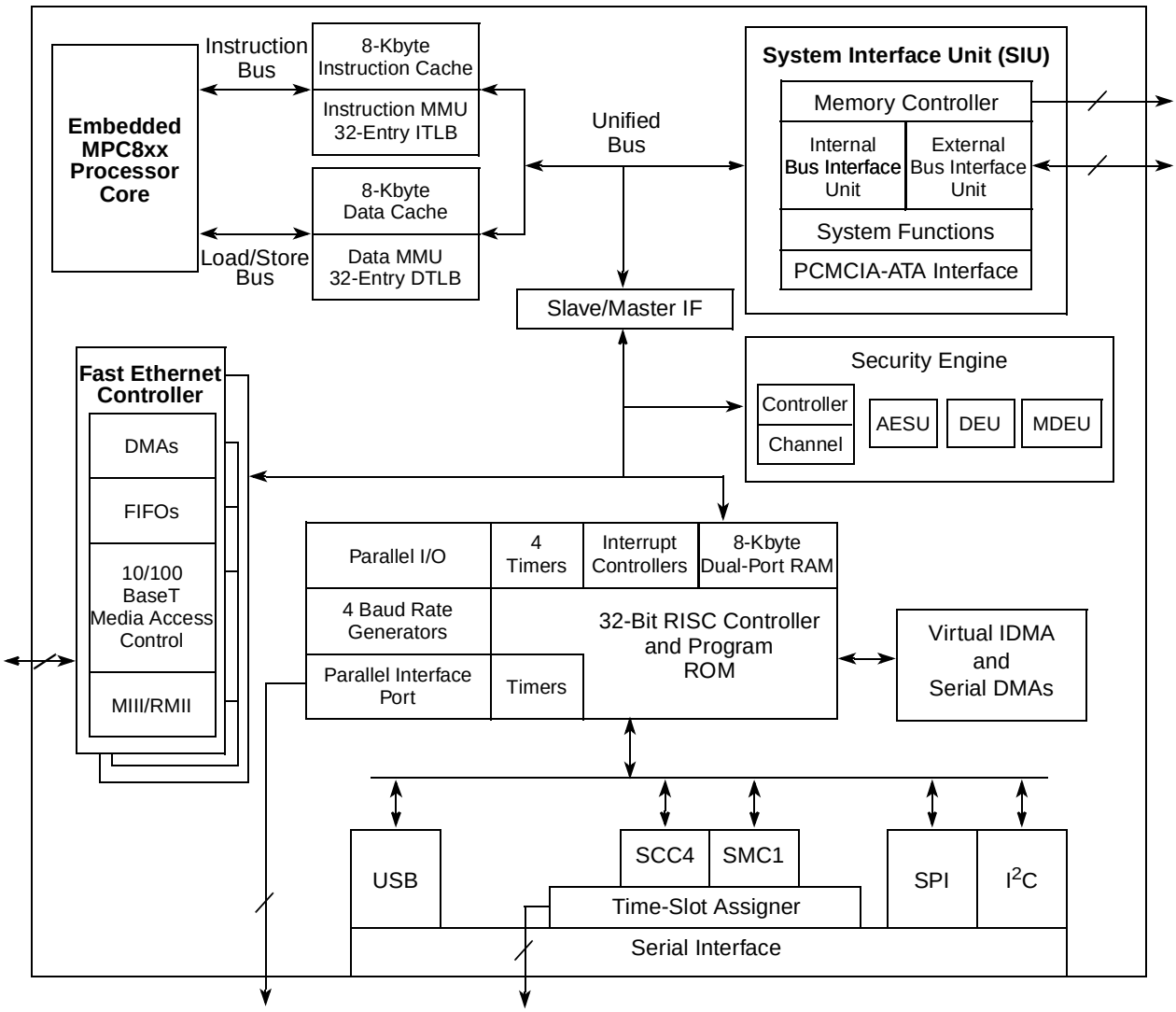


Figure 1. MPC875 Block Diagram

The MPC870 block diagram is shown in Figure 2.

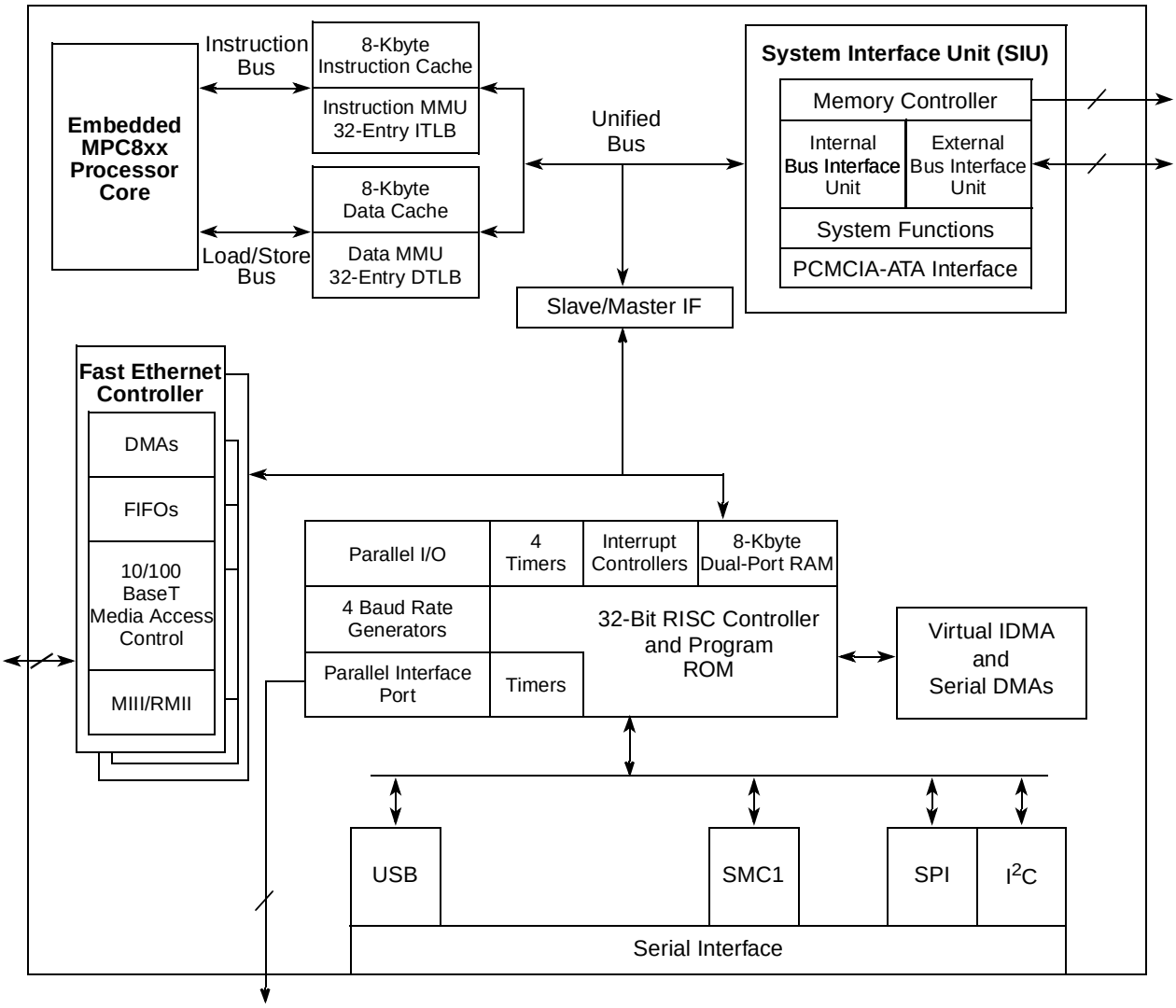


Figure 2. MPC870 Block Diagram

Table 10. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B25	CLKOUT rising edge to $\overline{OE}$, $\overline{WE}$(0:3)/BS_B[0:3] asserted (MAX = 0.00 × B1 + 9.00)	—	9.00		9.00		9.00	—	9.00	ns
B26	CLKOUT rising edge to $\overline{OE}$ negated (MAX = 0.00 × B1 + 9.00)	2.00	9.00	2.00	9.00	2.00	9.00	2.00	9.00	ns
B27	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 1 (MIN = 1.25 × B1 – 2.00)	35.90	—	29.30	—	16.90	—	13.60	—	ns
B27a	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 1 (MIN = 1.50 × B1 – 2.00)	43.50	—	35.50	—	20.70	—	16.75	—	ns
B28	CLKOUT rising edge to $\overline{WE}$(0:3)/BS_B[0:3] negated GPCM write access CSNT = 0 (MAX = 0.00 × B1 + 9.00)	—	9.00	—	9.00	—	9.00	—	9.00	ns
B28a	CLKOUT falling edge to $\overline{WE}$(0:3)/BS_B[0:3] negated GPCM write access TRLX = 0, CSNT = 1, EBDF = 0 (MAX = 0.25 × B1 + 6.80)	7.60	14.30	6.30	13.00	3.80	10.50	3.13	9.93	ns
B28b	CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0, CSNT = 1 ACS = 10 or ACS = 11, EBDF = 0 (MAX = 0.25 × B1 + 6.80)	—	14.30	—	13.00	—	10.50	—	9.93	ns
B28c	CLKOUT falling edge to $\overline{WE}$(0:3)/BS_B[0:3] negated GPCM write access TRLX = 0, CSNT = 1 write access TRLX = 0, CSNT = 1, EBDF = 1 (MAX = 0.375 × B1 + 6.6)	10.90	18.00	10.90	18.00	5.20	12.30	4.69	11.29	ns
B28d	CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1 (MAX = 0.375 × B1 + 6.6)	—	18.00	—	18.00	—	12.30	—	11.30	ns
B29	$\overline{WE}$(0:3)/BS_B[0:3] negated to D(0:31) High-Z GPCM write access, CSNT = 0, EBDF = 0 (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	1.80	—	1.13	—	ns
B29a	$\overline{WE}$(0:3)/BS_B[0:3] negated to D(0:31) High-Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 0 (MIN = 0.50 × B1 – 2.00)	13.20	—	10.50	—	5.60	—	4.25	—	ns
B29b	$\overline{CS}$ negated to D(0:31) High-Z GPCM write access, ACS = 00, TRLX = 0 and CSNT = 0 (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	1.80	—	1.13	—	ns
B29c	$\overline{CS}$ negated to D(0:31) High-Z GPCM write access, TRLX = 0, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 0 (MIN = 0.50 × B1 – 2.00)	13.20	—	10.50	—	5.60	—	4.25	—	ns

Table 10. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B29d	$\overline{WE}$(0:3)/BS_B[0:3] negated to D(0:31) High-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 0 (MIN = 1.50 × B1 – 2.00)	43.50	—	35.50	—	20.70	—	16.75	—	ns
B29e	$\overline{CS}$ negated to D(0:31) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 0 (MIN = 1.50 × B1 – 2.00)	43.50	—	35.50	—	20.70	—	16.75	—	ns
B29f	$\overline{WE}$(0:3/BS_B[0:3]) negated to D(0:31) High-Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 1 (MIN = 0.375 × B1 – 6.30)[7]	5.00	—	3.00	—	0.00	—	0.00	—	ns
B29g	$\overline{CS}$ negated to D(0:31) High-Z GPCM write access, TRLX = 0, CSNT = 1 ACS = 10 or ACS = 11, EBDF = 1 (MIN = 0.375 × B1 – 6.30)[7]	5.00	—	3.00	—	0.00	—	0.00	—	ns
B29h	$\overline{WE}$(0:3)/BS_B[0:3] negated to D(0:31) High-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 1 (MIN = 0.375 × B1 – 3.30)	38.40	—	31.10	—	17.50	—	13.85	—	ns
B29i	$\overline{CS}$ negated to D(0:31) (0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1 (MIN = 0.375 × B1 – 3.30)	38.40	—	31.10	—	17.50	—	13.85	—	ns
B30	$\overline{CS}$, $\overline{WE}$(0:3)/BS_B[0:3] negated to A(0:31), BADDR(28:30) invalid GPCM write access[8] (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	1.80	—	1.13	—	ns
B30a	$\overline{WE}$(0:3)/BS_B[0:3] negated to A(0:31), BADDR(28:30) invalid GPCM, write access, TRLX = 0, CSNT = 1, $\overline{CS}$ negated to A(0:31), invalid GPCM write access TRLX = 0, CSNT = 1, ACS = 10 or ACS == 11, EBDF = 0 (MIN = 0.50 × B1 – 2.00)	13.20	—	10.50	—	5.60	—	4.25	—	ns
B30b	$\overline{WE}$(0:3)/BS_B[0:3] negated to A(0:31), invalid GPCM BADDR(28:30), invalid GPCM write access, TRLX = 1, CSNT = 1. $\overline{CS}$ negated to A(0:31), invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10 or ACS == 11, EBDF = 0 (MIN = 1.50 × B1 – 2.00)	43.50	—	35.50	—	20.70	—	16.75	—	ns
B30c	$\overline{WE}$(0:3)/BS_B[0:3] negated to A(0:31), BADDR(28:30) invalid GPCM write access, TRLX = 0, CSNT = 1. $\overline{CS}$ negated to A(0:31) invalid GPCM write access, TRLX = 0, CSNT = 1 ACS = 10 or ACS == 11, EBDF = 1 (MIN = 0.375 × B1 – 3.00)	8.40	—	6.40	—	2.70	—	1.70	—	ns

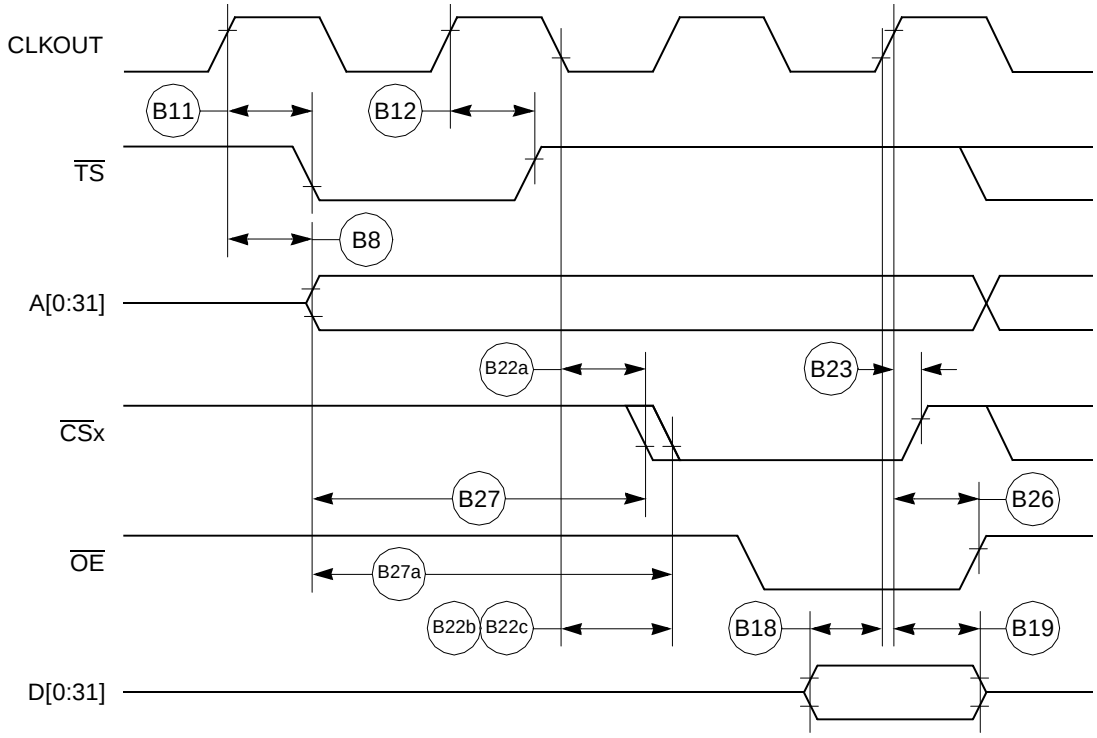


Figure 15. External Bus Read Timing (GPCM Controlled—TRLX = 1, ACS = 10, ACS = 11)

Figure 16 through Figure 18 provide the timing for the external bus write controlled by various GPCM factors.

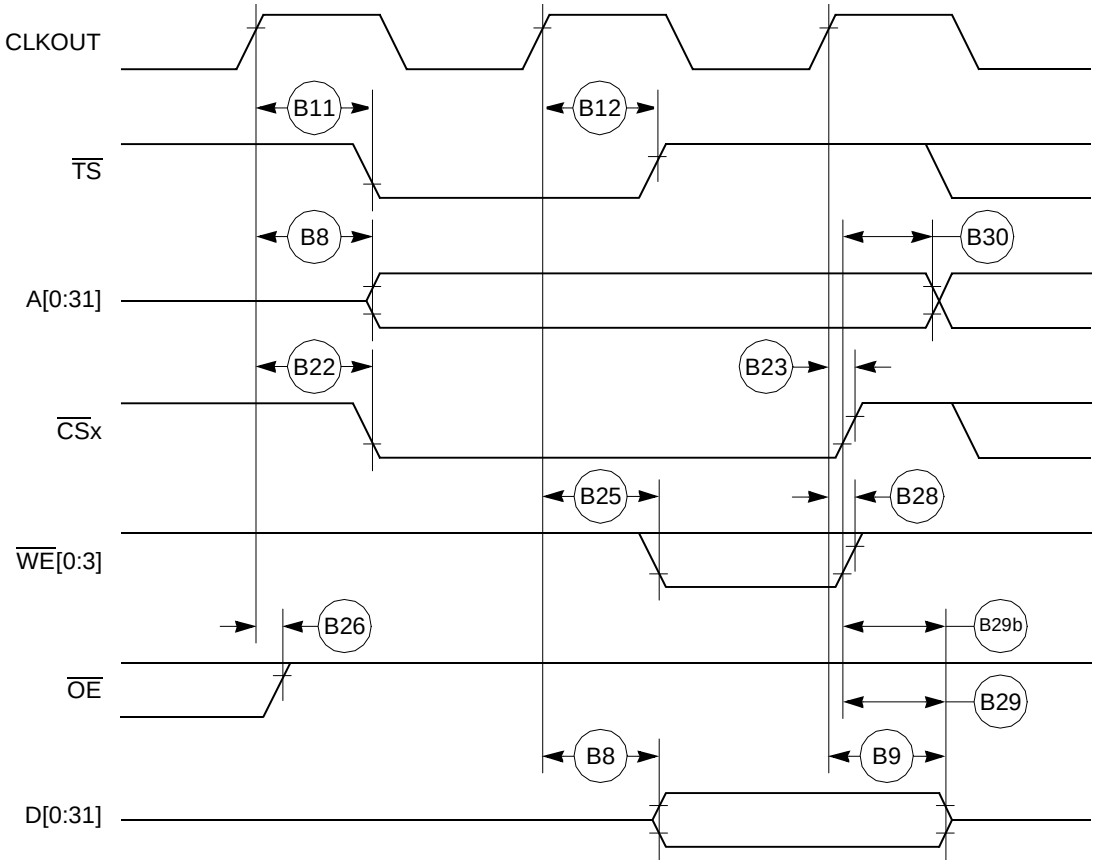


Figure 16. External Bus Write Timing (GPCM Controlled—TRLX = 0, CSNT = 0)

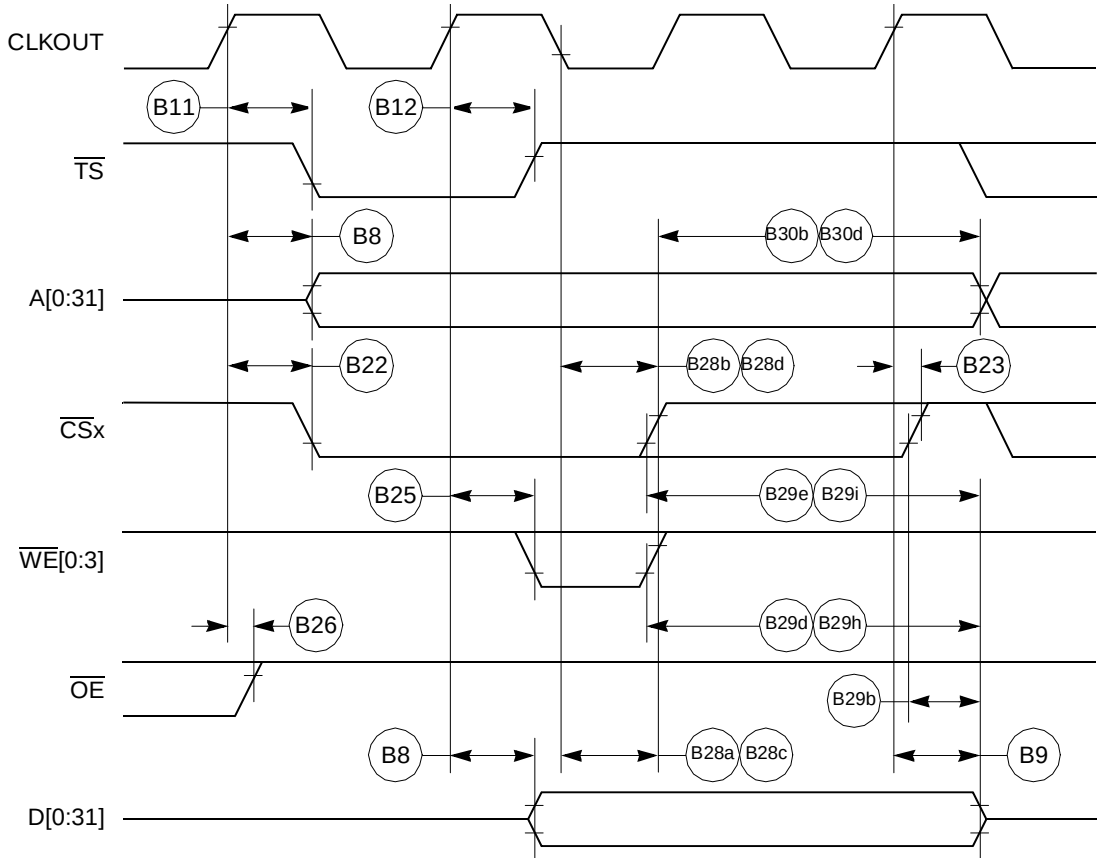


Figure 18. External Bus Write Timing (GPCM Controlled—TRLX = 1, CSNT = 1)

Table 11 provides the interrupt timing for the MPC875/MPC870.

Table 11. Interrupt Timing

Num	Characteristic[1]	All Frequencies		Unit
		Min	Max	
I39	$\overline{\text{IRQ}}$x valid to CLKOUT rising edge (setup time)	6.00		ns
I40	$\overline{\text{IRQ}}$x hold time after CLKOUT	2.00		ns
I41	$\overline{\text{IRQ}}$x pulse width low	3.00		ns
I42	$\overline{\text{IRQ}}$x pulse width high	3.00		ns
I43	$\overline{\text{IRQ}}$x edge-to-edge time	$4 \times T_{CLOCKOUT}$		—

1 The I39 and I40 timings describe the testing conditions under which the $\overline{\text{IRQ}}$ lines are tested when being defined as level sensitive. The $\overline{\text{IRQ}}$ lines are synchronized internally and do not have to be asserted or negated with reference to the CLKOUT. The I41, I42, and I43 timings are specified to allow correct functioning of the $\overline{\text{IRQ}}$ lines detection circuitry and have no direct relation with the total system interrupt latency that the MPC875/MPC870 is able to support.

Figure 25 provides the interrupt detection timing for the external level-sensitive lines.

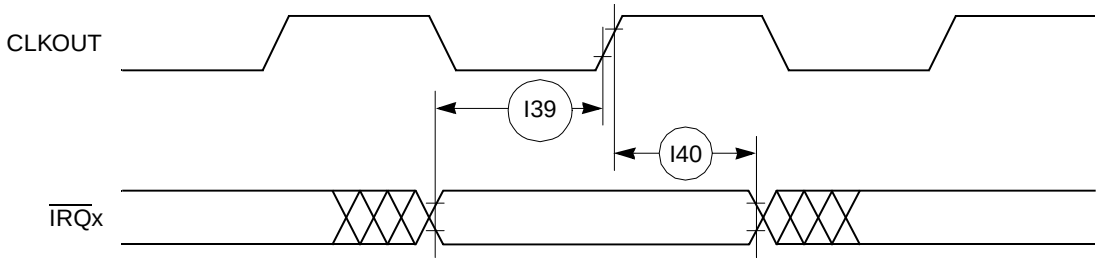


Figure 25. Interrupt Detection Timing for External Level Sensitive Lines

Figure 26 provides the interrupt detection timing for the external edge-sensitive lines.

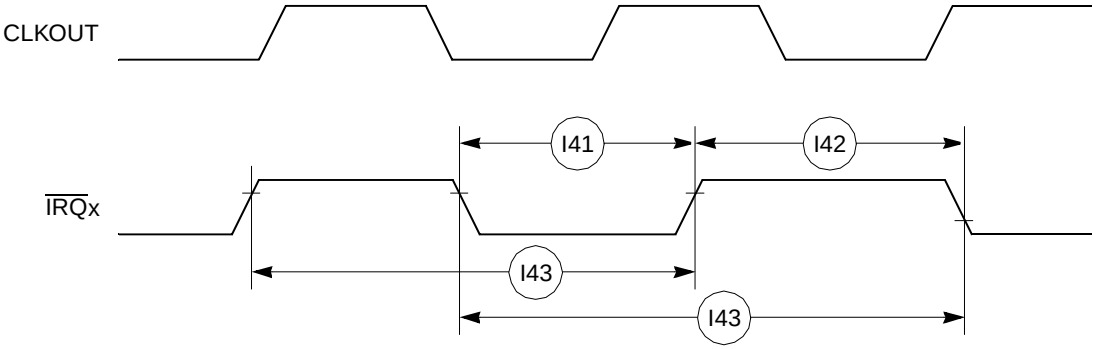


Figure 26. Interrupt Detection Timing for External Edge-Sensitive Lines

Table 12 shows the PCMCIA timing for the MPC875/MPC870.

Table 12. PCMCIA Timing

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
P44	A(0:31), $\overline{\text{REG}}$ valid to PCMCIA strobe asserted[1] (MIN = 0.75 × B1 – 2.00)	20.70	—	16.70	—	9.40	—	7.40	—	ns
P45	A(0:31), $\overline{\text{REG}}$ valid to ALE negation[1] (MIN = 1.00 × B1 – 2.00)	28.30	—	23.00	—	13.20	—	10.50	—	ns
P46	CLKOUT to $\overline{\text{REG}}$ valid (MAX = 0.25 × B1 + 8.00)	7.60	15.60	6.30	14.30	3.80	11.80	3.13	11.13	ns
P47	CLKOUT to $\overline{\text{REG}}$ invalid (MIN = 0.25 × B1 + 1.00)	8.60	—	7.30	—	4.80	—	4.125	—	ns
P48	CLKOUT to $\overline{\text{CE1}}$, $\overline{\text{CE2}}$ asserted (MAX = 0.25 × B1 + 8.00)	7.60	15.60	6.30	14.30	3.80	11.80	3.13	11.13	ns
P49	CLKOUT to $\overline{\text{CE1}}$, $\overline{\text{CE2}}$ negated (MAX = 0.25 × B1 + 8.00)	7.60	15.60	6.30	14.30	3.80	11.80	3.13	11.13	ns
P50	CLKOUT to $\overline{\text{PCOE}}$, $\overline{\text{IORD}}$, $\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ assert time (MAX = 0.00 × B1 + 11.00)	—	11.00	—	11.00	—	11.00	—	11.00	ns
P51	CLKOUT to $\overline{\text{PCOE}}$, $\overline{\text{IORD}}$, $\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ negate time (MAX = 0.00 × B1 + 11.00)	2.00	11.00	2.00	11.00	2.00	11.00	2.00	11.00	ns
P52	CLKOUT to ALE assert time (MAX = 0.25 × B1 + 6.30)	7.60	13.80	6.30	12.50	3.80	10.00	3.13	9.40	ns
P53	CLKOUT to ALE negate time (MAX = 0.25 × B1 + 8.00)	—	15.60	—	14.30	—	11.80	—	11.13	ns
P54	$\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ negated to D(0:31) invalid[1] (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	1.80	—	1.125	—	ns
P55	$\overline{\text{WAITA}}$ and $\overline{\text{WAITB}}$ valid to CLKOUT rising edge[1] (MIN = 0.00 × B1 + 8.00)	8.00	—	8.00	—	8.00	—	8.00	—	ns
P56	CLKOUT rising edge to $\overline{\text{WAITA}}$ and $\overline{\text{WAITB}}$ invalid[1] (MIN = 0.00 × B1 + 2.00)	2.00	—	2.00	—	2.00	—	2.00	—	ns

1 PSST = 1. Otherwise add PSST times cycle time.
PSHT = 0. Otherwise add PSHT times cycle time.
These synchronous timings define when the $\overline{\text{WAITA}}$ signals are detected in order to freeze (or relieve) the PCMCIA current cycle. The $\overline{\text{WAITA}}$ assertion will be effective only if it is detected 2 cycles before the PSL timer expiration. See Chapter 16, “PCMCIA Interface,” in the *MPC885 PowerQUICC™ Family Reference Manual*.

Figure 28 provides the PCMCIA access cycle timing for the external bus write.

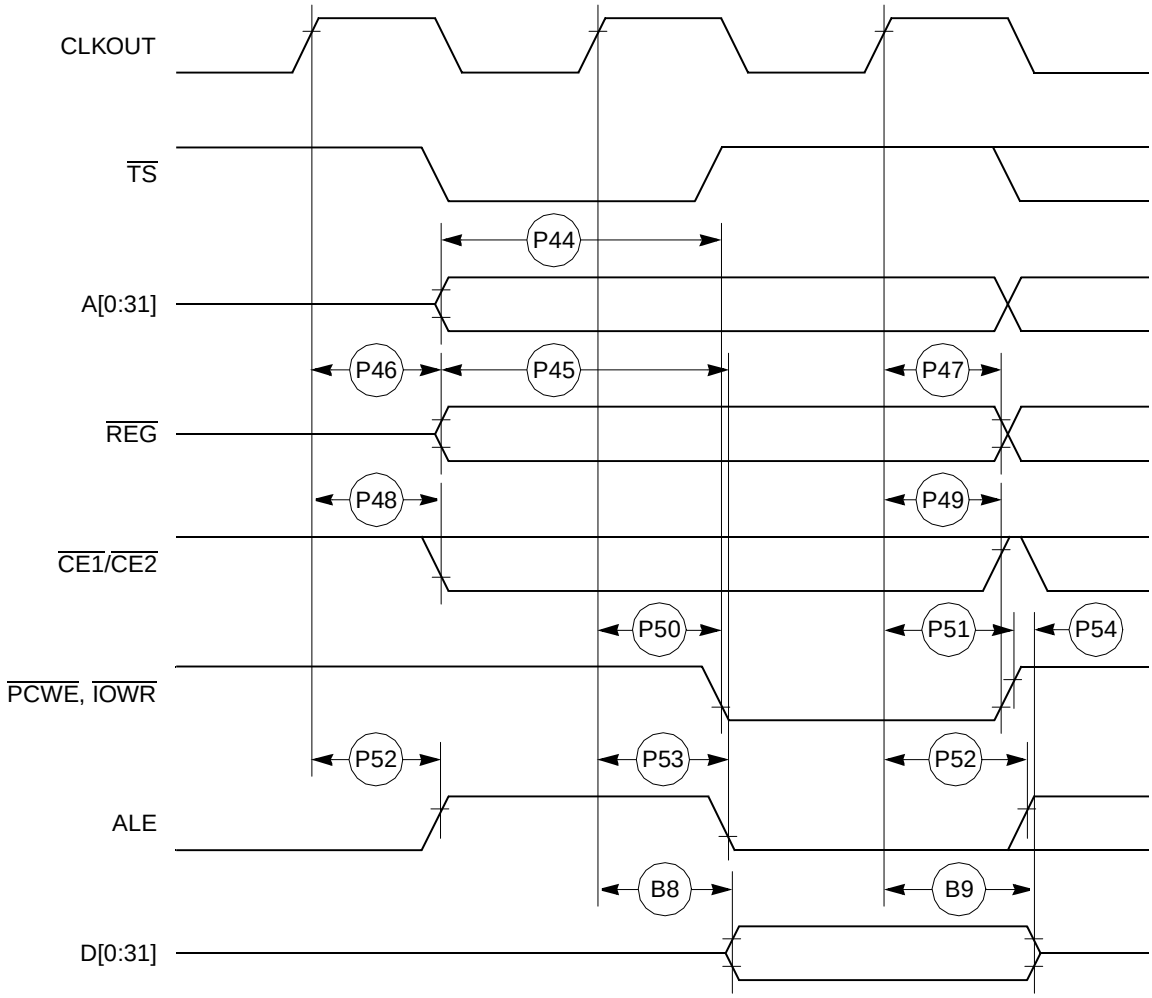


Figure 28. PCMCIA Access Cycles Timing External Bus Write

Figure 29 provides the PCMCIA WAIT signals detection timing.

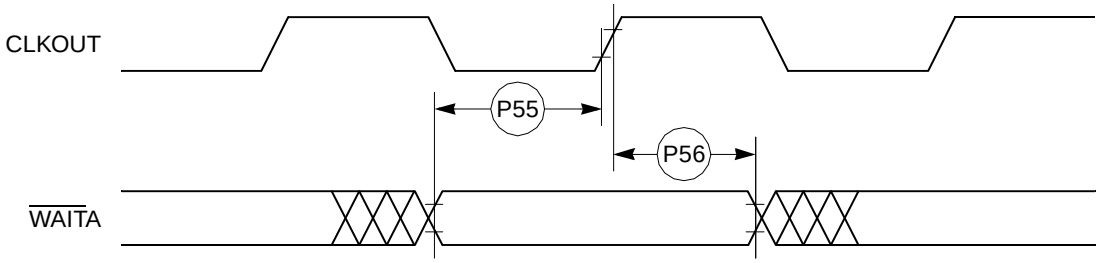


Figure 29. PCMCIA WAIT Signals Detection Timing

Table 13 shows the PCMCIA port timing for the MPC875/MPC870.

Table 13. PCMCIA Port Timing

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
P57	CLKOUT to OPx valid (MAX = 0.00 × B1 + 19.00)	—	19.00	—	19.00	—	19.00	—	19.00	ns
P58	$\overline{\text{HRESET}}$ negated to OPx drive[1] (MIN = 0.75 × B1 + 3.00)	25.70	—	21.70	—	14.40	—	12.40	—	ns
P59	IP_Xx valid to CLKOUT rising edge (MIN = 0.00 × B1 + 5.00)	5.00	—	5.00	—	5.00	—	5.00	—	ns
P60	CLKOUT rising edge to IP_Xx invalid (MIN = 0.00 × B1 + 1.00)	1.00	—	1.00	—	1.00	—	1.00	—	ns

1 OP2 and OP3 only.

Figure 30 provides the PCMCIA output port timing for the MPC875/MPC870.

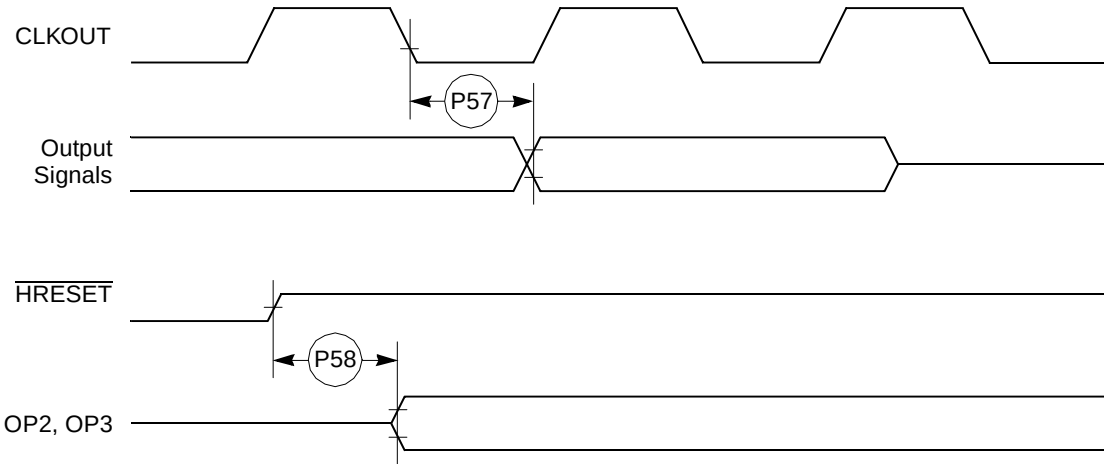


Figure 30. PCMCIA Output Port Timing

Figure 31 provides the PCMCIA input port timing for the MPC875/MPC870.

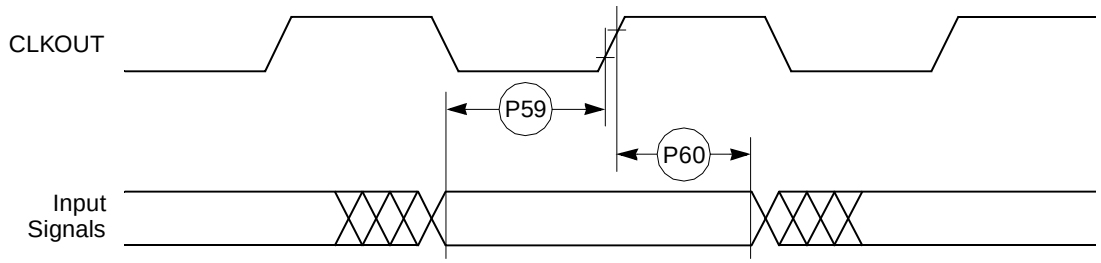


Figure 31. PCMCIA Input Port Timing

Table 15 shows the reset timing for the MPC875/MPC870.

Table 15. Reset Timing

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
R69	CLKOUT to $\overline{\text{HRESET}}$ high impedance (MAX = 0.00 × B1 + 20.00)	—	20.00	—	20.00	—	20.00	—	20.00	ns
R70	CLKOUT to $\overline{\text{SRESET}}$ high impedance (MAX = 0.00 × B1 + 20.00)	—	20.00	—	20.00	—	20.00	—	20.00	ns
R71	$\overline{\text{RSTCONF}}$ pulse width (MIN = 17.00 × B1)	515.20	—	425.00	—	257.60	—	212.50	—	ns
R72	—	—	—	—	—	—	—	—	—	—
R73	Configuration data to $\overline{\text{HRESET}}$ rising edge setup time (MIN = 15.00 × B1 + 50.00)	504.50	—	425.00	—	277.30	—	237.50	—	ns
R74	Configuration data to $\overline{\text{RSTCONF}}$ rising edge setup time (MIN = 0.00 × B1 + 350.00)	350.00	—	350.00	—	350.00	—	350.00	—	ns
R75	Configuration data hold time after $\overline{\text{RSTCONF}}$ negation (MIN = 0.00 × B1 + 0.00)	0.00	—	0.00	—	0.00	—	0.00	—	ns
R76	Configuration data hold time after $\overline{\text{HRESET}}$ negation (MIN = 0.00 × B1 + 0.00)	0.00	—	0.00	—	0.00	—	0.00	—	ns
R77	$\overline{\text{HRESET}}$ and $\overline{\text{RSTCONF}}$ asserted to data out drive (MAX = 0.00 × B1 + 25.00)	—	25.00	—	25.00	—	25.00	—	25.00	ns
R78	$\overline{\text{RSTCONF}}$ negated to data out high impedance (MAX = 0.00 × B1 + 25.00)	—	25.00	—	25.00	—	25.00	—	25.00	ns
R79	CLKOUT of last rising edge before chip three-states $\overline{\text{HRESET}}$ to data out high impedance (MAX = 0.00 × B1 + 25.00)	—	25.00	—	25.00	—	25.00	—	25.00	ns
R80	DSDI, DSCK setup (MIN = 3.00 × B1)	90.90	—	75.00	—	45.50	—	37.50	—	ns
R81	DSDI, DSCK hold time (MIN = 0.00 × B1 + 0.00)	0.00	—	0.00	—	0.00	—	0.00	—	ns
R82	$\overline{\text{SRESET}}$ negated to CLKOUT rising edge for DSDI and DSCK sample (MIN = 8.00 × B1)	242.40	—	200.00	—	121.20	—	100.00	—	ns

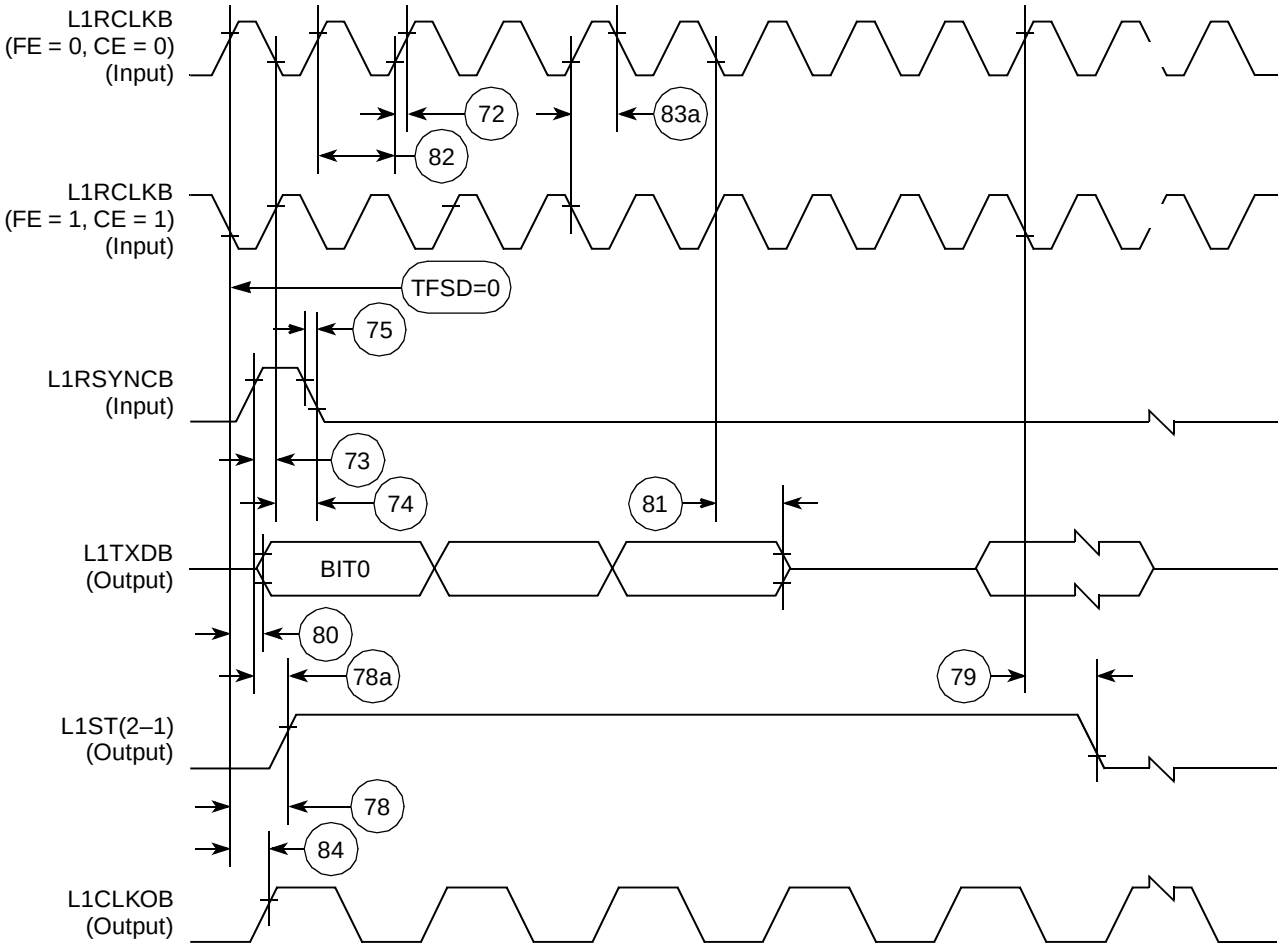


Figure 51. SI Transmit Timing with Double Speed Clocking (DSC = 1)

Table 36 contains a list of the MPC875/MPC870 input and output signals and shows multiplexing and pin assignments.

Table 36. Pin Assignments—JEDEC Standard

Name	Pin Number	Type
A[0:31]	R16, N14, M14, P15, P17, P16, N15, N16, M15, N17, L14, M16, L15, M17, K14, L16, L17, K17, G17, K15, J16, J15, G16, J14, H17, H16, G15, K16, H14, J17, H15, F17	Bidirectional Three-state (3.3 V only)
TSIZ0, $\overline{\text{REG}}$	F16	Bidirectional Three-state (3.3 V only)
TSIZ1	G14	Bidirectional Three-state (3.3 V only)
RD/$\overline{\text{WR}}$	D13	Bidirectional Three-state (3.3 V only)
$\overline{\text{BURST}}$	B9	Bidirectional Three-state (3.3 V only)
$\overline{\text{BDIP}}$, $\overline{\text{GPL\_B5}}$	C13	Output
$\overline{\text{TS}}$	C11	Bidirectional Active pull-up (3.3 V only)
$\overline{\text{TA}}$	C12	Bidirectional Active pull-up (3.3 V only)
$\overline{\text{TEA}}$	B12	Open-drain
$\overline{\text{BI}}$	B13	Bidirectional Active pull-up (3.3 V only)
$\overline{\text{IRQ2}}$, $\overline{\text{RSV}}$	C9	Bidirectional Three-state (3.3 V only)
$\overline{\text{IRQ4}}$, $\overline{\text{KR}}$, $\overline{\text{RETRY}}$, SPKROUT	E9	Bidirectional Three-state (3.3 V only)
D[0:31]	L5, N3, L3, L2, R2, K2, H3, G2, R3, M3, N2, M2, M4, N4, K5, K3, K4, P3, J2, J3, J4, J5, H2, P2, H4, H5, G5, L4, G3, F2, F3, E2	Bidirectional Three-state (3.3 V only)
CR, $\overline{\text{IRQ3}}$	E10	Input
FRZ, $\overline{\text{IRQ6}}$	B10	Bidirectional Three-state (3.3 V only)
$\overline{\text{BR}}$	B11	Bidirectional (3.3 V only)
$\overline{\text{BG}}$	D10	Bidirectional (3.3 V only)
$\overline{\text{BB}}$	C10	Bidirectional Active pull-up (3.3 V only)
$\overline{\text{IRQ0}}$	M6	Input (3.3 V only)
$\overline{\text{IRQ1}}$	P5	Input (3.3 V only)
$\overline{\text{IRQ7}}$	N5	Input (3.3 V only)
$\overline{\text{CS}}$[0:5]	B14, E11, C14, B15, E13, B16	Output

Table 36. Pin Assignments—JEDEC Standard (continued)

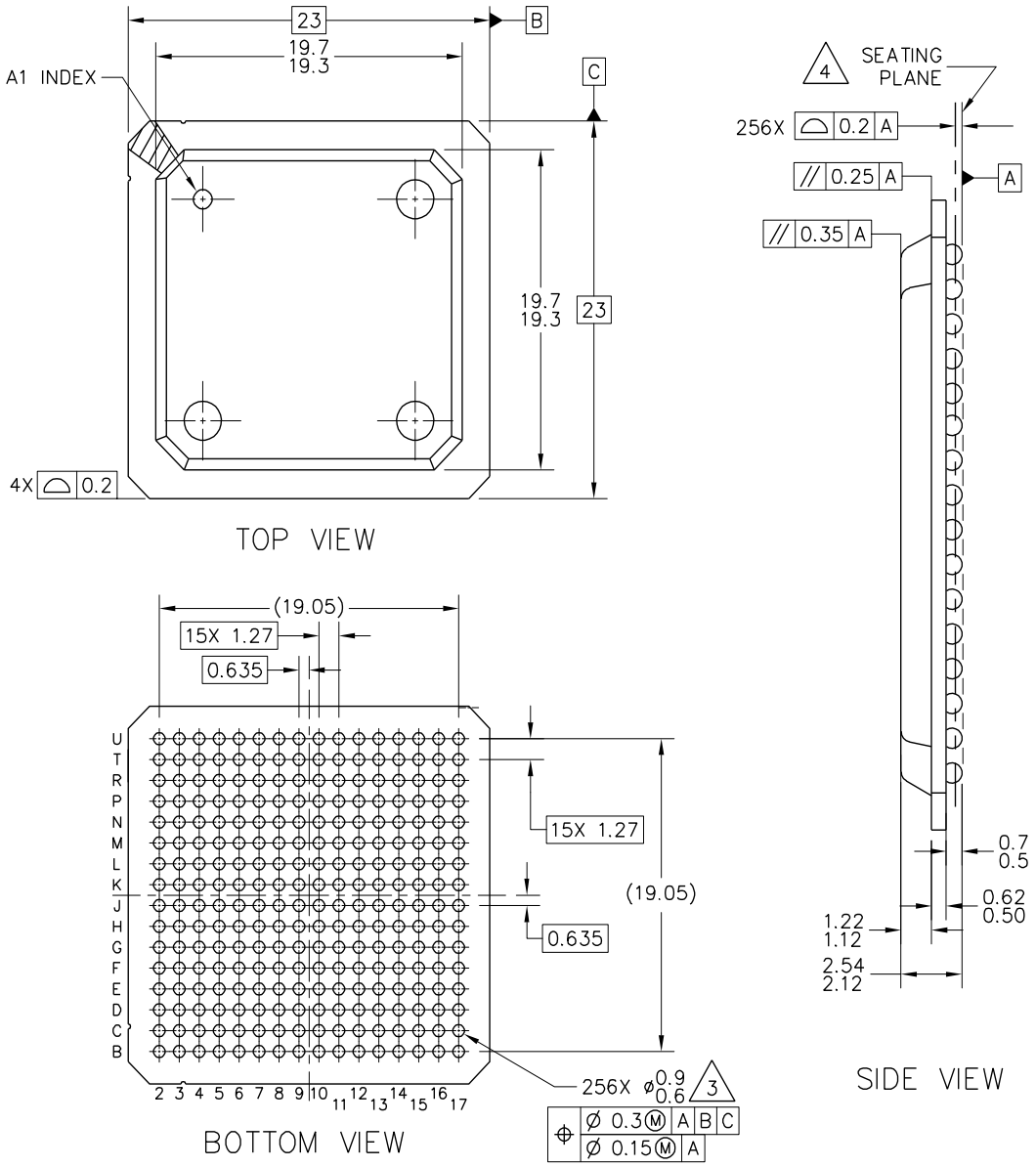
Name	Pin Number	Type
PE29, MII2-CRS	U7	Bidirectional (Optional: open-drain)
PE28, $\overline{\text{TOUT3}}$, MII2-COL	R7	Bidirectional (Optional: open-drain)
PE27, L1RQB, MII2-RXERR, RMII2-RXERR	T6	Bidirectional (Optional: open-drain)
PE26, L1CLKOB, MII2-RXDV, RMII2-CRS_DV	T2	Bidirectional (Optional: open-drain)
PE25, RXD4, MII2-RXD3, L1ST2	R4	Bidirectional (Optional: open-drain)
PE24, SMRXD1, BRGO1, MII2-RXD2	U8	Bidirectional (Optional: open-drain)
PE23, TXD4, MII2-RXCLK, L1ST1	U4	Bidirectional (Optional: open-drain)
PE22, TOUT2, MII2-RXD1, RMII2-RXD1, SDACK1	P4	Bidirectional (Optional: open-drain)
PE21, $\overline{\text{TOUT1}}$, MII2-RXD0, RMII2-RXD0	T9	Bidirectional (Optional: open-drain)
PE20, MII2-TXER	U3	Bidirectional (Optional: open-drain)
PE19, L1TXDB, MII2-TXEN, RMII2-TXEN	R6	Bidirectional (Optional: open-drain)
PE18, SMTXD1, MII2-TXD3	M5	Bidirectional (Optional: open-drain)
PE17, TIN3, CLK5, BRGO3, $\overline{\text{SMSYN1}}$, MII2-TXD2	T8	Bidirectional (Optional: open-drain)
PE16, L1RCLKB, CLK6, MII2-TXCLK, RMII2-REFCLK	U6	Bidirectional (Optional: open-drain)
PE15, $\overline{\text{TGATE1}}$, MII2-TXD1, RMII2-TXD1	T7	Bidirectional
PE14, MII2-TXD0, RMII2-TXD0	P8	Bidirectional
TMS	T14	Input (5-V tolerant)
TDI, DSDI	T13	Input (5-V tolerant)
TCK, DSCK	R13	Input (5-V tolerant)
$\overline{\text{TRST}}$	U14	Input (5-V tolerant)

Table 36. Pin Assignments—JEDEC Standard (continued)

Name	Pin Number	Type
TDO, DSDO	P13	Output (5-V tolerant)
MII1_CRS	U10	Input
MII_MDIO	M13	Bidirectional (5-V tolerant)
MII1_TX_EN, RMII1_TX_EN	U5	Output (5-V tolerant)
MII1_COL	R10	Input
V_{SSSYN}	E5	PLL analog GND
V_{SSSYN1}	F6	PLL analog GND
V_{DDSYN}	E6	PLL analog V_{DD}
GND	H8, H9, H10, H11, J8, J9, J10, J11, K8, K9, K10, K11, L8, L9, L10, L11, U15	Power
V_{DDL}	F7, F8, F9, F10, F11, H6, H13, J6, J13, K6, K13, L6, L13, N7, N8, N9, N10, N11	Power
V_{DDH}	G7, G8, G9, G10, G11, G12, H7, H12, J7, J12, K7, K12, L7, L12, M7, M8, M9, M10, M11, M12	Power
N/C	B17, T16, U2, U17	No connect

16.2 Mechanical Dimensions of the PBGA Package

Figure 70 shows the mechanical dimensions of the PBGA package.



NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M—1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

Note: Solder sphere composition is 95.5%Sn 45%Ag 0.5%Cu for MPC875/MPC870VRXXX.
Solder sphere composition is 62%Sn 36%Pb 2%Ag for MPC875/MPC870ZTXXX.

Figure 70. Mechanical Dimensions and Bottom Surface Nomenclature of the PBGA Package

17 Document Revision History

Table 37 lists significant changes between revisions of this hardware specification.

Table 37. Document Revision History

Revision Number	Date	Changes
0	2/2003	Initial release.
0.1	3/2003	Took out the time-slot assigner and changed the SCC for SCC3 to SCC4.
0.2	5/2003	Changed the package drawing, removed all references to Data Parity. Changed the SPI Master Timing Specs. 162 and 164. Added the RMII and USB timing. Added the 80-MHz timing.
0.3	5/2003	Made sure the pin types were correct. Changed the Features list to agree with the MPC885.
0.4	5/2003	Corrected the signals that had overlines on them. Made corrections on two pins that were typos.
0.5	5/2003	Changed the pin descriptions for PD8 and PD9.
0.6	5/2003	Changed a few typos. Put back the I^2C. Put in the new reset configuration, corrected the USB timing.
0.7	6/2003	Changed the pin descriptions per the June 22 spec, removed Utopia from the pin descriptions, changed PADIR, PBDIR, PCDIR and PDDIR to be 0 in the Mandatory Reset Config.
0.8	8/2003	Added the reference to USB 2.0 to the Features list and removed 1.1 from USB on the block diagrams.
0.9	8/2003	Changed the USB description to full-/low-speed compatible.
1.0	9/2003	Added the DSP information in the Features list. Put a new sentence under Mechanical Dimensions. Fixed table formatting. Nontechnical edits. Released to the external web.
1.1	10/2003	Added TDMb to the MPC875 Features list, the MPC875 Block Diagram, added 13.5 Serial Interface AC Electrical Specifications, and removed TDMa from the pin descriptions.
2.0	12/2003	Changed DBGC in the Mandatory Reset Configuration to X1. Changed the maximum operating frequency to 133 MHz. Put the timing in the 80 MHz column. Put in the orderable part numbers. Rounded the timings to hundredths in the 80 MHz column. Put the pin numbers in footnotes by the maximum currents in Table 6. Changed 22 and 41 in the Timing. Put TBD in the Thermal table.

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