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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	133MHz
Co-Processors/DSP	Communications; CPM, Security; SEC
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (1), 10/100Mbps (2)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 100°C (TA)
Security Features	Cryptography
Package / Case	256-BBGA
Supplier Device Package	256-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc875cvr133

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong





Power Dissipation 5

Table 5 provides information on power dissipation. The modes are 1:1, where CPU and bus speeds are equal, and 2:1, where CPU frequency is twice bus speed.

Die Revision	Bus Mode	Frequency	Typical ¹	Maximum ²	Unit
0	1:1	66 MHz	310	390	mW
		80 MHz	350	430	mW
	2:1	133 MHz	430	495	mW

Table 5. Power Dissipation (P_D)

¹ Typical power dissipation is measured at $V_{DDL} = V_{DDSYN} = 1.8$ V, and V_{DDH} is at 3.3 V. ² Maximum power dissipation at $V_{DDL} = V_{DDSYN} = 1.9$ V, and V_{DDH} is at 3.5 V.

NOTE

The values in Table 5 represent V_{DDL} -based power dissipation and do not include I/O power dissipation over V_{DDH} . I/O power dissipation varies widely by application due to buffer current, depending on external circuitry.

The V_{DDSYN} power dissipation is negligible.

DC Characteristics 6

Table 6 provides the DC electrical characteristics for the MPC875/MPC870.

Table 6. DC Electrical Specifications

Characteristic	Symbol	Min	Мах	Unit
Operating voltage	V _{DDH} (I/O)	3.135	3.465	V
	V _{DDL} (core)	1.7	1.9	V
	V _{DDSYN} 1	1.7	1.9	V
	Difference between V _{DDL} and V _{DDSYN}	_	100	mV
Input high voltage (all inputs except EXTAL and EXTCLK) ²	V _{IH}	2.0	3.465	V
Input low voltage ³	V _{IL}	GND	0.8	V
EXTAL, EXTCLK input high voltage	V _{IHC}	$0.7 imes V_{DDH}$	V _{DDH}	V
Input leakage current, V_{in} = 5.5 V (except TMS, TRST, DSCK, and DSDI pins) for 5-V tolerant pins ¹	l _{in}	—	100	μA
Input leakage current, $V_{in} = V_{DDH}$ (except TMS, TRST, DSCK, and DSDI)	l _{in}	—	10	μA
Input leakage current, $V_{in} = 0 V$ (except TMS, TRST, DSCK, and DSDI pins)	l _{in}	_	10	μA
Input capacitance ⁴	C _{in}	—	20	pF



The maximum bus speed supported by the MPC875/MPC870 is 80 MHz. Higher-speed parts must be operated in half-speed bus mode (for example, an MPC875/MPC870 used at 133 MHz must be configured for a 66 MHz bus). Table 8 shows the frequency ranges for standard part frequencies in 1:1 bus mode, and Table 9 shows the frequency ranges for standard part frequencies in 2:1 bus mode.

Part Frequency	66 I	MHz	80 MHz	
Tart requency	Min	Мах	Min	Мах
Core frequency	40	66.67	40	80
Bus frequency	40	66.67	40	80

Table 8. Frequency Ranges for Standard Part Frequencies (1:1 Bus Mode)

Table 9. Frequency Ranges for Standard Part Frequencies (2:1 Bus Mode)

Part Frequency	66 MHz		80 MHz		133 MHz	
Fait Frequency	Min	Max	Min	Мах	Min	Max
Core frequency	40	66.67	40	80	40	133
Bus frequency	20	33.33	20	40	20	66

Table 10 provides the bus operation timing for the MPC875/MPC870 at 33, 40, 66, and 80 MHz.

The timing for the MPC875/MPC870 bus shown Table 10, assumes a 50-pF load for maximum delays and a 0-pF load for minimum delays. CLKOUT assumes a 100-pF load maximum delay

Table 10. Bus Operation Timings

Num	Characteristic	33	MHz	40 MHz		66 MHz		80 MHz		Unit
Num	Characteristic	Min	Мах	Min	Max	Min	Max	Min	Max	Omt
B1	Bus period (CLKOUT), see Table 8	_	—	—	—	_		—	—	ns
B1a	EXTCLK to CLKOUT phase skew—If CLKOUT is an integer multiple of EXTCLK, then the rising edge of EXTCLK is aligned with the rising edge of CLKOUT. For a non-integer multiple of EXTCLK, this synchronization is lost, and the rising edges of EXTCLK and CLKOUT have a continuously varying phase skew.	-2	+2	-2	+2	-2	+2	-2	+2	ns
B1b	CLKOUT frequency jitter peak-to-peak	_	1	_	1		1	_	1	ns
B1c	Frequency jitter on EXTCLK	_	0.50	_	0.50	_	0.50	_	0.50	%
B1d	CLKOUT phase jitter peak-to-peak for OSCLK \ge 15 MHz		4	—	4		4	—	4	ns
	CLKOUT phase jitter peak-to-peak for OSCLK < 15 MHz		5		5		5		5	ns

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		33	MHz	40 M	MHz	66	MHz	80 MHz		
Num	Characteristic	Min	Max	Min	Max	Min	Max	Min	Max	Unit
B29d	$\label{eq:weight} \hline \hline WE(0:3)/BS_B[0:3] \mbox{ negated to } D(0:31) \mbox{ High-Z} \\ GPCM \mbox{ write access, } TRLX = 1, \mbox{ CSNT} = 1, \\ EBDF = 0 \mbox{ (MIN} = 1.50 \times B1 - 2.00) \\ \hline \hline \end{tabular}$	43.50		35.50		20.70		16.75		ns
B29e	\overline{CS} negated to D(0:31) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 0 (MIN = 1.50 × B1 - 2.00)	43.50	_	35.50		20.70	_	16.75	_	ns
B29f	$\label{eq:weighted_states} \hline \hline WE(0:3/BS_B[0:3]) \ \text{negated to } D(0:31) \ \text{High-Z} \\ \text{GPCM write access, } TRLX = 0, \ \text{CSNT} = 1, \\ \text{EBDF} = 1 \ (\text{MIN} = 0.375 \times \text{B1} - 6.30)^7 \\ \hline \hline \end{array}$	5.00		3.00		0.00		0.00	_	ns
B29g	$\overline{\text{CS}}$ negated to D(0:31) High-Z GPCM write access, TRLX = 0, CSNT = 1 ACS = 10 or ACS = 11, EBDF = 1 (MIN = 0.375 × B1 - 6.30) ⁷	5.00	_	3.00	_	0.00	_	0.00	_	ns
B29h	$eq:weighted_$	38.40	_	31.10	_	17.50	_	13.85	_	ns
B29i	$\frac{\overline{\text{CS}} \text{ negated to D(0:31) (0:3) High-Z GPCM}}{\text{write access, TRLX = 1, CSNT = 1, ACS = 10}}$ or ACS = 11, EBDF = 1 (MIN = 0.375 × B1 - 3.30)	38.40	_	31.10	_	17.50	_	13.85	_	ns
B30	$\overline{\text{CS}}$, $\overline{\text{WE}}(0:3)/\text{BS}_{B}[0:3]$ negated to A(0:31), BADDR(28:30) invalid GPCM write access ⁸ (MIN = 0.25 × B1 - 2.00)	5.60	_	4.30		1.80	_	1.13	_	ns
B30a	$\label{eq:weighted_states} \hline \hline WE(0:3)/BS_B[0:3] \mbox{ negated to } A(0:31), \\ BADDR(28:30) \mbox{ invalid GPCM, write access,} \\ TRLX = 0, \mbox{ CSNT = 1, } \hline CS \mbox{ negated to } A(0:31), \\ \mbox{ invalid GPCM write access } TRLX = 0, \\ CSNT = 1, \mbox{ ACS = 10 or } ACS == 11, \mbox{ EBDF = 0} \\ (MIN = 0.50 \times B1 - 2.00) \\ \hline \hline \hline \hline \end{tabular}$	13.20	_	10.50		5.60	_	4.25	_	ns
B30b	$eq:weighted_$	43.50	_	35.50		20.70	_	16.75	_	ns
B30c	$eq:weighted_$	8.40	_	6.40	_	2.70	_	1.70	_	ns

Table 10. Bus Operation Timings (continued)



Num	Characteristic	33	MHz	40	MHz	66	MHz	80 MHz		Unit
Num	Characteristic	Min	Max	Min	Max	Min	Max	Min	Max	Unit
B30d	WE(0:3)/BS_B[0:3] negated to A(0:31), BADDR(28:30) invalid GPCM write access TRLX = 1, CSNT =1, CS negated to A(0:31) invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10 or 11, EBDF = 1	38.67		31.38		17.83		14.19		ns
B31	CLKOUT falling edge to \overline{CS} valid as requested by control bit CST4 in the corresponding word in the UPM (MAX = $0.00 \times B1 + 6.00$)	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B31a	CLKOUT falling edge to \overline{CS} valid as requested by control bit CST1 in the corresponding word in the UPM (MAX = $0.25 \times B1 + 6.80$)	7.60	14.30	6.30	13.00	3.80	10.50	3.13	10.00	ns
B31b	CLKOUT rising edge to \overline{CS} valid, as requested by control bit CST2 in the corresponding word in the UPM (MAX = $0.00 \times B1 + 8.00$)	1.50	8.00	1.50	8.00	1.50	8.00	1.50	8.00	ns
B31c	CLKOUT rising edge to \overline{CS} valid, as requested by control bit CST3 in the corresponding word in the UPM (MAX = $0.25 \times B1 + 6.30$)	7.60	13.80	6.30	12.50	3.80	10.00	3.13	9.40	ns
B31d	CLKOUT falling edge to \overline{CS} valid as requested by control bit CST1 in the corresponding word in the UPM EBDF = 1 (MAX = 0.375 × B1 + 6.6)	13.30	18.00	11.30	16.00	7.60	12.30	4.69	11.30	ns
B32	CLKOUT falling edge to $\overline{\text{BS}}$ valid as requested by control bit BST4 in the corresponding word in the UPM (MAX = 0.00 × B1 + 6.00)	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B32a	CLKOUT falling edge to \overline{BS} valid as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 0 (MAX = 0.25 × B1 + 6.80)	7.60	14.30	6.30	13.00	3.80	10.50	3.13	10.00	ns
B32b	CLKOUT rising edge to $\overline{\text{BS}}$ valid, as requested by control bit BST2 in the corresponding word in the UPM (MAX = $0.00 \times \text{B1} + 8.00$)	1.50	8.00	1.50	8.00	1.50	8.00	1.50	8.00	ns
B32c	CLKOUT rising edge to $\overline{\text{BS}}$ valid, as requested by control bit BST3 in the corresponding word in the UPM (MAX = $0.25 \times \text{B1} + 6.80$)	7.60	14.30	6.30	13.00	3.80	10.50	3.13	10.00	ns
B32d	CLKOUT falling edge to \overline{BS} valid as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 1 (MAX = 0.375 × B1 + 6.60)	13.30	18.00	11.30	16.00	7.60	12.30	4.49	11.30	ns
B33	CLKOUT falling edge to $\overline{\text{GPL}}$ valid as requested by control bit GxT4 in the corresponding word in the UPM (MAX = 0.00 × B1 + 6.00)	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns

Table 10. Bus Operation Timings (continued)



Figure 5 provides the control timing diagram.

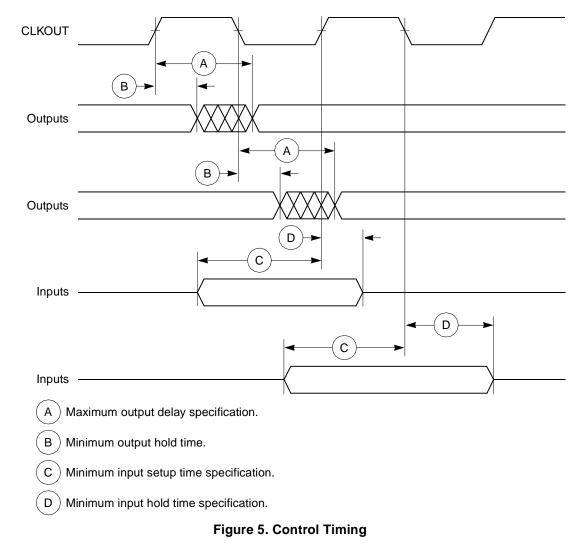


Figure 6 provides the timing for the external clock.

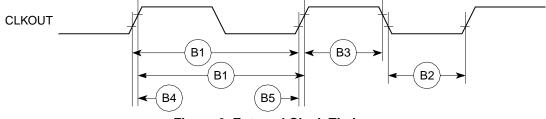


Figure 6. External Clock Timing

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Figure 11 provides the timing for the input data controlled by the UPM for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

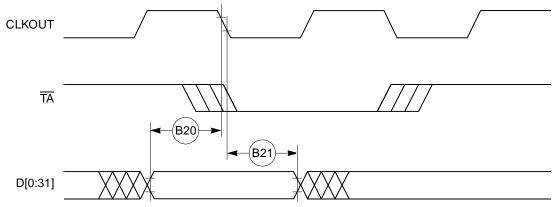


Figure 11. Input Data Timing when Controlled by UPM in the Memory Controller and DLT3 = 1

Figure 12 through Figure 15 provide the timing for the external bus read controlled by various GPCM factors.

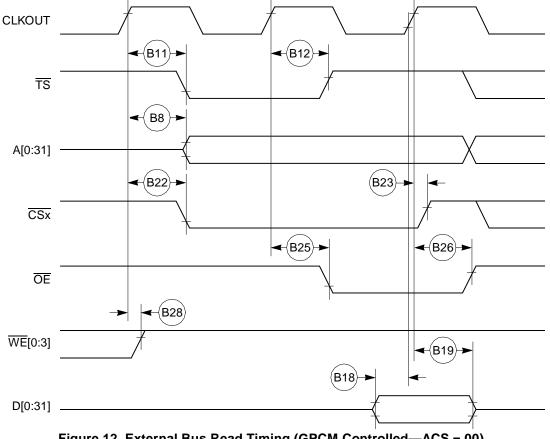
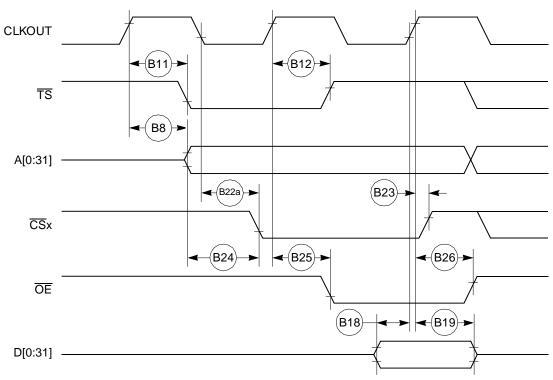


Figure 12. External Bus Read Timing (GPCM Controlled—ACS = 00)

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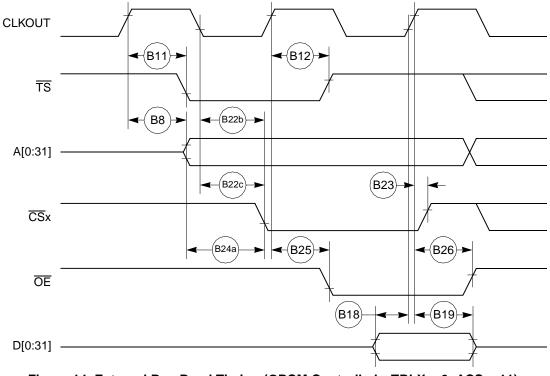


Figure 14. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 11)

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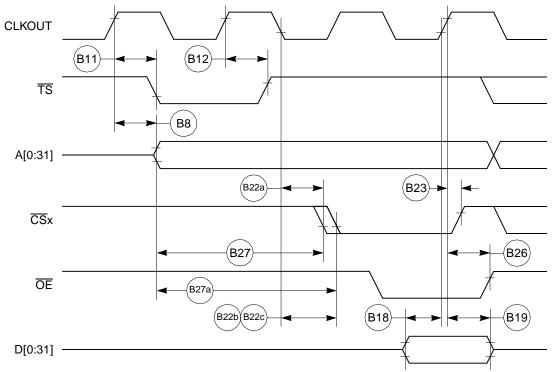
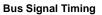


Figure 15. External Bus Read Timing (GPCM Controlled—TRLX = 1, ACS = 10, ACS = 11)





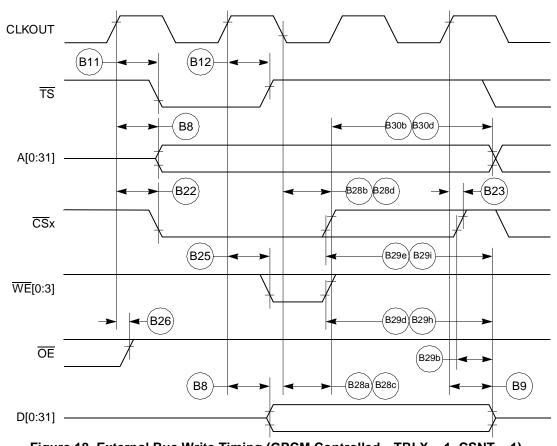


Figure 18. External Bus Write Timing (GPCM Controlled—TRLX = 1, CSNT = 1)



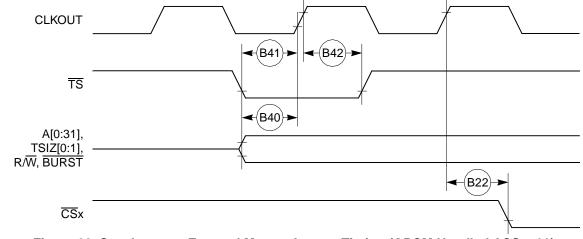


Figure 22 provides the timing for the synchronous external master access controlled by the GPCM.

Figure 22. Synchronous External Master Access Timing (GPCM Handled ACS = 00)

Figure 23 provides the timing for the asynchronous external master memory access controlled by the GPCM.

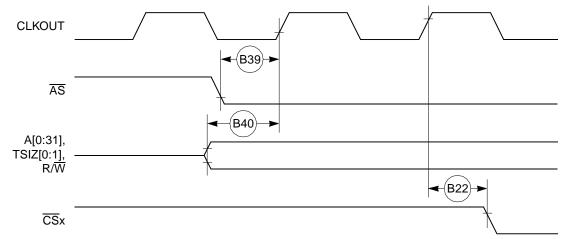




Figure 24 provides the timing for the asynchronous external master control signals negation.

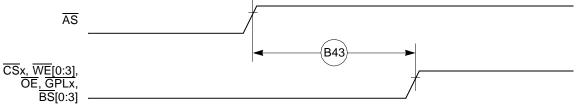
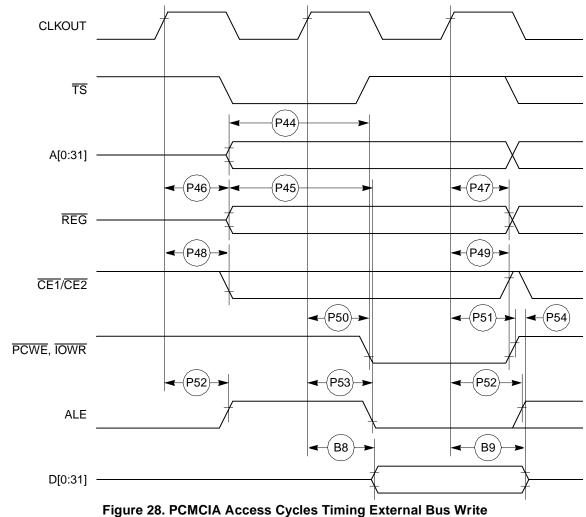


Figure 24. Asynchronous External Master—Control Signals Negation Timing



Figure 28 provides the PCMCIA access cycle timing for the external bus write.



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Figure 29 provides the PCMCIA \overline{WAIT} signals detection timing.

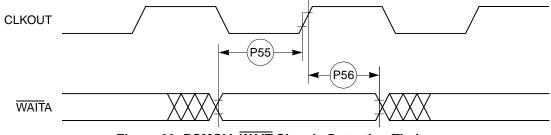


Figure 29. PCMCIA WAIT Signals Detection Timing

CPM Electrical Characteristics



13 CPM Electrical Characteristics

This section provides the AC and DC electrical specifications for the communications processor module (CPM) of the MPC875/MPC870.

13.1 Port C Interrupt AC Electrical Specifications

Table 17 provides the timings for Port C interrupts.

Table	17.	Port C	Interrupt	Timing
-------	-----	--------	-----------	--------

Num	Characteristic	33.34	MHz	Unit
Num	Characteristic		Мах	Onic
35	Port C interrupt pulse width low (edge-triggered mode)	55	_	ns
36	Port C interrupt minimum time between active edges	55	_	ns

Figure 41 shows the Port C interrupt detection timing.

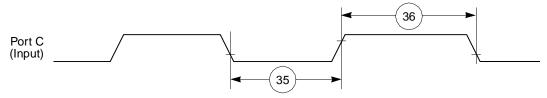


Figure 41. Port C Interrupt Detection Timing

13.2 IDMA Controller AC Electrical Specifications

Table 18 provides the IDMA controller timings as shown in Figure 42 through Figure 45.

Table 18. IDMA Controller Timing

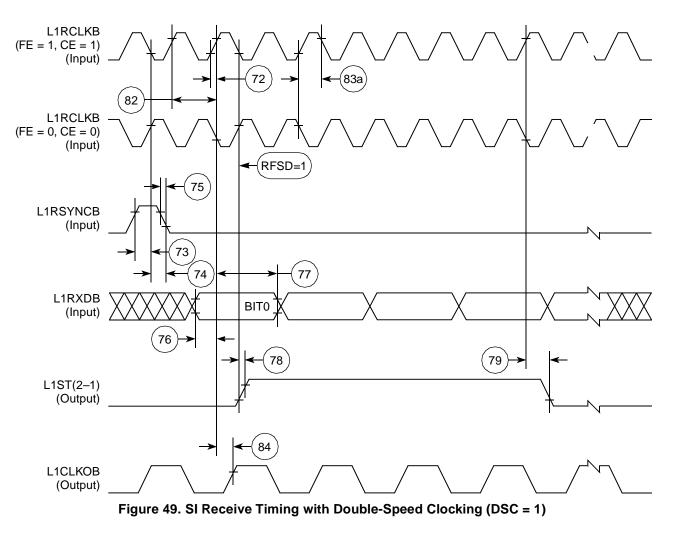
Num	Characteristic	All Freq	Unit	
num	Characteristic	Min	Мах	Unit
40	DREQ setup time to clock high	7	—	ns
41	DREQ hold time from clock high ¹	TBD	—	ns
42	SDACK assertion delay from clock high	_	12	ns
43	SDACK negation delay from clock low	_	12	ns
44	SDACK negation delay from TA low	_	20	ns
45	SDACK negation delay from clock high	_	15	ns
46	\overline{TA} assertion to rising edge of the clock setup time (applies to external \overline{TA})	7	—	ns

¹ Applies to high-to-low mode (EDM = 1).

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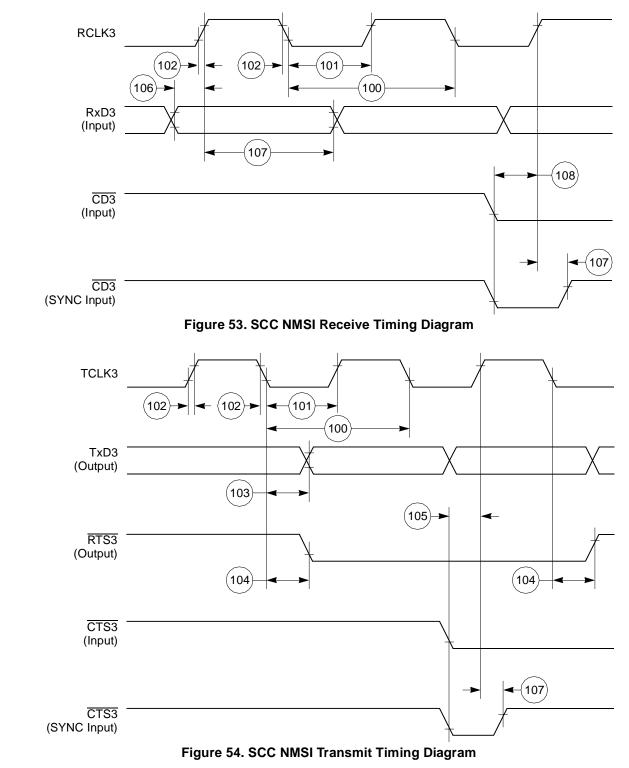
CPM Electrical Characteristics





CPM Electrical Characteristics







14 USB Electrical Characteristics

This section provides the AC timings for the USB interface.

14.1 USB Interface AC Timing Specifications

The USB Port uses the transmit clock on SCC1. Table 30 lists the USB interface timings.

Table 30. USB Interface AC Timing Specifications

Name	Characteristic	All Freq	Unit	
Name		Min	Max	onin
US1	USBCLK frequency of operation ¹ Low speed Full speed		6 48	
US4	USBCLK duty cycle (measured at 1.5 V)	45	55	%

¹ USBCLK accuracy should be ±500 ppm or better. USBCLK may be stopped to conserve power.

15 FEC Electrical Characteristics

This section provides the AC electrical specifications for the Fast Ethernet controller (FEC). Note that the timing specifications for the MII signals are independent of system clock frequency (part speed designation). Also, MII signals use TTL signal levels compatible with devices operating at either 5.0 or 3.3 V.

15.1 MII and Reduced MII Receive Signal Timing

The receiver functions correctly up to a MII_RX_CLK maximum frequency of 25 MHz + 1%. The reduced MII (RMII) receiver functions correctly up to a RMII_REFCLK maximum frequency of 50 MHz + 1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_RX_CLK frequency -1%.

Table 31 provides information on the MII receive signal timing.

Num	Characteristic	Min	Мах	Unit
M1	MII_RXD[3:0], MII_RX_DV, MII_RX_ER to MII_RX_CLK setup	5	_	ns
M2	MII_RX_CLK to MII_RXD[3:0], MII_RX_DV, MII_RX_ER hold	5	_	ns
M3	MII_RX_CLK pulse width high	35%	65%	MII_RX_CLK period
M4	MII_RX_CLK pulse width low	35%	65%	MII_RX_CLK period
M1_RMII	RMII_RXD[1:0], RMII_CRS_DV, RMII_RX_ERR to RMII_REFCLK setup	4	_	ns
M2_RMII	RMII_REFCLK to RMII_RXD[1:0], RMII_CRS_DV, RMII_RX_ERR hold	2		ns

Table 31. MII Receive Signal Timing



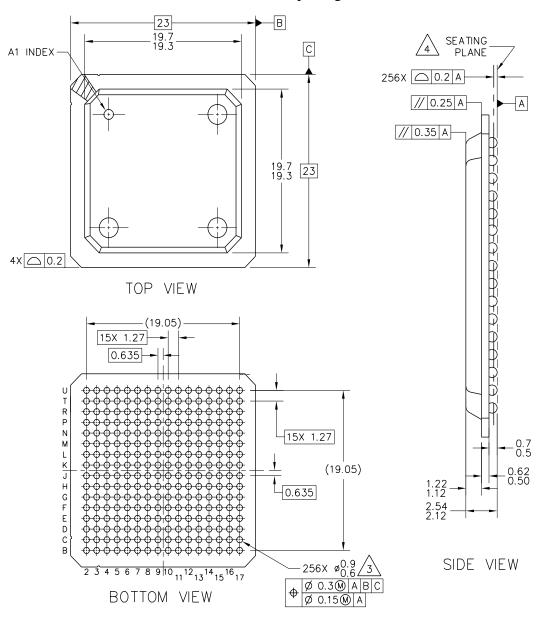
Name	Pin Number	Туре	
TDO, DSDO	P13	Output (5-V tolerant)	
MII1_CRS	U10	Input	
MII_MDIO	M13	Bidirectional (5-V tolerant)	
MII1_TX_EN, RMII1_TX_EN	U5	Output (5-V tolerant)	
MII1_COL	R10	Input	
V _{SSSYN}	E5	PLL analog GND	
V _{SSSYN1}	F6	PLL analog GND	
V _{DDSYN}	E6	PLL analog V _{DD}	
GND	H8, H9, H10, H11, J8, J9, J10, J11, K8, K9, K10, K11, L8, L9, L10, L11, U15	Power	
V _{DDL}	F7, F8, F9, F10, F11, H6, H13, J6, J13, K6, K13, L6, L13, N7, N8, N9, N10, N11	Power	
V _{DDH}	G7, G8, G9, G10, G11, G12, H7, H12, J7, J12, K7, K12, L7, L12, M7, M8, M9, M10, M11, M12	Power	
N/C	B17, T16, U2, U17	No connect	

Table 36. Pin Assignments—JEDEC Standard (continued)



16.2 Mechanical Dimensions of the PBGA Package

Figure 70 shows the mechanical dimensions of the PBGA package.



NOTES:

- 1. ALL DIMENSIONS ARE IN MILLIMETERS.
- 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
- 3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
- 4. DATUM A, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
- **Note:** Solder sphere composition is 95.5%Sn 45%Ag 0.5%Cu for MPC875/MPC870VRXXX. Solder sphere composition is 62%Sn 36%Pb 2%Ag for MPC875/MPC870ZTXXX.

Figure 70. Mechanical Dimensions and Bottom Surface Nomenclature of the PBGA Package

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