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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	66MHz
Co-Processors/DSP	Communications; CPM, Security; SEC
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (1), 10/100Mbps (2)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 100°C (TA)
Security Features	Cryptography
Package / Case	256-BBGA
Supplier Device Package	256-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc875cvr66

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



1 Overview

The MPC875/MPC870 is a versatile single-chip integrated microprocessor and peripheral combination that can be used in a variety of controller applications and communications and networking systems. The MPC875/MPC870 provides enhanced ATM functionality over that of other ATM-enabled members of the MPC860 family.

Table 1 shows the functionality supported by the MPC875/MPC870.

Part	Cache (Kbytes)		Ethernet		scc	SMC	IISB	Security
Tart	I Cache	D Cache	10BaseT	10/100	000	OMC	000	Engine
MPC875	8	8	1	2	1	1	1	Yes
MPC870	8	8	—	2		1	1	No

Table 1. MPC875/MPC870 Devices

2 Features

The MPC875/MPC870 is comprised of three modules that each use the 32-bit internal bus: a MPC8xx core, a system integration unit (SIU), and a communications processor module (CPM).

The following list summarizes the key MPC875/MPC870 features:

- Embedded MPC8xx core up to 133 MHz
- Maximum frequency operation of the external bus is 80 MHz (in 1:1 mode)
 - The 133-MHz core frequency supports 2:1 mode only
 - The 66-/80-MHz core frequencies support both the 1:1 and 2:1 modes
- Single-issue, 32-bit core (compatible with the Power Architecture definition) with thirty-two 32-bit general-purpose registers (GPRs)
 - The core performs branch prediction with conditional prefetch and without conditional execution
 - 8-Kbyte data cache and 8-Kbyte instruction cache (see Table 1)
 - Instruction cache is two-way, set-associative with 256 sets in 2 blocks
 - Data cache is two-way, set-associative with 256 sets
 - Cache coherency for both instruction and data caches is maintained on 128-bit (4-word) cache blocks
 - Caches are physically addressed, implement a least recently used (LRU) replacement algorithm, and are lockable on a cache block basis
 - MMUs with 32-entry TLB, fully associative instruction and data TLBs
 - MMUs support multiple page sizes of 4, 16, and 512 Kbytes, and 8 Mbytes; 16 virtual address spaces and 16 protection groups
 - Advanced on-chip emulation debug mode
- Up to 32-bit data bus (dynamic bus sizing for 8, 16, and 32 bits)



- Thirty-two address lines
- Memory controller (eight banks)
 - Contains complete dynamic RAM (DRAM) controller
 - Each bank can be a chip select or \overline{RAS} to support a DRAM bank
 - Up to 30 wait states programmable per memory bank
 - Glueless interface to DRAM, SIMMS, SRAM, EPROMs, Flash EPROMs, and other memory devices
 - DRAM controller programmable to support most size and speed memory interfaces
 - Four \overline{CAS} lines, four \overline{WE} lines, and one \overline{OE} line
 - Boot chip-select available at reset (options for 8-, 16-, or 32-bit memory)
 - Variable block sizes (32 Kbytes–256 Mbytes)
 - Selectable write protection
 - On-chip bus arbitration logic
- General-purpose timers
 - Four 16-bit timers or two 32-bit timers
 - Gate mode can enable/disable counting
 - Interrupt can be masked on reference match and event capture
- Two Fast Ethernet controllers (FEC)—Two 10/100 Mbps Ethernet/IEEE Std. 802.3® CDMA/CS that interface through MII and/or RMII interfaces
- System integration unit (SIU)
 - Bus monitor
 - Software watchdog
 - Periodic interrupt timer (PIT)
 - Clock synthesizer
 - Decrementer and time base
 - Reset controller
 - IEEE 1149.1[™] Std. test access port (JTAG)
- Security engine is optimized to handle all the algorithms associated with IPsec, SSL/TLS, SRTP, IEEE 802.11i® standard, and iSCSI processing. Available on the MPC875, the security engine contains a crypto-channel, a controller, and a set of crypto hardware accelerators (CHAs). The CHAs are:
 - Data encryption standard execution unit (DEU)
 - DES, 3DES
 - Two key (K1, K2, K1) or three key (K1, K2, K3)
 - ECB and CBC modes for both DES and 3DES
 - Advanced encryption standard unit (AESU)
 - Implements the Rijndael symmetric key cipher



Features

- ECB, CBC, and counter modes
- 128-, 192-, and 256-bit key lengths
- Message digest execution unit (MDEU)
 - SHA with 160- or 256-bit message digest
 - MD5 with 128-bit message digest
 - HMAC with either algorithm
- Master/slave logic, with DMA
 - 32-bit address/32-bit data
 - Operation at MPC8xx bus frequency
- Crypto-channel supporting multi-command descriptors
 - Integrated controller managing crypto-execution units
 - Buffer size of 256 bytes for each execution unit, with flow control for large data sizes
- Interrupts
 - Six external interrupt request (IRQ) lines
 - Twelve port pins with interrupt capability
 - Twenty-three internal interrupt sources
 - Programmable priority between SCCs
 - Programmable highest priority request
- Communications processor module (CPM)
 - RISC controller
 - Communication-specific commands (for example, GRACEFUL STOP TRANSMIT, ENTER HUNT MODE, and RESTART TRANSMIT)
 - Supports continuous mode transmission and reception on all serial channels
 - 8-Kbytes of dual-port RAM
 - Several serial DMA (SDMA) channels to support the CPM
 - Three parallel I/O registers with open-drain capability
- On-chip 16×16 multiply accumulate controller (MAC)
 - One operation per clock (two-clock latency, one-clock blockage)
 - MAC operates concurrently with other instructions
 - FIR loop—Four clocks per four multiplies
- Four baud-rate generators
 - Independent (can be connected to SCC or SMC)
 - Allows changes during operation
 - Autobaud support option
- SCC (serial communication controller)
 - Ethernet/IEEE 802.3® standard, supporting full 10-Mbps operation
 - HDLC/SDLC



Features

- HDLC bus (implements an HDLC-based local area network (LAN))
- Asynchronous HDLC to support point-to-point protocol (PPP)
- AppleTalk
- Universal asynchronous receiver transmitter (UART)
- Synchronous UART
- Serial infrared (IrDA)
- Binary synchronous communication (BISYNC)
- Totally transparent (bit streams)
- Totally transparent (frame based with optional cyclic redundancy check (CRC))
- SMC (serial management channel)
 - UART (low-speed operation)
 - Transparent
- Universal serial bus (USB)—Supports operation as a USB function endpoint, a USB host controller, or both for testing purposes (loopback diagnostics)
 - USB 2.0 full-/low-speed compatible
 - The USB function mode has the following features:
 - Four independent endpoints support control, bulk, interrupt, and isochronous data transfers
 - CRC16 generation and checking
 - CRC5 checking
 - NRZI encoding/decoding with bit stuffing
 - 12- or 1.5-Mbps data rate
 - Flexible data buffers with multiple buffers per frame
 - Automatic retransmission upon transmit error
 - The USB host controller has the following features:
 - Supports control, bulk, interrupt, and isochronous data transfers
 - CRC16 generation and checking
 - NRZI encoding/decoding with bit stuffing
 - Supports both 12- and 1.5-Mbps data rates (automatic generation of preamble token and data rate configuration). Note that low-speed operation requires an external hub.
 - Flexible data buffers with multiple buffers per frame
 - Supports local loopback mode for diagnostics (12 Mbps only)
- Serial peripheral interface (SPI)
 - Supports master and slave modes
 - Supports multiple-master operation on the same bus
- Inter-integrated circuit (I²C) port
 - Supports master and slave modes
 - Supports a multiple-master environment

NP

Thermal Characteristics

Rating	Symbol	Value	Unit
Temperature ¹ (standard)	T _{A(min)}	0	°C
	T _{J(max)}	95	°C
Temperature (extended)	T _{A(min)}	-40	°C
	T _{J(max)}	100	°C

Table 3	. Operating	Temperatures
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¹ Minimum temperatures are guaranteed as ambient temperature, T_A. Maximum temperatures are guaranteed as junction temperature, T_J.

This device contains circuitry protecting against damage due to high-static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{DDH}).

4 Thermal Characteristics

Table 4 shows the thermal characteristics for the MPC875/MPC870.

Rating	Er	Environment			Unit
Junction-to-ambient ¹	Natural convection	Single-layer board (1s)	$R_{\theta JA}^2$	43	°C/W
		Four-layer board (2s2p)	$R_{\theta JMA}{}^3$	29	
	Airflow (200 ft/min)	Single-layer board (1s)	$R_{\theta JMA}{}^3$	36	
		Four-layer board (2s2p)	$R_{\theta JMA}{}^3$	26	
Junction-to-board ⁴			R _{θJB}	20	
Junction-to-case ⁵			$R_{\theta JC}$	10	
Junction-to-package top ⁶	Natural convection		Ψ_{JT}	2	
	Airflow (200 ft/min)		Ψ_{JT}	2	1

Table 4. MPC875/MPC870 Thermal Resistance Data

¹ Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.

² Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.

³ Per JEDEC JESD51-6 with the board horizontal.

- ⁴ Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- ⁵ Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature. For exposed pad packages where the pad would be expected to be soldered, junction-to-case thermal resistance is a simulated value from the junction to the exposed pad without contact resistance.

⁶ Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2.



11 Bus Signal Timing

The maximum bus speed supported by the MPC875/MPC870 is 80 MHz. Higher-speed parts must be operated in half-speed bus mode (for example, an MPC875/MPC870 used at 133 MHz must be configured for a 66 MHz bus). Table 8 shows the frequency ranges for standard part frequencies in 1:1 bus mode, and Table 9 shows the frequency ranges for standard part frequencies in 2:1 bus mode.

Part Frequency		MHz	80 MHz		
		Max	Min	Max	
Core frequency	40	66.67	40	80	
Bus frequency	40	66.67	40	80	

Table 8. Frequency Ranges for Standard Part Frequencies (1:1 Bus Mode)

Table 9. Frequency Ranges for Standard Part Frequencies (2:1 Bus Mode)

Part Frequency		66 MHz		80 MHz		133 MHz	
		Max	Min	Max	Min	Max	
Core frequency	40	66.67	40	80	40	133	
Bus frequency	20	33.33	20	40	20	66	

Table 10 provides the bus operation timing for the MPC875/MPC870 at 33, 40, 66, and 80 MHz.

The timing for the MPC875/MPC870 bus shown Table 10, assumes a 50-pF load for maximum delays and a 0-pF load for minimum delays. CLKOUT assumes a 100-pF load maximum delay

Table 10. Bus Operation Timings

Num	Charactoristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
Num	Characteristic	Min	Max	Min	Мах	Min	Max	Min	Max	Unit
B1	Bus period (CLKOUT), see Table 8	—	—	—	_	—	—	—	_	ns
B1a	EXTCLK to CLKOUT phase skew—If CLKOUT is an integer multiple of EXTCLK, then the rising edge of EXTCLK is aligned with the rising edge of CLKOUT. For a non-integer multiple of EXTCLK, this synchronization is lost, and the rising edges of EXTCLK and CLKOUT have a continuously varying phase skew.	-2	+2	-2	+2	-2	+2	-2	+2	ns
B1b	CLKOUT frequency jitter peak-to-peak	—	1	—	1	_	1	—	1	ns
B1c	Frequency jitter on EXTCLK		0.50	_	0.50	_	0.50	_	0.50	%
B1d	CLKOUT phase jitter peak-to-peak for OSCLK \ge 15 MHz	—	4	—	4	_	4	—	4	ns
	CLKOUT phase jitter peak-to-peak for OSCLK < 15 MHz		5		5		5		5	ns



Bus Signal Timing



Figure 17. External Bus Write Timing (GPCM Controlled—TRLX = 0, CSNT = 1)



Figure 20 provides the timing for the asynchronous asserted UPWAIT signal controlled by the UPM.



Figure 20. Asynchronous UPWAIT Asserted Detection in UPM Handled Cycles Timing

Figure 21 provides the timing for the asynchronous negated UPWAIT signal controlled by the UPM.



Figure 21. Asynchronous UPWAIT Negated Detection in UPM Handled Cycles Timing





Figure 43. SDACK Timing Diagram—Peripheral Write, Externally-Generated TA



13.3 Baud Rate Generator AC Electrical Specifications

Table 19 provides the baud rate generator timings as shown in Figure 46.

Table 19. Baud Rate Generator Timing

Num	Characteristic		All Frequencies		
			Мах	Onit	
50	BRGO rise and fall time	_	10	ns	
51	BRGO duty cycle	40	60	%	
52	BRGO cycle	40	—	ns	



Figure 46. Baud Rate Generator Timing Diagram

13.4 Timer AC Electrical Specifications

Table 20 provides the general-purpose timer timings as shown in Figure 47.

Table	20.	Timer	Timing
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Num	Characteristic	All Freq	Unit	
		Min	Мах	Unit
61	TIN/TGATE rise and fall time	10	—	ns
62	TIN/TGATE low time	1	—	clk
63	TIN/TGATE high time	2	—	clk
64	TIN/TGATE cycle time	3	—	clk
65	CLKO low to TOUT valid	3	25	ns





Figure 47. CPM General-Purpose Timers Timing Diagram

13.5 Serial Interface AC Electrical Specifications

Table 21 provides the serial interface (SI) timings as shown in Figure 48 through Figure 52.

Num	Characteristic	All Fre	Unit	
Num	Characteristic	Min	Max	Unit
70	L1RCLKB, L1TCLKB frequency (DSC = 0) ^{1, 2}	—	SYNCCLK/2.5	MHz
71	L1RCLKB, L1TCLKB width low $(DSC = 0)^2$	P + 10	_	ns
71a	L1RCLKB, L1TCLKB width high (DSC = 0) ³	P + 10	—	ns
72	L1TXDB, L1ST1 and L1ST2, L1RQ, L1CLKO rise/fall time	—	15.00	ns
73	L1RSYNCB, L1TSYNCB valid to L1CLKB edge (SYNC setup time)	20.00	—	ns
74	L1CLKB edge to L1RSYNCB, L1TSYNCB, invalid (SYNC hold time)	35.00	—	ns
75	L1RSYNCB, L1TSYNCB rise/fall time	—	15.00	ns
76	L1RXDB valid to L1CLKB edge (L1RXDB setup time)	17.00	—	ns
77	L1CLKB edge to L1RXDB invalid (L1RXDB hold time)	13.00	—	ns
78	L1CLKB edge to L1ST1 and L1ST2 valid ⁴	10.00	45.00	ns
78A	L1SYNCB valid to L1ST1 and L1ST2 valid	10.00	45.00	ns
79	L1CLKB edge to L1ST1 and L1ST2 invalid	10.00	45.00	ns
80	L1CLKB edge to L1TXDB valid	10.00	55.00	ns
80A	L1TSYNCB valid to L1TXDB valid ⁴	10.00	55.00	ns
81	L1CLKB edge to L1TXDB high impedance	0.00	42.00	ns
82	L1RCLKB, L1TCLKB frequency (DSC = 1)	_	16.00 or SYNCCLK/2	MHz
83	L1RCLKB, L1TCLKB width low (DSC = 1)	P + 10	_	ns

Table 21. SI Timing









SCC in NMSI Mode Electrical Specifications 13.6

Table 22 provides the NMSI external clock timing.

Table 22. NMSI Externa	Clock Timing
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Num	Characteristic	All Frequencies		Unit
Num	Characteristic	Min	Мах	Onit
100	RCLK3 and TCLK3 width high ¹	1/SYNCCLK	_	ns
101	RCLK3 and TCLK3 width low	1/SYNCCLK + 5	_	ns
102	RCLK3 and TCLK3 rise/fall time	—	15.00	ns
103	TXD3 active delay (from TCLK3 falling edge)	0.00	50.00	ns
104	RTS3 active/inactive delay (from TCLK3 falling edge)	0.00	50.00	ns
105	CTS3 setup time to TCLK3 rising edge	5.00	_	ns
106	RXD3 setup time to RCLK3 rising edge	5.00	_	ns
107	RXD3 hold time from RCLK3 rising edge ²	5.00	_	ns
108	CD3 setup time to RCLK3 rising edge	5.00	—	ns

¹ The ratios SYNCCLK/RCLK3 and SYNCCLK/TCLK3 must be greater than or equal to 2.25/1.
² Also applies to CD and CTS hold time when they are used as external SYNC signals.

Table 23 provides the NMSI internal clock timing.

Table 23. NMSI Internal Clock Timing

Num	Characteristic	All Fre	Unit	
	Cildiacteristic	Min	Мах	Unit
100	RCLK3 and TCLK3 frequency ¹	0.00	SYNCCLK/3	MHz
102	RCLK3 and TCLK3 rise/fall time	_	_	ns
103	TXD3 active delay (from TCLK3 falling edge)	0.00	30.00	ns
104	RTS3 active/inactive delay (from TCLK3 falling edge)	0.00	30.00	ns
105	CTS3 setup time to TCLK3 rising edge	40.00	—	ns
106	RXD3 setup time to RCLK3 rising edge	40.00	—	ns
107	RXD3 hold time from RCLK3 rising edge ²	0.00	—	ns
108	CD3 setup time to RCLK3 rising edge	40.00	—	ns

The ratios SYNCCLK/RCLK3 and SYNCCLK/TCLK3 must be greater or equal to 3/1.
Also applies to CD and CTS hold time when they are used as external SYNC signals.







Figure 55. HDLC Bus Timing Diagram

13.7 Ethernet Electrical Specifications

Table 24 provides the Ethernet timings as shown in Figure 56 through Figure 58.

Table 24. Ethernet Timing

Num	Characteristic	All Frequencies		l lm:t
		Min	Мах	Unit
120	CLSN width high	40	_	ns
121	RCLK3 rise/fall time	—	15	ns
122	RCLK3 width low	40	_	ns
123	RCLK3 clock period ¹	80	120	ns
124	RXD3 setup time	20	_	ns
125	RXD3 hold time	5	_	ns
126	RENA active delay (from RCLK3 rising edge of the last data bit)	10	_	ns
127	RENA width low	100	_	ns
128	TCLK3 rise/fall time	—	15	ns
129	TCLK3 width low	40	_	ns
130	TCLK3 clock period ¹	99	101	ns
131	TXD3 active delay (from TCLK3 rising edge)	_	50	ns
132	TXD3 inactive delay (from TCLK3 rising edge)	6.5	50	ns
133	TENA active delay (from TCLK3 rising edge)	10	50	ns
134	TENA inactive delay (from TCLK3 rising edge)	10	50	ns



13.10 SPI Slave AC Electrical Specifications

Table 27 provides the SPI slave timings as shown in Figure 62 and Figure 63.

Table 27. SPI Slave Timing

Num	Characteristic	All Freq	Unit	
	Cildiacteristic		Мах	Onit
170	Slave cycle time	2	_	t _{cyc}
171	Slave enable lead time	15	_	ns
172	Slave enable lag time	15	_	ns
173	Slave clock (SPICLK) high or low time	1	_	t _{cyc}
174	Slave sequential transfer delay (does not require deselect)	1	_	t _{cyc}
175	Slave data setup time (inputs)	20	_	ns
176	Slave data hold time (inputs)	20	_	ns
177	Slave access time	—	50	ns









13.11 I²C AC Electrical Specifications

Table 28 provides the I^2C (SCL < 100 kHz) timings.

Table 28	. I ² C	Timing	(SCL <	100 kHz)
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Num	Characteristic	All Frequencies		Unit
Num	Characteristic	Min	Мах	Onic
200	SCL clock frequency (slave)	0	100	kHz
200	SCL clock frequency (master) ¹	1.5	100	kHz
202	Bus free time between transmissions	4.7	_	μs
203	Low period of SCL	4.7	_	μs
204	High period of SCL	4.0	-	μs
205	Start condition setup time	4.7	-	μs
206	Start condition hold time	4.0	-	μs
207	Data hold time	0		μs
208	Data setup time	250		ns
209	SDL/SCL rise time	_	1	μs



Figure 65 shows MII receive signal timing.



Figure 65. MII Receive Signal Timing Diagram

15.2 MII and Reduced MII Transmit Signal Timing

The transmitter functions correctly up to a MII_TX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_TX_CLK frequency -1%.

Table 32 provides information on the MII transmit signal timing.

Table 3	2. MII	Transmit	Signal	Timing
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Num	Characteristic	Min	Max	Unit
M5	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER invalid	5	_	ns
M6	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER valid	—	25	ns
M7	MII_TX_CLK pulse width high	35%	65%	MII_TX_CLK period
M8	MII_TX_CLK pulse width low	35%	65%	MII_TX_CLK period
M20_RMII	RMII_TXD[1:0], RMII_TX_EN to RMII_REFCLK setup	4	_	ns
M21_RMII	RMII_TXD[1:0], RMII_TX_EN data hold from RMII_REFCLK rising edge	2	—	ns



Name	Pin Number	Туре
PB30, SPICLK	Т17	Bidirectional (Optional: open-drain) (5-V tolerant)
PB29, SPIMOSI	R17	Bidirectional (Optional: open-drain) (5-V tolerant)
PB28, SPIMISO, BRGO4	R14	Bidirectional (Optional: open-drain) (5-V tolerant)
PB27, I2CSDA, BRGO1	N13	Bidirectional (Optional: open-drain)
PB26, I2CSCL, BRGO2	N12	Bidirectional (Optional: open-drain)
PB25, SMTXD1	U13	Bidirectional (Optional: open-drain) (5-V tolerant)
PB24, SMRXD1	T12	Bidirectional (Optional: open-drain) (5-V tolerant)
PB23, SDACK1, SMSYN1	U12	Bidirectional (Optional: open-drain)
PB19, MII1-RXD3, RTS4	T11	Bidirectional (Optional: open-drain)
PC15, DREQ0, L1ST1	R15	Bidirectional (5-V tolerant)
PC13, MII1-TXD3, SDACK1	U9	Bidirectional (5-V tolerant)
PC12, MII1-TXD2, TOUT1	T15	Bidirectional (5-V tolerant)
PC11, USBRXP	P12	Bidirectional
PC10, USBRXN, TGATE1	U11	Bidirectional
PC7, CTS4, L1TSYNCB, USBTXP	Т10	Bidirectional (5-V tolerant)
PC6, CD4, L1RSYNCB, USBTXN	P10	Bidirectional (5-V tolerant)
PD8, RXD4, MII-MDC, RMII-MDC	Т3	Bidirectional (5-V tolerant)
PE31, CLK8, L1TCLKB, MII1-RXCLK	P9	Bidirectional (Optional: open-drain)
PE30, L1RXDB, MII1-RXD2	R8	Bidirectional (Optional: open-drain)

Table 36. Pin Assignments—JEDEC Standard (continued)



16.2 Mechanical Dimensions of the PBGA Package

Figure 70 shows the mechanical dimensions of the PBGA package.



NOTES:

- 1. ALL DIMENSIONS ARE IN MILLIMETERS.
- 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
- 3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
- 4. DATUM A, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
- **Note:** Solder sphere composition is 95.5%Sn 45%Ag 0.5%Cu for MPC875/MPC870VRXXX. Solder sphere composition is 62%Sn 36%Pb 2%Ag for MPC875/MPC870ZTXXX.

Figure 70. Mechanical Dimensions and Bottom Surface Nomenclature of the PBGA Package

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