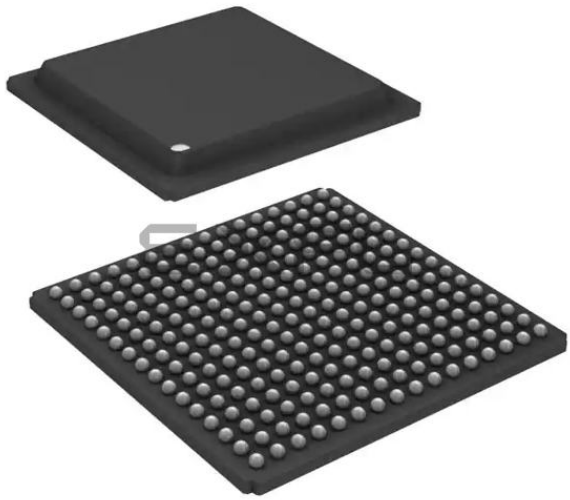

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	133MHz
Co-Processors/DSP	Communications; CPM, Security; SEC
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (1), 10/100Mbps (2)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TA)
Security Features	Cryptography
Package / Case	256-BBGA
Supplier Device Package	256-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc875zt133

- The MPC875 has a time-slot assigner (TSA) that supports one TDM bus (TDMb)
  - Allows SCC and SMC to run in multiplexed and/or non-multiplexed operation
  - Supports T1, CEPT, PCM highway, ISDN basic rate, ISDN primary rate, user-defined
  - 1- or 8-bit resolution
  - Allows independent transmit and receive routing, frame synchronization, and clocking
  - Allows dynamic changes
  - Can be internally connected to two serial channels (one SCC and one SMC)
- PCMCIA interface
  - Master (socket) interface, release 2.1-compliant
  - Supports one independent PCMCIA socket on the MPC875/MPC870
  - Eight memory or I/O windows supported
- Debug interface
  - Eight comparators: four operate on instruction address, two operate on data address, and two operate on data
  - Supports conditions: = ≠ < >
  - Each watchpoint can generate a break point internally
- Normal high and normal low power modes to conserve power
- 1.8-V core and 3.3-V I/O operation with 5-V TTL compatibility
- The MPC875/MPC870 comes in a 256-pin ball grid array (PBGA) package

The MPC875 block diagram is shown in Figure 1.

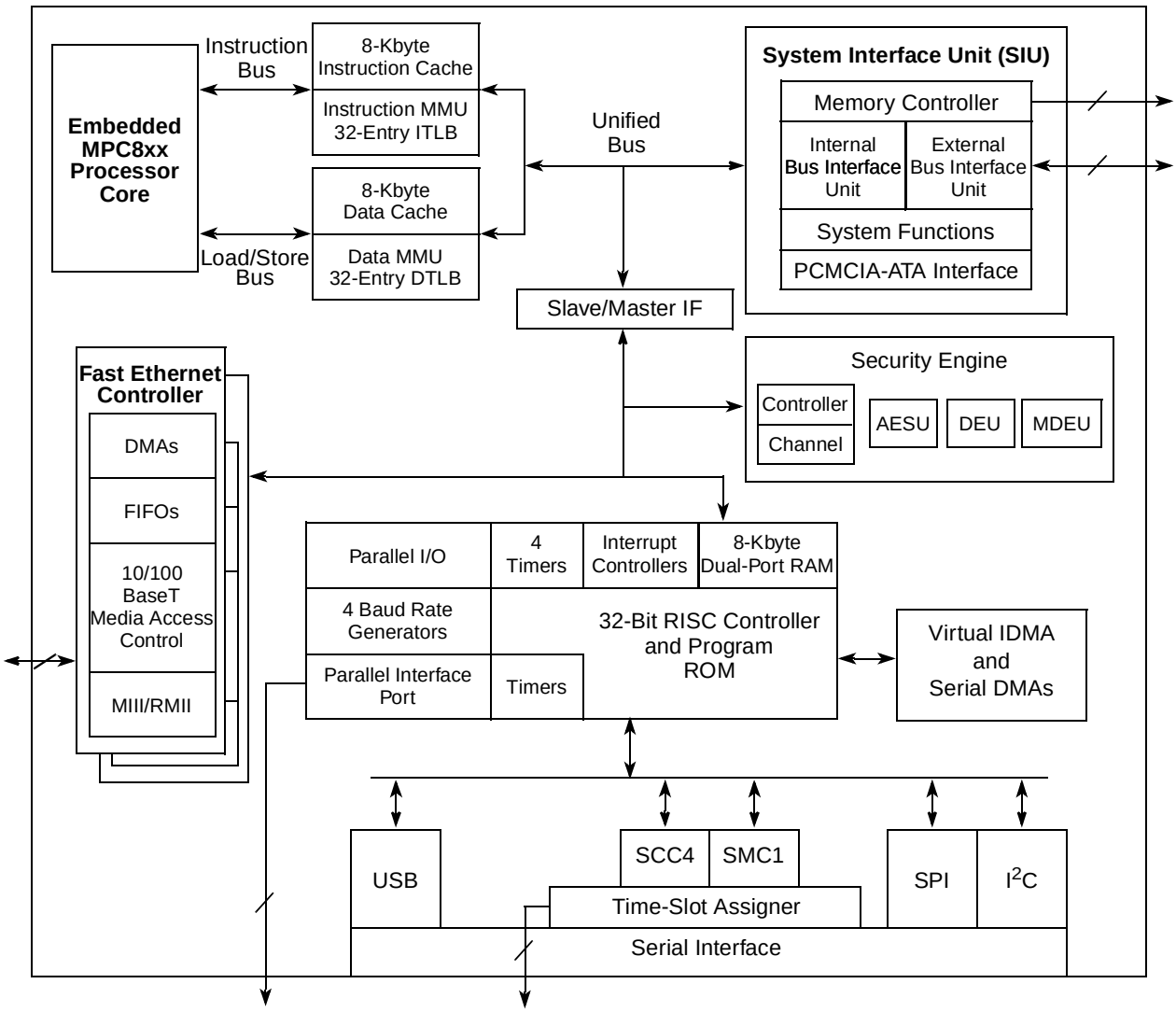


Figure 1. MPC875 Block Diagram

Table 6. DC Electrical Specifications (continued)

Characteristic	Symbol	Min	Max	Unit
Output high voltage, I_{OH} = –2.0 mA, V_{DDH} = 3.0 V (except XTAL and open-drain pins)	V_{OH}	2.4	—	V
Output low voltage I_{OL} = 2.0 mA (CLKOUT) I_{OL} = 3.2 mA[5] I_{OL} = 5.3 mA[6] I_{OL} = 7.0 mA (TXD1/PA14, TXD2/PA12) I_{OL} = 8.9 mA ($\overline{TS}$, $\overline{TA}$, $\overline{TEA}$, $\overline{BI}$, $\overline{BB}$, $\overline{HRESET}$, $\overline{SRESET}$)	V_{OL}	—	0.5	V

1 The difference between V_{DDL} and V_{DDSYN} cannot be more than 100 mV.

2 The signals PA[0:15], PB[14:31], PC[4:15], PD[3:15], PE(14:31), TDI, TDO, TCK, $\overline{TRST}$, TMS, MII1_TXEN, and MII_MDIO are 5-V tolerant. The minimum voltage is still 2.0 V.

3 V_{IL}(max) for the I^2C interface is 0.8 V rather than the 1.5 V as specified in the I^2C standard.

4 Input capacitance is periodically sampled.

5 A(0:31), TSIZ0/$\overline{REG}$, TSIZ1, D(0:31), $\overline{IRQ}$(2:4), $\overline{IRQ6}$, RD/$\overline{WR}$, $\overline{BURST}$, IP_B(0:1), PA(0:4), PA(6:7), PA(10:11), PA15, PB19, PB(23:31), PC(6:7), PC(10:13), PC15, PD8, PE(14:31), MII1_CRS, MII_MDIO, MII1_TXEN, and MII1_COL.

6 $\overline{BDIP}$/$\overline{GPL\_B}$(5), $\overline{BR}$, $\overline{BG}$, FRZ/$\overline{IRQ6}$, $\overline{CS}$(0:7), $\overline{WE}$(0:3), $\overline{BS}$_A(0:3), $\overline{GPL\_A0}$/$\overline{GPL\_B0}$, $\overline{OE}$/$\overline{GPL\_A1}$/$\overline{GPL\_B1}$, $\overline{GPL\_A}$(2:3)/$\overline{GPL\_B}$(2:3)/$\overline{CS}$(2:3), UPWAITA/$\overline{GPL\_A4}$, UPWAITB/$\overline{GPL\_B4}$, $\overline{GPL\_A5}$, ALE_A, $\overline{CE1}$_A, $\overline{CE2}$_A, OP(0:3), and BADDR(28:30).

7 Thermal Calculation and Measurement

For the following discussions, $P_D = (V_{DDL} \times I_{DDL}) + P_{I/O}$, where $P_{I/O}$ is the power dissipation of the I/O drivers.

NOTE

The V_{DDSYN} power dissipation is negligible.

7.1 Estimation with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J, in °C can be obtained from the following equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_A = ambient temperature (°C)

$R_{\theta JA}$ = package junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in package

The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. However, the answer is only an estimate; test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

One consequence of multiple power supplies is that when power is initially applied, the voltage rails ramp up at different rates. The rates depend on the nature of the power supply, the type of load on each power supply, and the manner in which different voltages are derived. The following restrictions apply:

- V_{DDL} must not exceed V_{DDH} during power up and power down
- V_{DDL} must not exceed 1.9 V, and V_{DDH} must not exceed 3.465 V

These cautions are necessary for the long-term reliability of the part. If they are violated, the electrostatic discharge (ESD) protection diodes are forward-biased, and excessive current can flow through these diodes. If the system power supply design does not control the voltage sequencing, the circuit shown in Figure 4 can be added to meet these requirements. The MUR420 Schottky diodes control the maximum potential difference between the external bus and core power supplies on power up, and the 1N5820 diodes regulate the maximum potential difference on power down.

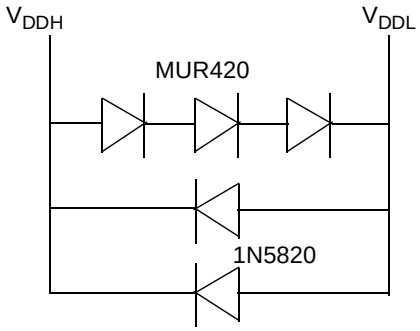


Figure 4. Example Voltage Sequencing Circuit

9 Mandatory Reset Configurations

The MPC875/MPC870 requires a mandatory configuration during reset.

If hardware reset configuration word (HRCW) is enabled, the HRCW[DBGC] value needs to be set to binary X1 in the HRCW and the SIUMCR[DBGC] should be programmed with the same value in the boot code after reset. This can be done by asserting the $\overline{\text{RSTCONF}}$ during $\overline{\text{HRESET}}$ assertion.

If HRCW is disabled, the SIUMCR[DBGC] should be programmed with binary X1 in the boot code after reset by negating the $\overline{\text{RSTCONF}}$ during the $\overline{\text{HRESET}}$ assertion.

The MBMR[GPLB4DIS], PAPAR, PADIR, PBPAR, PBDIR, PCPAR, and PCDIR need to be configured with the mandatory values in Table 7 in the boot code after the reset is negated.

Table 7. Mandatory Reset Configuration of MPC875/MPC870

Register/Configuration	Field	Value (Binary)
HRCW (Hardware reset configuration word)	HRCW[DBGC]	X1
SIUMCR (SIU module configuration register)	SIUMCR[DBGC]	X1
MBMR (Machine B mode register)	MBMR[GPLB4DIS}	0
PAPAR (Port A pin assignment register)	PAPAR[5:9] PAPAR[12:13]	0

Table 7. Mandatory Reset Configuration of MPC875/MPC870 (continued)

Register/Configuration	Field	Value (Binary)
PADIR (Port A data direction register)	PADIR[5:9] PADIR[12:13]	0
PBPAR (Port B pin assignment register)	PBPAR[14:18] PBPAR[20:22]	0
PBDIR (Port B data direction register)	PBDIR[14:8] PBDIR[20:22]	0
PCPAR (Port C pin assignment register)	PCPAR[4:5] PCPAR[8:9] PCPAR[14]	0
PCDIR (Port C data direction register)	PCDIR[4:5] PCDIR[8:9] PCDIR[14]	0
PDPAR (Port D pin assignment register)	PDPAR[3:7] PDPAR[9:5]	0
PDDIR (Port D data direction register)	PDDIR[3:7] PDDIR[9:15]	0

10 Layout Practices

Each V_{DD} pin on the MPC875/MPC870 should be provided with a low-impedance path to the board's supply. Each GND pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The V_{DD} power supply should be bypassed to ground using at least four 0.1-µF bypass capacitors located as close as possible to the four sides of the package. Each board designed should be characterized and additional appropriate decoupling capacitors should be used if required. The capacitor leads and associated printed-circuit traces connecting to chip V_{DD} and GND should be kept to less than half an inch per capacitor lead. At a minimum, a four-layer board employing two inner layers as V_{DD} and GND planes should be used.

All output pins on the MPC875/MPC870 have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses. Maximum PC trace lengths of 6 inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the V_{DD} and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins. For more information, refer to Section 14.4.3, "Clock Synthesizer Power (V_{DDSYN}, V_{SSSYN}, V_{SSSYN1})," in the *MPC885 PowerQUICC™ Family Reference Manual*.

11 Bus Signal Timing

The maximum bus speed supported by the MPC875/MPC870 is 80 MHz. Higher-speed parts must be operated in half-speed bus mode (for example, an MPC875/MPC870 used at 133 MHz must be configured for a 66 MHz bus). Table 8 shows the frequency ranges for standard part frequencies in 1:1 bus mode, and Table 9 shows the frequency ranges for standard part frequencies in 2:1 bus mode.

Table 8. Frequency Ranges for Standard Part Frequencies (1:1 Bus Mode)

Part Frequency	66 MHz		80 MHz	
	Min	Max	Min	Max
Core frequency	40	66.67	40	80
Bus frequency	40	66.67	40	80

Table 9. Frequency Ranges for Standard Part Frequencies (2:1 Bus Mode)

Part Frequency	66 MHz		80 MHz		133 MHz	
	Min	Max	Min	Max	Min	Max
Core frequency	40	66.67	40	80	40	133
Bus frequency	20	33.33	20	40	20	66

Table 10 provides the bus operation timing for the MPC875/MPC870 at 33, 40, 66, and 80 MHz.

The timing for the MPC875/MPC870 bus shown Table 10, assumes a 50-pF load for maximum delays and a 0-pF load for minimum delays. CLKOUT assumes a 100-pF load maximum delay

Table 10. Bus Operation Timings

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B1	Bus period (CLKOUT), see Table 8	—	—	—	—	—	—	—	—	ns
B1a	EXTCLK to CLKOUT phase skew—If CLKOUT is an integer multiple of EXTCLK, then the rising edge of EXTCLK is aligned with the rising edge of CLKOUT. For a non-integer multiple of EXTCLK, this synchronization is lost, and the rising edges of EXTCLK and CLKOUT have a continuously varying phase skew.	–2	+2	–2	+2	–2	+2	–2	+2	ns
B1b	CLKOUT frequency jitter peak-to-peak	—	1	—	1	—	1	—	1	ns
B1c	Frequency jitter on EXTCLK	—	0.50	—	0.50	—	0.50	—	0.50	%
B1d	CLKOUT phase jitter peak-to-peak for OSCLK ≥ 15 MHz	—	4	—	4	—	4	—	4	ns
	CLKOUT phase jitter peak-to-peak for OSCLK < 15 MHz	—	5	—	5	—	5	—	5	ns

Figure 11 provides the timing for the input data controlled by the UPM for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

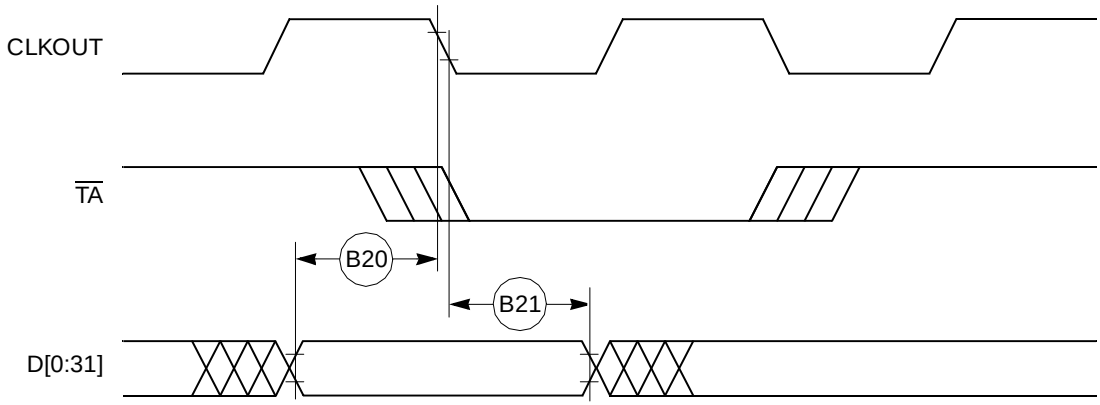


Figure 11. Input Data Timing when Controlled by UPM in the Memory Controller and DLT3 = 1

Figure 12 through Figure 15 provide the timing for the external bus read controlled by various GPCM factors.

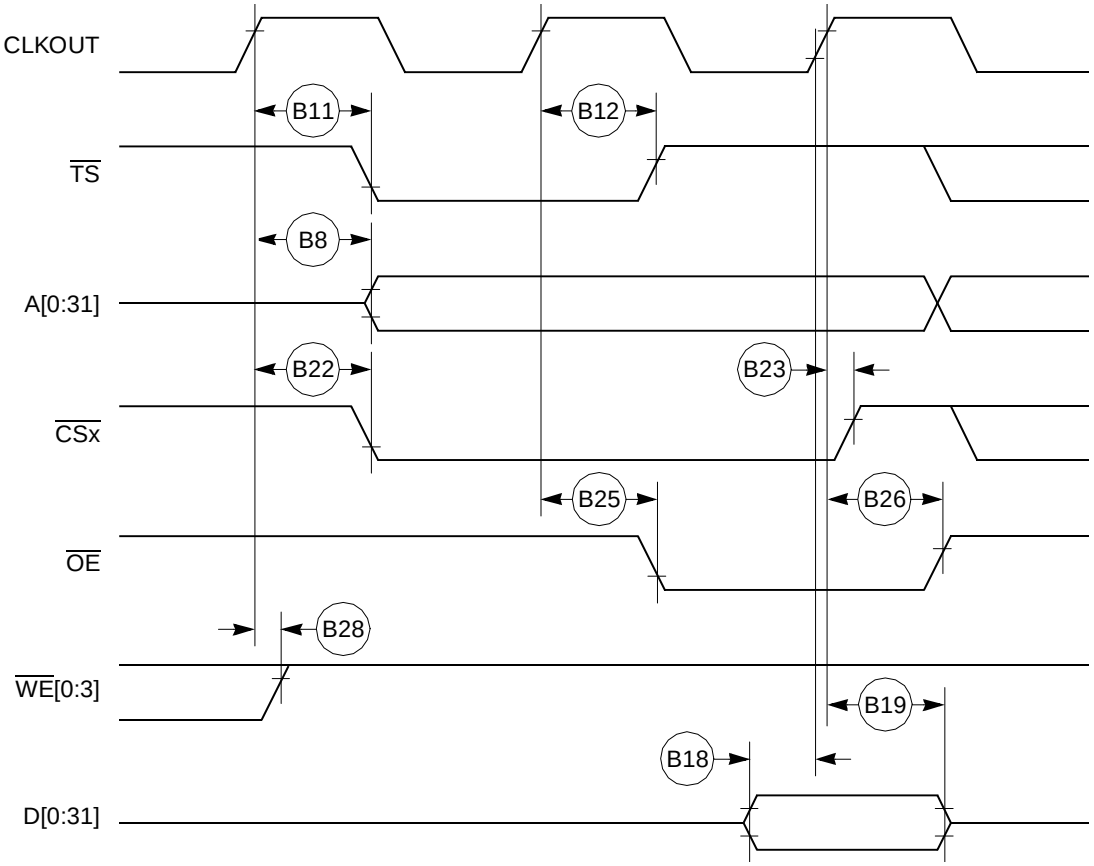


Figure 12. External Bus Read Timing (GPCM Controlled—ACS = 00)

Figure 16 through Figure 18 provide the timing for the external bus write controlled by various GPCM factors.

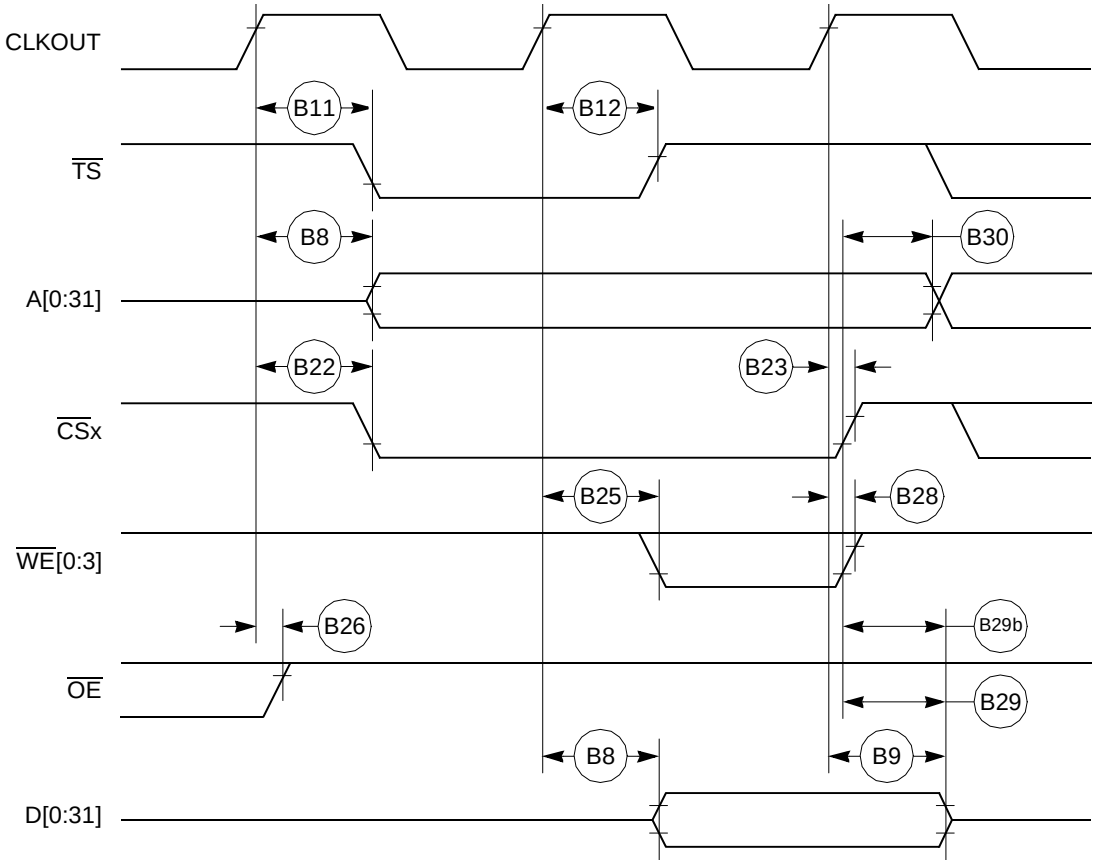


Figure 16. External Bus Write Timing (GPCM Controlled—TRLX = 0, CSNT = 0)

Figure 27 provides the PCMCIA access cycle timing for the external bus read.

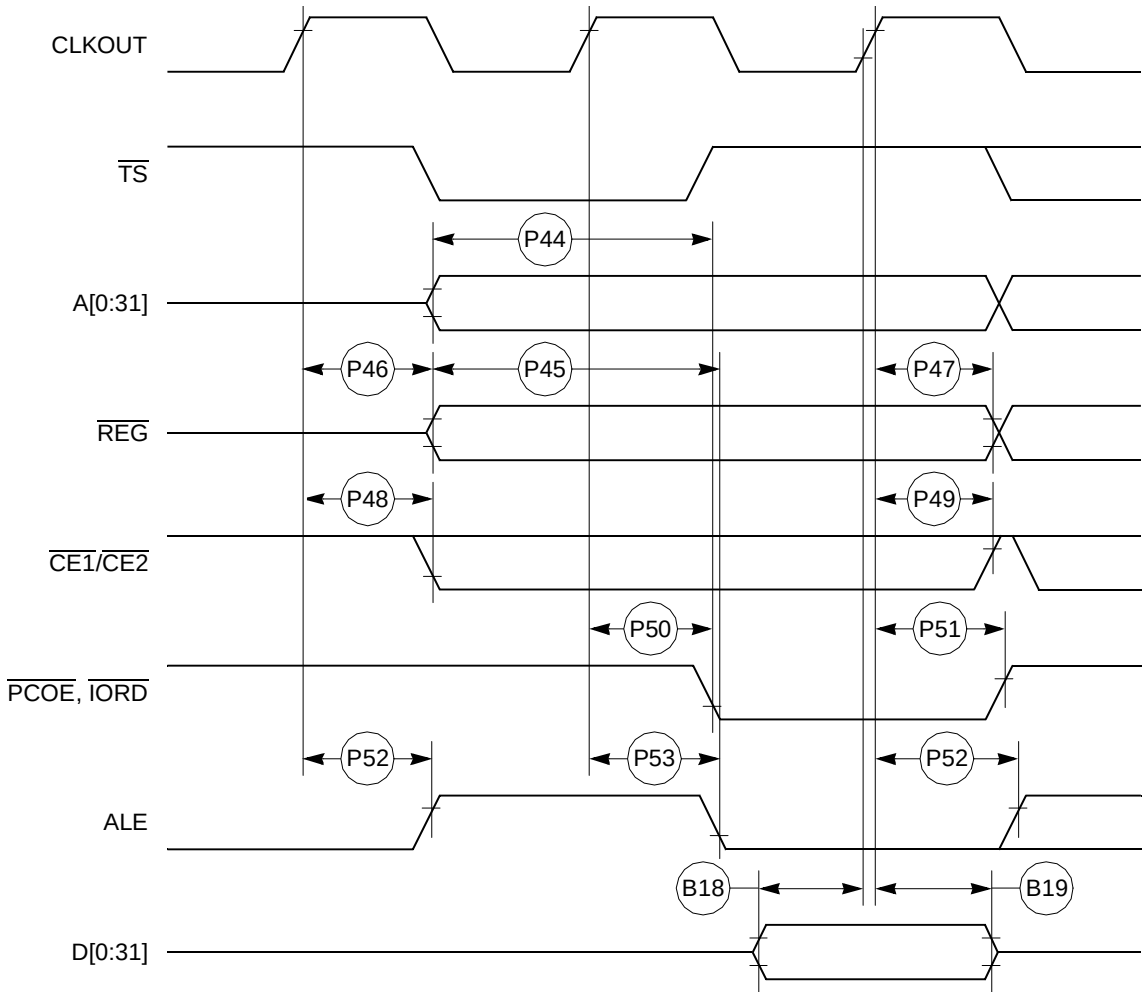


Figure 27. PCMCIA Access Cycles Timing External Bus Read

Figure 28 provides the PCMCIA access cycle timing for the external bus write.

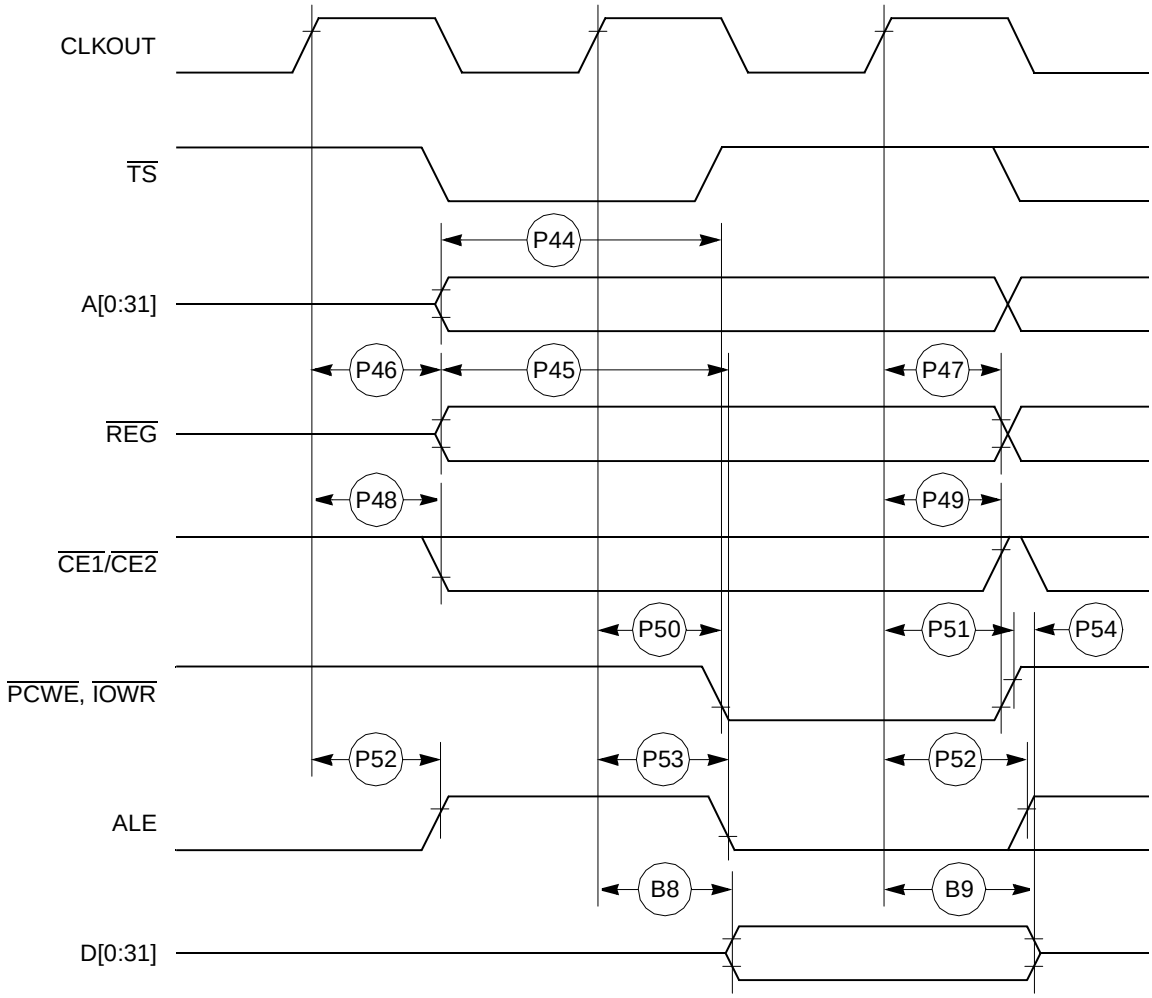


Figure 28. PCMCIA Access Cycles Timing External Bus Write

Figure 29 provides the PCMCIA WAIT signals detection timing.

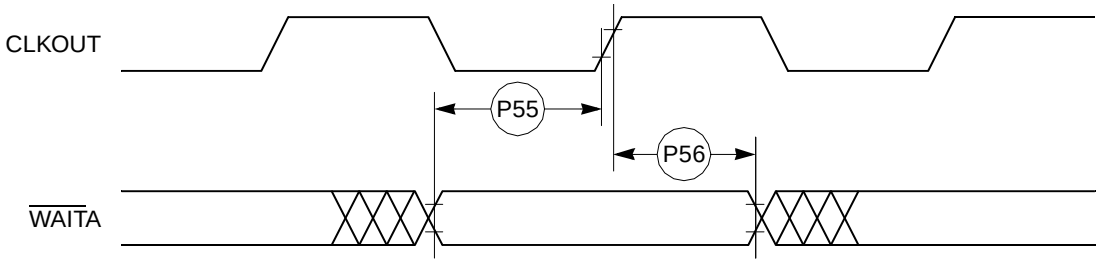


Figure 29. PCMCIA WAIT Signals Detection Timing

Table 13 shows the PCMCIA port timing for the MPC875/MPC870.

Table 13. PCMCIA Port Timing

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
P57	CLKOUT to OPx valid (MAX = 0.00 × B1 + 19.00)	—	19.00	—	19.00	—	19.00	—	19.00	ns
P58	$\overline{\text{HRESET}}$ negated to OPx drive[1] (MIN = 0.75 × B1 + 3.00)	25.70	—	21.70	—	14.40	—	12.40	—	ns
P59	IP_Xx valid to CLKOUT rising edge (MIN = 0.00 × B1 + 5.00)	5.00	—	5.00	—	5.00	—	5.00	—	ns
P60	CLKOUT rising edge to IP_Xx invalid (MIN = 0.00 × B1 + 1.00)	1.00	—	1.00	—	1.00	—	1.00	—	ns

1 OP2 and OP3 only.

Figure 30 provides the PCMCIA output port timing for the MPC875/MPC870.

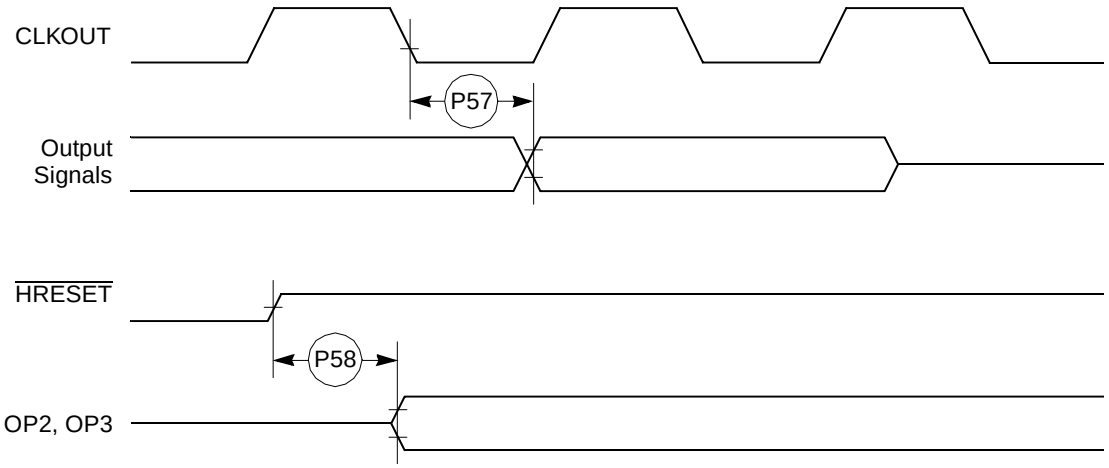


Figure 30. PCMCIA Output Port Timing

Figure 31 provides the PCMCIA input port timing for the MPC875/MPC870.

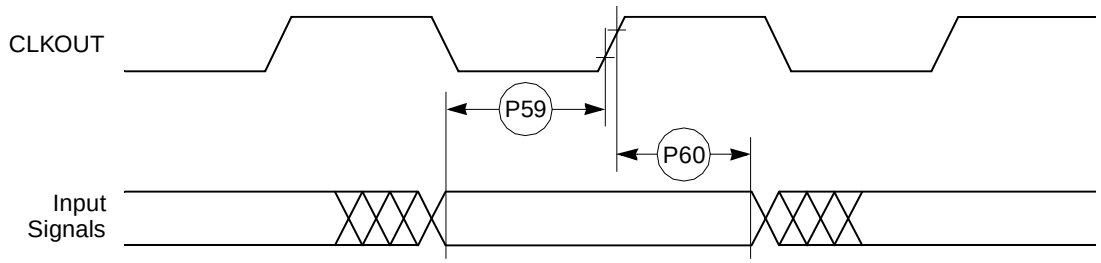


Figure 31. PCMCIA Input Port Timing

Table 14 shows the debug port timing for the MPC875/MPC870.

Table 14. Debug Port Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
D61	DSCK cycle time	$3 \times T_{CLOCKOUT}$		—
D62	DSCK clock pulse width	$1.25 \times T_{CLOCKOUT}$		—
D63	DSCK rise and fall times	0.00	3.00	ns
D64	DSDI input data setup time	8.00		ns
D65	DSDI data hold time	5.00		ns
D66	DSCK low to DSDO data valid	0.00	15.00	ns
D67	DSCK low to DSDO invalid	0.00	2.00	ns

Figure 32 provides the input timing for the debug port clock.

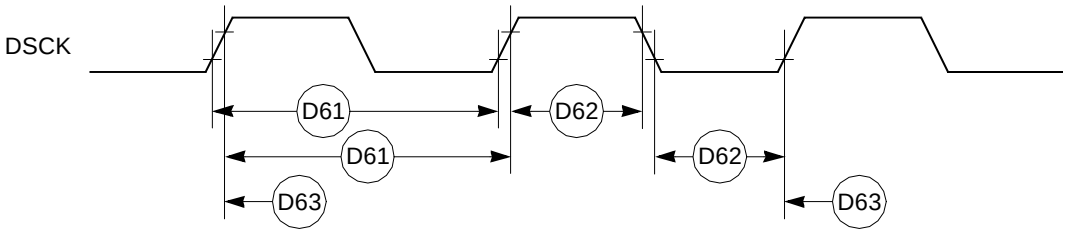


Figure 32. Debug Port Clock Input Timing

Figure 33 provides the timing for the debug port.

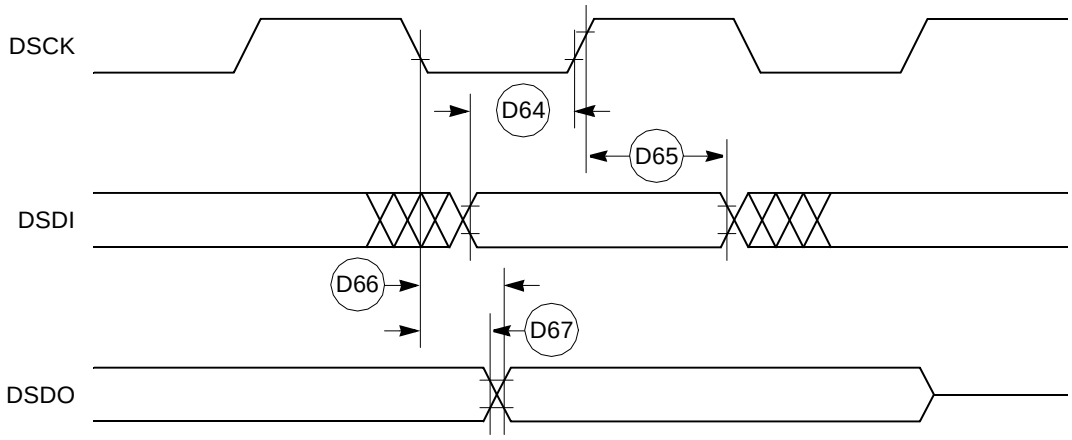


Figure 33. Debug Port Timings

Table 21. SI Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
83a	L1RCLKB, L1TCLKB width high (DSC = 1)[3]	P + 10	—	ns
84	L1CLKB edge to L1CLKOB valid (DSC = 1)	—	30.00	ns
85	$\overline{\text{L1RQB}}$ valid before falling edge of L1TSYNCB[4]	1.00	—	L1TCLK
86	L1GRB setup time[2]	42.00	—	ns
87	L1GRB hold time	42.00	—	ns
88	L1CLKB edge to L1SYNCB valid (FSD = 00) CNT = 0000, BYT = 0, DSC = 0)	—	0.00	ns

1 The ratio SYNCCLK/L1RCLKB must be greater than 2.5/1.
2 These specs are valid for IDL mode only.
3 Where P = 1/CLKOUT. Thus, for a 25-MHz CLKO1 rate, P = 40 ns.
4 These strobes and TxD on the first bit of the frame become valid after the L1CLKB edge or L1SYNCB, whichever comes later.

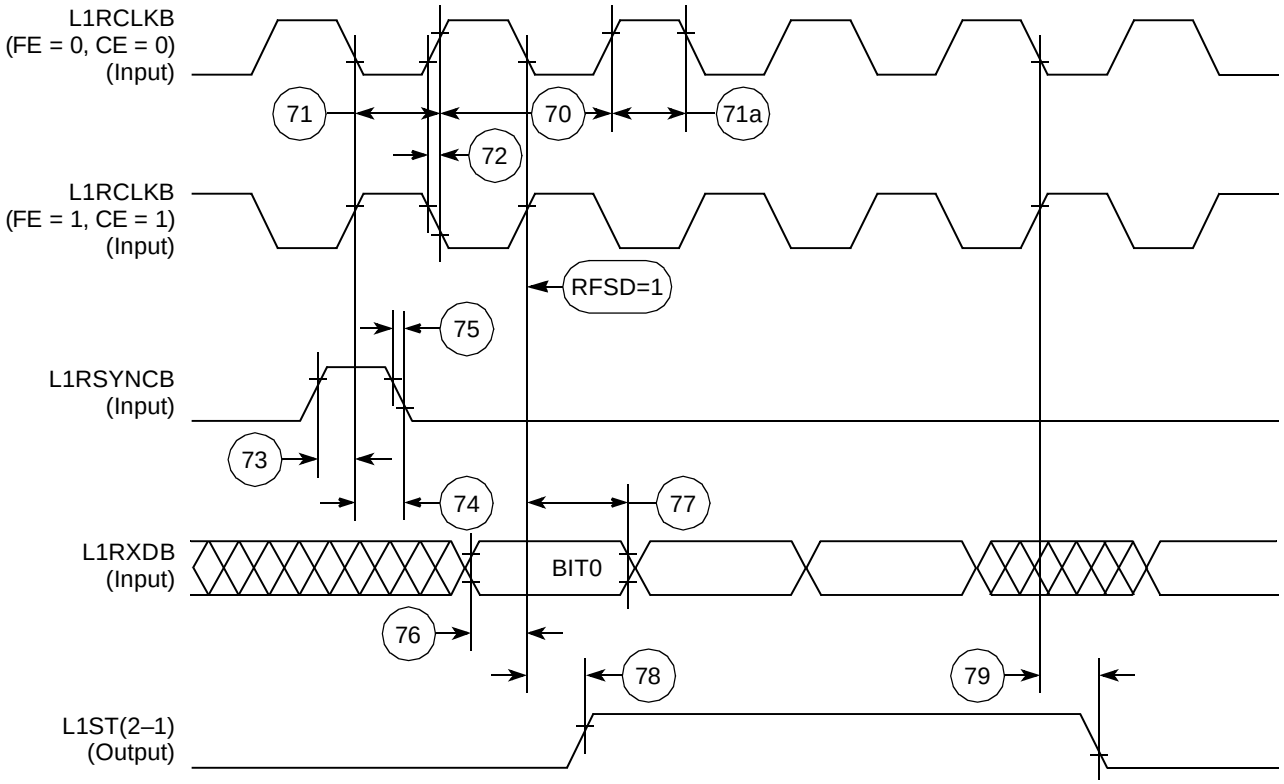


Figure 48. SI Receive Timing Diagram with Normal Clocking (DSC = 0)

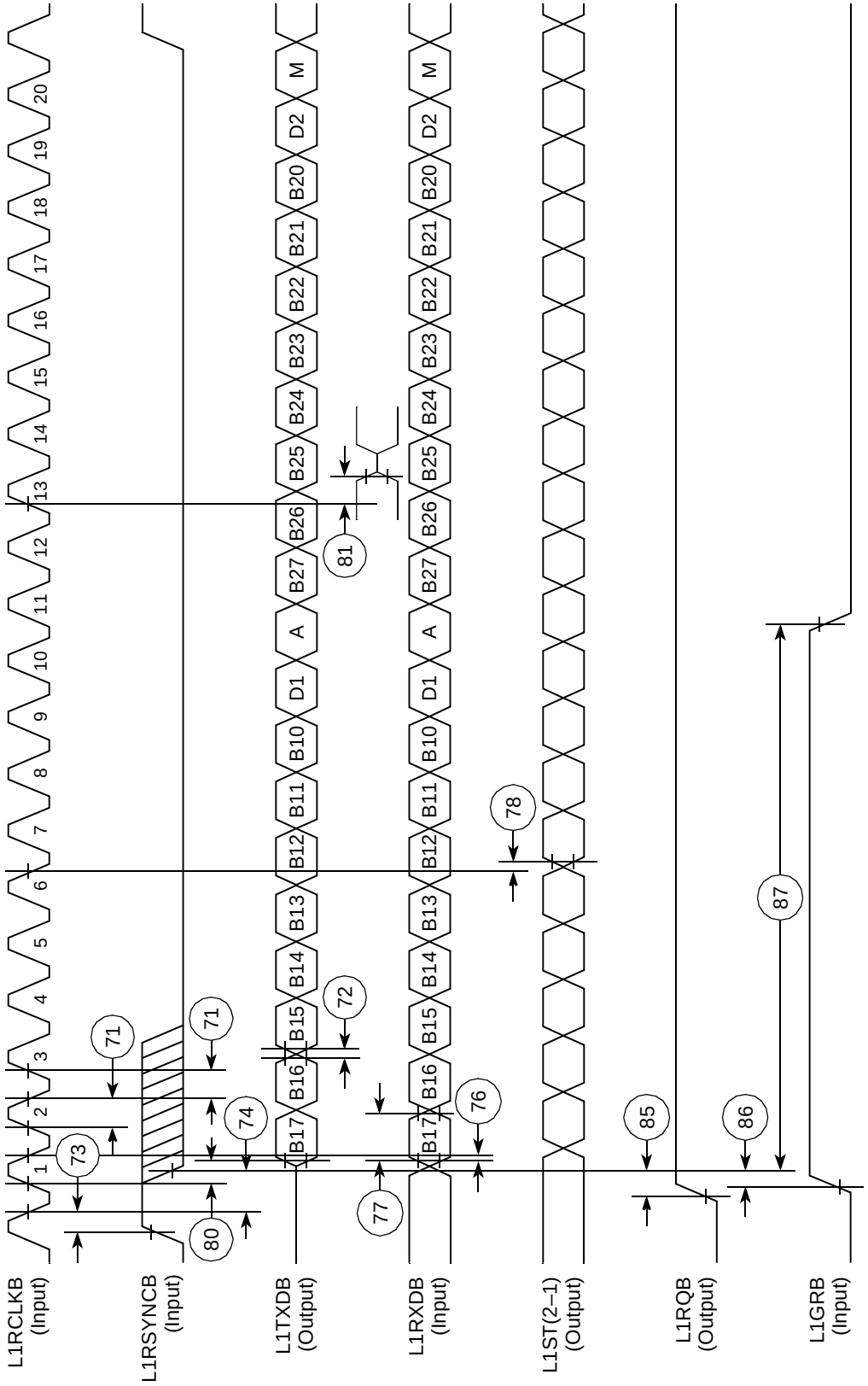


Figure 52. IDL Timing

Figure 53 through Figure 55 show the NMSI timings.

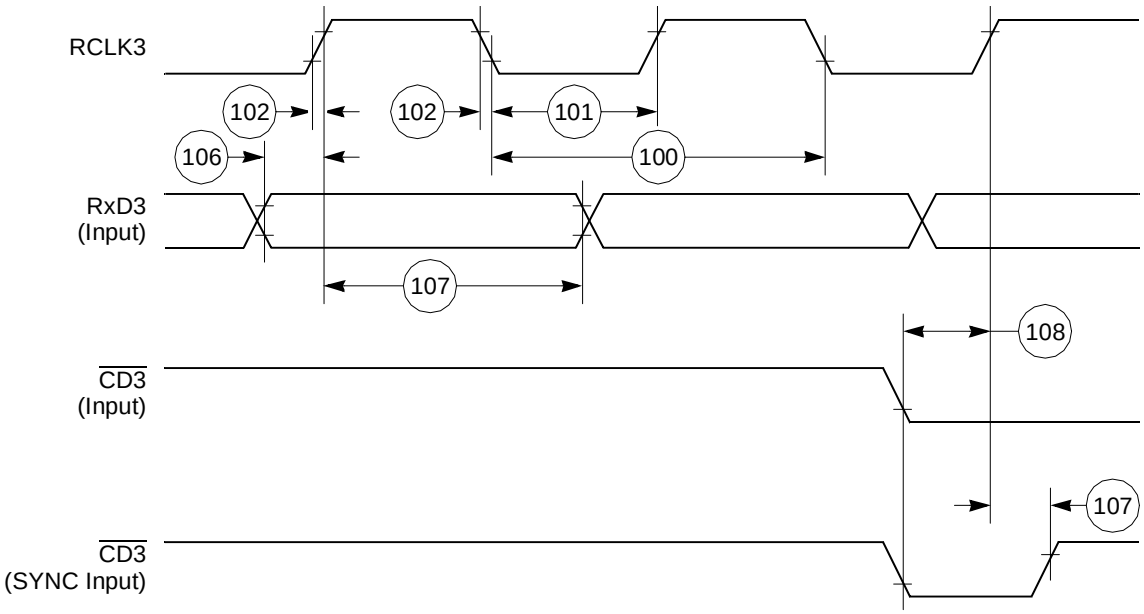


Figure 53. SCC NMSI Receive Timing Diagram

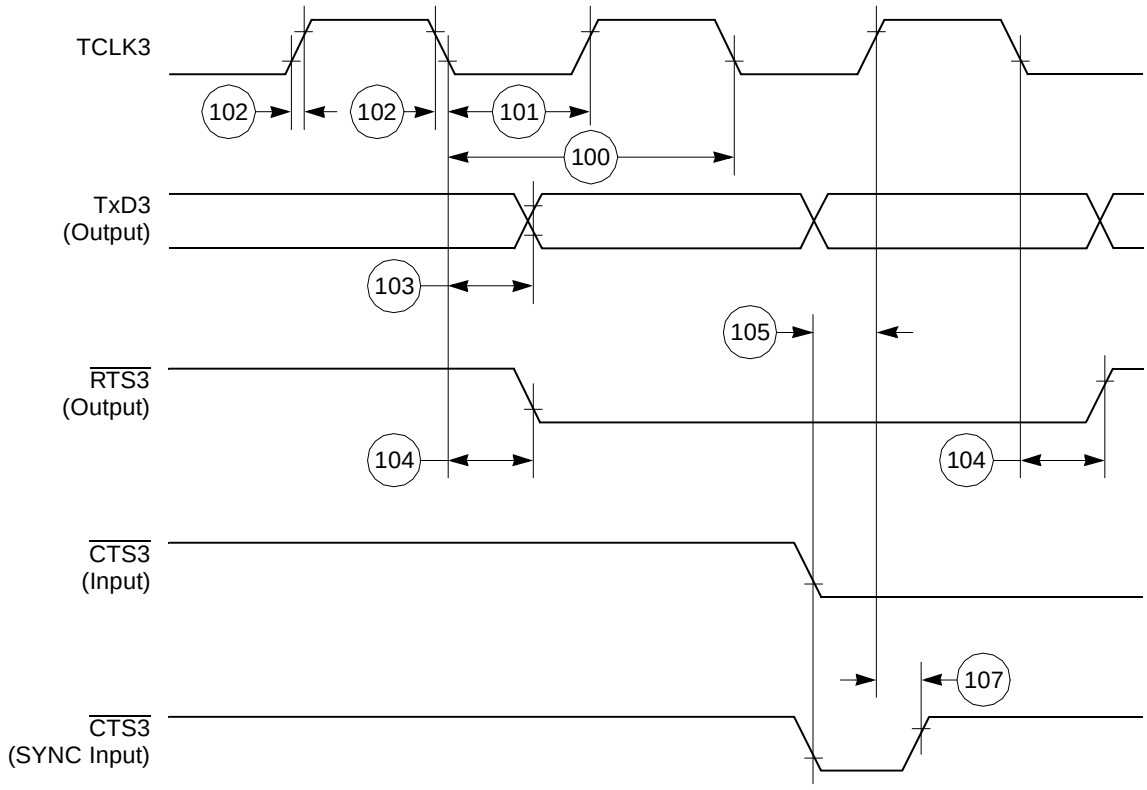
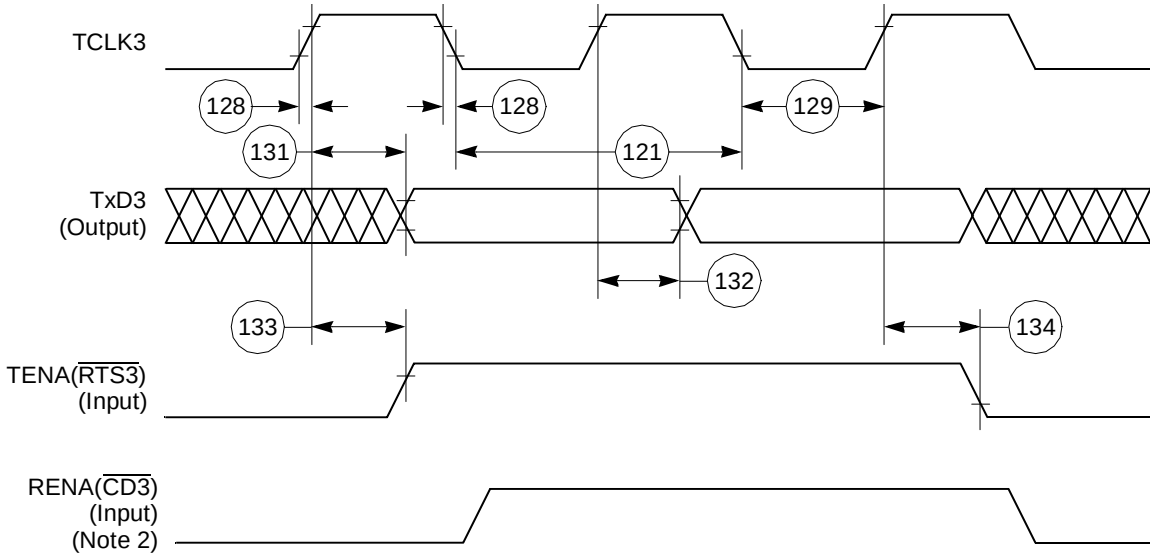


Figure 54. SCC NMSI Transmit Timing Diagram



Notes:
1. Transmit clock invert (TCI) bit in GSMR is set.
2. If RENA is negated before TENA or RENA is not asserted at all during transmit, then the CSL bit is set in the buffer descriptor at the end of the frame transmission.

Figure 58. Ethernet Transmit Timing Diagram

13.8 SMC Transparent AC Electrical Specifications

Table 25 provides the SMC transparent timings as shown in Figure 59.

Table 25. SMC Transparent Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
150	SMCLK clock period[1]	100	—	ns
151	SMCLK width low	50	—	ns
151A	SMCLK width high	50	—	ns
152	SMCLK rise/fall time	—	15	ns
153	SMTXD active delay (from SMCLK falling edge)	10	50	ns
154	SMRXD/SMSYNC setup time	20	—	ns
155	RXD1/SMSYNC hold time	5	—	ns

1 SYNCCLK must be at least twice as fast as SMCLK.

Table 28. I²C Timing (SCL < 100 kHz) (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
210	SDL/SCL fall time	—	300	ns
211	Stop condition setup time	4.7	—	µs

1 SCL frequency is given by SCL = BRGCLK_frequency/((BRG register + 3) × pre_scalar × 2).
The ratio SYNCCLK/(BRGCLK/pre_scalar) must be greater than or equal to 4/1.

Table 29 provides the I²C (SCL > 100 kHz) timings.

Table 29. I²C Timing (SCL > 100 kHz)

Num	Characteristic	Expression	All Frequencies		Unit
			Min	Max	
200	SCL clock frequency (slave)	fSCL	0	BRGCLK/48	Hz
200	SCL clock frequency (master)[1]	fSCL	BRGCLK/16512	BRGCLK/48	Hz
202	Bus free time between transmissions	—	1/(2.2 × fSCL)	—	s
203	Low period of SCL	—	1/(2.2 × fSCL)	—	s
204	High period of SCL	—	1/(2.2 × fSCL)	—	s
205	Start condition setup time	—	1/(2.2 × fSCL)	—	s
206	Start condition hold time	—	1/(2.2 × fSCL)	—	s
207	Data hold time	—	0	—	s
208	Data setup time	—	1/(40 × fSCL)	—	s
209	SDL/SCL rise time	—	—	1/(10 × fSCL)	s
210	SDL/SCL fall time	—	—	1/(33 × fSCL)	s
211	Stop condition setup time	—	1/2(2.2 × fSCL)	—	s

1 SCL frequency is given by SCL = BRGCLK_frequency/((BRG register + 3) × pre_scalar × 2).
The ratio SYNCCLK/(BRGCLK/pre_scalar) must be greater than or equal to 4/1.

Figure 64 shows the I²C bus timing.

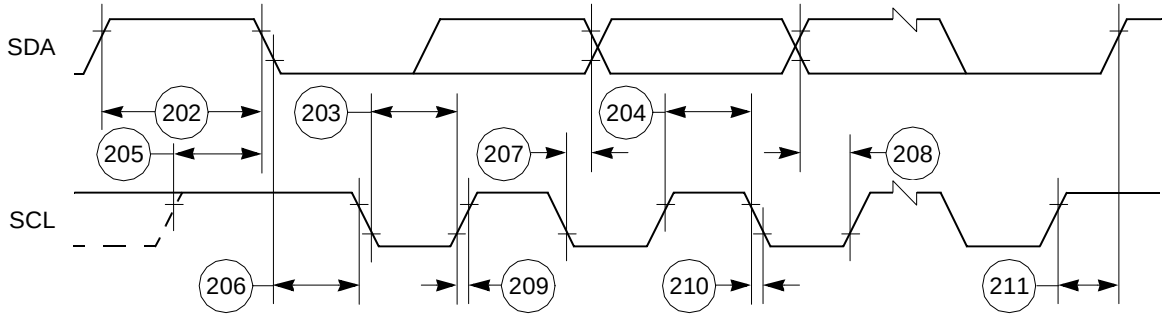


Figure 64. I²C Bus Timing Diagram

Table 36. Pin Assignments—JEDEC Standard (continued)

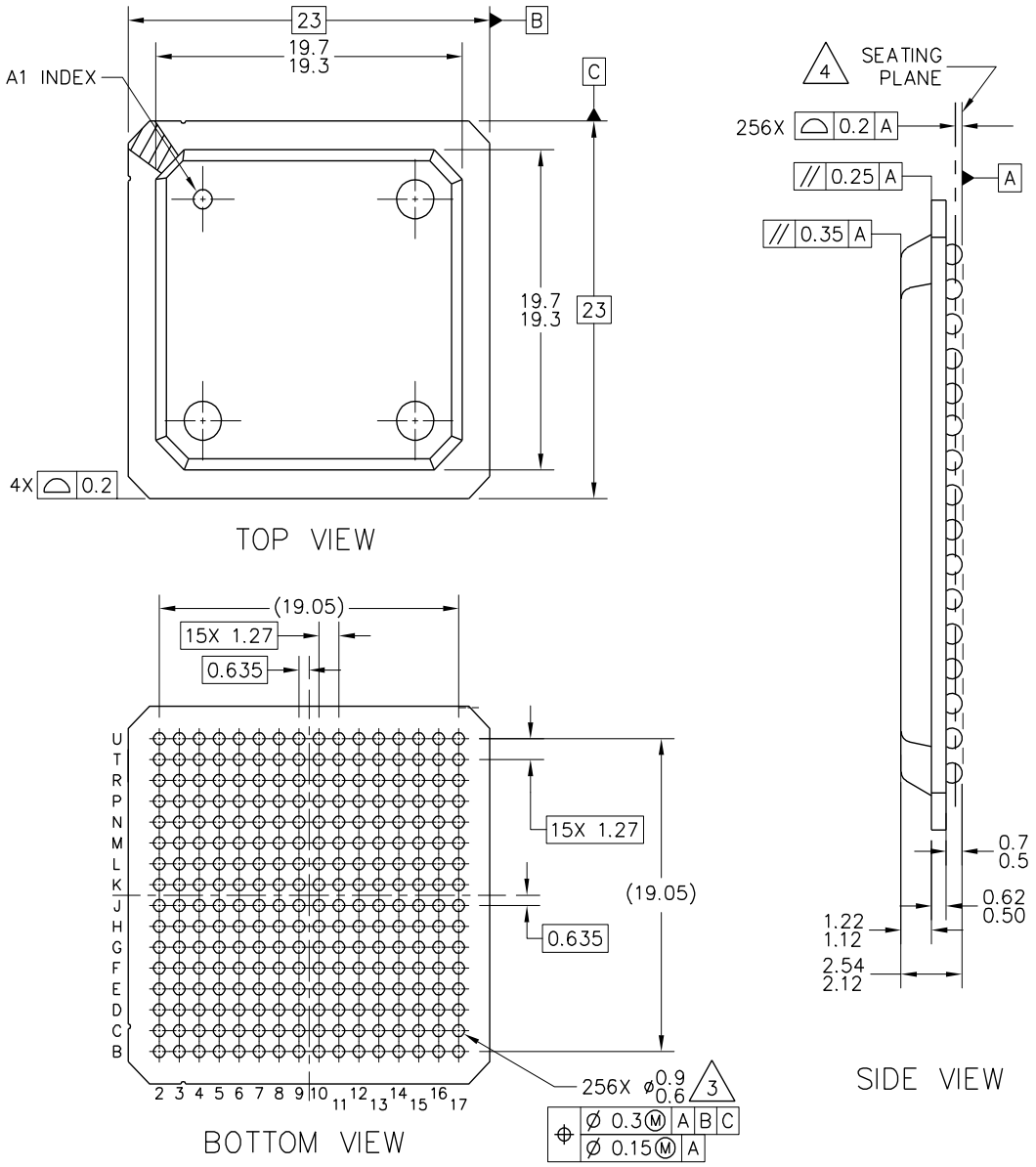
Name	Pin Number	Type
$\overline{\text{CS6}}$, CE1_B	F12	Output
$\overline{\text{CS7}}$, CE2_B	D15	Output
$\overline{\text{WE0}}$, BS_B0, $\overline{\text{IORD}}$	E15	Output
$\overline{\text{WE1}}$, BS_B1, $\overline{\text{IOWR}}$	D17	Output
$\overline{\text{WE2}}$, BS_B2, $\overline{\text{PCOE}}$	D16	Output
$\overline{\text{WE3}}$, BS_B3, $\overline{\text{PCWE}}$	G13	Output
$\overline{\text{BS\_A}}$[0:3]	F14, E16, E17, F15	Output
$\overline{\text{GPL\_A0}}$, $\overline{\text{GPL\_B0}}$	C17	Output
$\overline{\text{OE}}$, $\overline{\text{GPL\_A1}}$, $\overline{\text{GPL\_B1}}$	F13	Output
$\overline{\text{GPL\_A}}$[2:3], $\overline{\text{GPL\_B}}$[2:3], $\overline{\text{CS}}$[2–3]	E14, C16	Output
UPWAITA, $\overline{\text{GPL\_A4}}$	D11	Bidirectional (3.3 V only)
UPWAITB, $\overline{\text{GPL\_B4}}$	E12	Bidirectional
$\overline{\text{GPL\_A5}}$	D12	Output
$\overline{\text{PORESET}}$	D5	Input (3.3 V only)
$\overline{\text{RSTCONF}}$	C3	Input (3.3 V only)
$\overline{\text{HRESET}}$	E7	Open-drain
$\overline{\text{SRESET}}$	C4	Open-drain
XTAL	D6	Analog output
EXTAL	D7	Analog input (3.3 V only)
CLKOUT	G4	Output
EXTCLK	B4	Input (3.3 V only)
TEXP	B3	Output
ALE_A	B7	Output
$\overline{\text{CE1\_A}}$	C15	Output
$\overline{\text{CE2\_A}}$	D14	Output
$\overline{\text{WAIT\_A}}$	D4	Input (3.3 V only)
IP_A0	G6	Input (3.3 V only)
IP_A1	F5	Input (3.3 V only)
IP_A2, $\overline{\text{IOIS16\_A}}$	D3	Input (3.3 V only)
IP_A3	E4	Input (3.3 V only)
IP_A4	D2	Input (3.3 V only)
IP_A5	E3	Input (3.3 V only)

Table 36. Pin Assignments—JEDEC Standard (continued)

Name	Pin Number	Type
PE29, MII2-CRS	U7	Bidirectional (Optional: open-drain)
PE28, $\overline{\text{TOUT3}}$, MII2-COL	R7	Bidirectional (Optional: open-drain)
PE27, L1RQB, MII2-RXERR, RMII2-RXERR	T6	Bidirectional (Optional: open-drain)
PE26, L1CLKOB, MII2-RXDV, RMII2-CRS_DV	T2	Bidirectional (Optional: open-drain)
PE25, RXD4, MII2-RXD3, L1ST2	R4	Bidirectional (Optional: open-drain)
PE24, SMRXD1, BRGO1, MII2-RXD2	U8	Bidirectional (Optional: open-drain)
PE23, TXD4, MII2-RXCLK, L1ST1	U4	Bidirectional (Optional: open-drain)
PE22, TOUT2, MII2-RXD1, RMII2-RXD1, SDACK1	P4	Bidirectional (Optional: open-drain)
PE21, $\overline{\text{TOUT1}}$, MII2-RXD0, RMII2-RXD0	T9	Bidirectional (Optional: open-drain)
PE20, MII2-TXER	U3	Bidirectional (Optional: open-drain)
PE19, L1TXDB, MII2-TXEN, RMII2-TXEN	R6	Bidirectional (Optional: open-drain)
PE18, SMTXD1, MII2-TXD3	M5	Bidirectional (Optional: open-drain)
PE17, TIN3, CLK5, BRGO3, $\overline{\text{SMSYN1}}$, MII2-TXD2	T8	Bidirectional (Optional: open-drain)
PE16, L1RCLKB, CLK6, MII2-TXCLK, RMII2-REFCLK	U6	Bidirectional (Optional: open-drain)
PE15, $\overline{\text{TGATE1}}$, MII2-TXD1, RMII2-TXD1	T7	Bidirectional
PE14, MII2-TXD0, RMII2-TXD0	P8	Bidirectional
TMS	T14	Input (5-V tolerant)
TDI, DSDI	T13	Input (5-V tolerant)
TCK, DSCK	R13	Input (5-V tolerant)
$\overline{\text{TRST}}$	U14	Input (5-V tolerant)

16.2 Mechanical Dimensions of the PBGA Package

Figure 70 shows the mechanical dimensions of the PBGA package.



NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M—1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

Note: Solder sphere composition is 95.5%Sn 45%Ag 0.5%Cu for MPC875/MPC870VRXXX.
Solder sphere composition is 62%Sn 36%Pb 2%Ag for MPC875/MPC870ZTXXX.

Figure 70. Mechanical Dimensions and Bottom Surface Nomenclature of the PBGA Package