Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	66MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (2)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 100°C (TA)
Security Features	-
Package / Case	256-BBGA
Supplier Device Package	256-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc870cvr66

  - ECB, CBC, and counter modes
  - 128-, 192-, and 256-bit key lengths
- Message digest execution unit (MDEU)
  - SHA with 160- or 256-bit message digest
  - MD5 with 128-bit message digest
  - HMAC with either algorithm
- Master/slave logic, with DMA
  - 32-bit address/32-bit data
  - Operation at MPC8xx bus frequency
- Crypto-channel supporting multi-command descriptors
  - Integrated controller managing crypto-execution units
  - Buffer size of 256 bytes for each execution unit, with flow control for large data sizes

- Interrupts
  - Six external interrupt request (IRQ) lines
  - Twelve port pins with interrupt capability
  - Twenty-three internal interrupt sources
  - Programmable priority between SCCs
  - Programmable highest priority request
- Communications processor module (CPM)
  - RISC controller
  - Communication-specific commands (for example, GRACEFUL STOP TRANSMIT, ENTER HUNT MODE, and RESTART TRANSMIT)
  - Supports continuous mode transmission and reception on all serial channels
  - 8-Kbytes of dual-port RAM
  - Several serial DMA (SDMA) channels to support the CPM
  - Three parallel I/O registers with open-drain capability
- On-chip 16 × 16 multiply accumulate controller (MAC)
  - One operation per clock (two-clock latency, one-clock blockage)
  - MAC operates concurrently with other instructions
  - FIR loop—Four clocks per four multiplies
- Four baud-rate generators
  - Independent (can be connected to SCC or SMC)
  - Allows changes during operation
  - Autobaud support option
- SCC (serial communication controller)
  - Ethernet/IEEE 802.3® standard, supporting full 10-Mbps operation
  - HDLC/SDLC

Table 6. DC Electrical Specifications (continued)

Characteristic	Symbol	Min	Max	Unit
Output high voltage, I_{OH} = –2.0 mA, V_{DDH} = 3.0 V (except XTAL and open-drain pins)	V_{OH}	2.4	—	V
Output low voltage I_{OL} = 2.0 mA (CLKOUT) I_{OL} = 3.2 mA[5] I_{OL} = 5.3 mA[6] I_{OL} = 7.0 mA (TXD1/PA14, TXD2/PA12) I_{OL} = 8.9 mA ($\overline{TS}$, $\overline{TA}$, $\overline{TEA}$, $\overline{BI}$, $\overline{BB}$, $\overline{HRESET}$, $\overline{SRESET}$)	V_{OL}	—	0.5	V

1 The difference between V_{DDL} and V_{DDSYN} cannot be more than 100 mV.

2 The signals PA[0:15], PB[14:31], PC[4:15], PD[3:15], PE(14:31), TDI, TDO, TCK, $\overline{TRST}$, TMS, MII1_TXEN, and MII_MDIO are 5-V tolerant. The minimum voltage is still 2.0 V.

3 V_{IL}(max) for the I^2C interface is 0.8 V rather than the 1.5 V as specified in the I^2C standard.

4 Input capacitance is periodically sampled.

5 A(0:31), TSIZ0/$\overline{REG}$, TSIZ1, D(0:31), $\overline{IRQ}$(2:4), $\overline{IRQ6}$, RD/$\overline{WR}$, $\overline{BURST}$, IP_B(0:1), PA(0:4), PA(6:7), PA(10:11), PA15, PB19, PB(23:31), PC(6:7), PC(10:13), PC15, PD8, PE(14:31), MII1_CRS, MII_MDIO, MII1_TXEN, and MII1_COL.

6 $\overline{BDIP}$/$\overline{GPL\_B}$(5), $\overline{BR}$, $\overline{BG}$, FRZ/$\overline{IRQ6}$, $\overline{CS}$(0:7), $\overline{WE}$(0:3), $\overline{BS}$_A(0:3), $\overline{GPL\_A0}$/$\overline{GPL\_B0}$, $\overline{OE}$/$\overline{GPL\_A1}$/$\overline{GPL\_B1}$, $\overline{GPL\_A}$(2:3)/$\overline{GPL\_B}$(2:3)/$\overline{CS}$(2:3), UPWAITA/$\overline{GPL\_A4}$, UPWAITB/$\overline{GPL\_B4}$, $\overline{GPL\_A5}$, ALE_A, $\overline{CE1}$_A, $\overline{CE2}$_A, OP(0:3), and BADDR(28:30).

7 Thermal Calculation and Measurement

For the following discussions, $P_D = (V_{DDL} \times I_{DDL}) + P_{I/O}$, where $P_{I/O}$ is the power dissipation of the I/O drivers.

NOTE

The V_{DDSYN} power dissipation is negligible.

7.1 Estimation with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J, in °C can be obtained from the following equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_A = ambient temperature (°C)

$R_{\theta JA}$ = package junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in package

The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. However, the answer is only an estimate; test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

7.2 Estimation with Junction-to-Case Thermal Resistance

Historically, thermal resistance has frequently been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)

$R_{\theta CA}$ = case-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user adjusts the thermal environment to affect the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the airflow around the device, add a heat sink, change the mounting arrangement on the printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device. This thermal model is most useful for ceramic packages with heat sinks where some 90% of the heat flows through the case and the heat sink to the ambient environment. For most packages, a better model is required.

7.3 Estimation with Junction-to-Board Thermal Resistance

A simple package thermal model that has demonstrated reasonable accuracy (about 20%) is a two-resistor model consisting of a junction-to-board and a junction-to-case thermal resistance. The junction-to-case thermal resistance covers the situation where a heat sink is used or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed-circuit board. It has been observed that the thermal performance of most plastic packages and especially PBGA packages is strongly dependent on the board temperature. If the board temperature is known, an estimate of the junction temperature in the environment can be made using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

$R_{\theta JB}$ = junction-to-board thermal resistance (°C/W)

T_B = board temperature (°C)

P_D = power dissipation in package

If the board temperature is known and the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. For this method to work, the board and board mounting must be similar to the test board used to determine the junction-to-board thermal resistance, namely a 2s2p (board with a power and a ground plane) and vias attaching the thermal balls to the ground plane.

7.4 Estimation Using Simulation

When the board temperature is not known, a thermal simulation of the application is needed. The simple two-resistor model can be used with the thermal simulation of the application [2], or a more accurate and complex model of the package can be used in the thermal simulation.

7.5 Experimental Determination

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

Ψ_{JT} = thermal characterization parameter

T_T = thermocouple temperature on top of package

P_D = power dissipation in package

The thermal characterization parameter is measured per the JESD51-2 specification published by JEDEC using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by the cooling effects of the thermocouple wire.

7.6 References

Semiconductor Equipment and Materials International 805 East Middlefield Rd Mountain View, CA 94043	(415) 964-5111
MIL-SPEC and EIA/JESD (JEDEC) specifications (Available from Global Engineering Documents)	800-854-7179 or 303-397-7956
JEDEC Specifications	http://www.jedec.org

1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
2. 2. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

8 Power Supply and Power Sequencing

This section provides design considerations for the MPC875/MPC870 power supply. The MPC875/MPC870 has a core voltage (V_{DDL}) and PLL voltage (V_{DDSYN}), which both operate at a lower voltage than the I/O voltage (V_{DDH}). The I/O section of the MPC875/MPC870 is supplied with 3.3 V across V_{DDH} and V_{SS} (GND).

The signals PA[0:3], PA[8:11], PB15, PB[24:25], PB[28:31], PC[4:7], PC[12:13], PC15, PD[3:15], TDI, TDO, TCK, $\overline{\text{TRST}}$, TMS, MII_TXEN, and MII_MDIO are 5 V tolerant. No input can be more than 2.5 V greater than V_{DDH}. In addition, 5-V tolerant pins cannot exceed 5.5 V, and remaining input pins cannot exceed 3.465 V. This restriction applies to power up, power down, and normal operation.

Table 7. Mandatory Reset Configuration of MPC875/MPC870 (continued)

Register/Configuration	Field	Value (Binary)
PADIR (Port A data direction register)	PADIR[5:9] PADIR[12:13]	0
PBPAR (Port B pin assignment register)	PBPAR[14:18] PBPAR[20:22]	0
PBDIR (Port B data direction register)	PBDIR[14:8] PBDIR[20:22]	0
PCPAR (Port C pin assignment register)	PCPAR[4:5] PCPAR[8:9] PCPAR[14]	0
PCDIR (Port C data direction register)	PCDIR[4:5] PCDIR[8:9] PCDIR[14]	0
PDPAR (Port D pin assignment register)	PDPAR[3:7] PDPAR[9:5]	0
PDDIR (Port D data direction register)	PDDIR[3:7] PDDIR[9:15]	0

10 Layout Practices

Each V_{DD} pin on the MPC875/MPC870 should be provided with a low-impedance path to the board's supply. Each GND pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The V_{DD} power supply should be bypassed to ground using at least four 0.1-µF bypass capacitors located as close as possible to the four sides of the package. Each board designed should be characterized and additional appropriate decoupling capacitors should be used if required. The capacitor leads and associated printed-circuit traces connecting to chip V_{DD} and GND should be kept to less than half an inch per capacitor lead. At a minimum, a four-layer board employing two inner layers as V_{DD} and GND planes should be used.

All output pins on the MPC875/MPC870 have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses. Maximum PC trace lengths of 6 inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the V_{DD} and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins. For more information, refer to Section 14.4.3, "Clock Synthesizer Power (V_{DDSYN}, V_{SSSYN}, V_{SSSYN1})," in the *MPC885 PowerQUICC™ Family Reference Manual*.

11 Bus Signal Timing

The maximum bus speed supported by the MPC875/MPC870 is 80 MHz. Higher-speed parts must be operated in half-speed bus mode (for example, an MPC875/MPC870 used at 133 MHz must be configured for a 66 MHz bus). Table 8 shows the frequency ranges for standard part frequencies in 1:1 bus mode, and Table 9 shows the frequency ranges for standard part frequencies in 2:1 bus mode.

Table 8. Frequency Ranges for Standard Part Frequencies (1:1 Bus Mode)

Part Frequency	66 MHz		80 MHz	
	Min	Max	Min	Max
Core frequency	40	66.67	40	80
Bus frequency	40	66.67	40	80

Table 9. Frequency Ranges for Standard Part Frequencies (2:1 Bus Mode)

Part Frequency	66 MHz		80 MHz		133 MHz	
	Min	Max	Min	Max	Min	Max
Core frequency	40	66.67	40	80	40	133
Bus frequency	20	33.33	20	40	20	66

Table 10 provides the bus operation timing for the MPC875/MPC870 at 33, 40, 66, and 80 MHz.

The timing for the MPC875/MPC870 bus shown Table 10, assumes a 50-pF load for maximum delays and a 0-pF load for minimum delays. CLKOUT assumes a 100-pF load maximum delay

Table 10. Bus Operation Timings

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B1	Bus period (CLKOUT), see Table 8	—	—	—	—	—	—	—	—	ns
B1a	EXTCLK to CLKOUT phase skew—If CLKOUT is an integer multiple of EXTCLK, then the rising edge of EXTCLK is aligned with the rising edge of CLKOUT. For a non-integer multiple of EXTCLK, this synchronization is lost, and the rising edges of EXTCLK and CLKOUT have a continuously varying phase skew.	–2	+2	–2	+2	–2	+2	–2	+2	ns
B1b	CLKOUT frequency jitter peak-to-peak	—	1	—	1	—	1	—	1	ns
B1c	Frequency jitter on EXTCLK	—	0.50	—	0.50	—	0.50	—	0.50	%
B1d	CLKOUT phase jitter peak-to-peak for OSCLK ≥ 15 MHz	—	4	—	4	—	4	—	4	ns
	CLKOUT phase jitter peak-to-peak for OSCLK < 15 MHz	—	5	—	5	—	5	—	5	ns

Table 10. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B15	CLKOUT to $\overline{\text{TEA}}$ High-Z (MIN = 0.00 × B1 + 2.50)	2.50	15.00	2.50	15.00	2.50	15.00	2.50	15.00	ns
B16	$\overline{\text{TA}}$, $\overline{\text{BI}}$ valid to CLKOUT (setup time) (MIN = 0.00 × B1 + 6.00)	6.00	—	6.00	—	6.00	—	6	—	ns
B16a	$\overline{\text{TEA}}$, $\overline{\text{KR}}$, $\overline{\text{RETRY}}$, $\overline{\text{CR}}$ valid to CLKOUT (setup time) (MIN = 0.00 × B1 + 4.5)	4.50	—	4.50	—	4.50	—	4.50	—	ns
B16b	$\overline{\text{BB}}$, $\overline{\text{BG}}$, $\overline{\text{BR}}$, valid to CLKOUT (setup time)[2] (4MIN = 0.00 × B1 + 0.00)	4.00	—	4.00	—	4.00	—	4.00	—	ns
B17	CLKOUT to $\overline{\text{TA}}$, $\overline{\text{TEA}}$, $\overline{\text{BI}}$, $\overline{\text{BB}}$, $\overline{\text{BG}}$, $\overline{\text{BR}}$ valid (hold time) (MIN = 0.00 × B1 + 1.00[3])	1.00	—	1.00	—	2.00	—	2.00	—	ns
B17a	CLKOUT to $\overline{\text{KR}}$, $\overline{\text{RETRY}}$, $\overline{\text{CR}}$ valid (hold time) (MIN = 0.00 × B1 + 2.00)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B18	D(0:31) valid to CLKOUT rising edge (setup time)[4] (MIN = 0.00 × B1 + 6.00)	6.00	—	6.00	—	6.00	—	6.00	—	ns
B19	CLKOUT rising edge to D(0:31) valid (hold time)[4] (MIN = 0.00 × B1 + 1.00[5])	1.00	—	1.00	—	2.00	—	2.00	—	ns
B20	D(0:31) valid to CLKOUT falling edge (setup time)[6] (MIN = 0.00 × B1 + 4.00)	4.00	—	4.00	—	4.00	—	4.00	—	ns
B21	CLKOUT falling edge to D(0:31) valid (hold time)[6] (MIN = 0.00 × B1 + 2.00)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B22	CLKOUT rising edge to $\overline{\text{CS}}$ asserted GPCM ACS = 00 (MAX = 0.25 × B1 + 6.3)	7.60	13.80	6.30	12.50	3.80	10.00	3.13	9.43	ns
B22a	CLKOUT falling edge to $\overline{\text{CS}}$ asserted GPCM ACS = 10, TRLX = 0 (MAX = 0.00 × B1 + 8.00)	—	8.00	—	8.00	—	8.00	—	8.00	ns
B22b	CLKOUT falling edge to $\overline{\text{CS}}$ asserted GPCM ACS = 11, TRLX = 0, EBDF = 0 (MAX = 0.25 × B1 + 6.3)	7.60	13.80	6.30	12.50	3.80	10.00	3.13	9.43	ns
B22c	CLKOUT falling edge to $\overline{\text{CS}}$ asserted GPCM ACS = 11, TRLX = 0, EBDF = 1 (MAX = 0.375 × B1 + 6.6)	10.90	18.00	10.90	16.00	5.20	12.30	4.69	10.93	ns
B23	CLKOUT rising edge to $\overline{\text{CS}}$ negated GPCM read access, GPCM write access ACS = 00, TRLX = 0 and CSNT = 0 (MAX = 0.00 × B1 + 8.00)	2.00	8.00	2.00	8.00	2.00	8.00	2.00	8.00	ns
B24	A(0:31) and BADDR(28:30) to $\overline{\text{CS}}$ asserted GPCM ACS = 10, TRLX = 0 (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	1.80	—	1.13	—	ns
B24a	A(0:31) and BADDR(28:30) to $\overline{\text{CS}}$ asserted GPCM ACS = 11, TRLX = 0 (MIN = 0.50 × B1 – 2.00)	13.20	—	10.50	—	5.60	—	4.25	—	ns

Table 10. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B25	CLKOUT rising edge to $\overline{OE}$, $\overline{WE}$(0:3)/BS_B[0:3] asserted (MAX = 0.00 × B1 + 9.00)	—	9.00		9.00		9.00	—	9.00	ns
B26	CLKOUT rising edge to $\overline{OE}$ negated (MAX = 0.00 × B1 + 9.00)	2.00	9.00	2.00	9.00	2.00	9.00	2.00	9.00	ns
B27	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 1 (MIN = 1.25 × B1 – 2.00)	35.90	—	29.30	—	16.90	—	13.60	—	ns
B27a	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 1 (MIN = 1.50 × B1 – 2.00)	43.50	—	35.50	—	20.70	—	16.75	—	ns
B28	CLKOUT rising edge to $\overline{WE}$(0:3)/BS_B[0:3] negated GPCM write access CSNT = 0 (MAX = 0.00 × B1 + 9.00)	—	9.00	—	9.00	—	9.00	—	9.00	ns
B28a	CLKOUT falling edge to $\overline{WE}$(0:3)/BS_B[0:3] negated GPCM write access TRLX = 0, CSNT = 1, EBDF = 0 (MAX = 0.25 × B1 + 6.80)	7.60	14.30	6.30	13.00	3.80	10.50	3.13	9.93	ns
B28b	CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0, CSNT = 1 ACS = 10 or ACS = 11, EBDF = 0 (MAX = 0.25 × B1 + 6.80)	—	14.30	—	13.00	—	10.50	—	9.93	ns
B28c	CLKOUT falling edge to $\overline{WE}$(0:3)/BS_B[0:3] negated GPCM write access TRLX = 0, CSNT = 1 write access TRLX = 0, CSNT = 1, EBDF = 1 (MAX = 0.375 × B1 + 6.6)	10.90	18.00	10.90	18.00	5.20	12.30	4.69	11.29	ns
B28d	CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1 (MAX = 0.375 × B1 + 6.6)	—	18.00	—	18.00	—	12.30	—	11.30	ns
B29	$\overline{WE}$(0:3)/BS_B[0:3] negated to D(0:31) High-Z GPCM write access, CSNT = 0, EBDF = 0 (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	1.80	—	1.13	—	ns
B29a	$\overline{WE}$(0:3)/BS_B[0:3] negated to D(0:31) High-Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 0 (MIN = 0.50 × B1 – 2.00)	13.20	—	10.50	—	5.60	—	4.25	—	ns
B29b	$\overline{CS}$ negated to D(0:31) High-Z GPCM write access, ACS = 00, TRLX = 0 and CSNT = 0 (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	1.80	—	1.13	—	ns
B29c	$\overline{CS}$ negated to D(0:31) High-Z GPCM write access, TRLX = 0, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 0 (MIN = 0.50 × B1 – 2.00)	13.20	—	10.50	—	5.60	—	4.25	—	ns

Table 10. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B30d	$\overline{WE}$(0:3)/BS_B[0:3] negated to A(0:31), BADDR(28:30) invalid GPCM write access TRLX = 1, CSNT =1, $\overline{CS}$ negated to A(0:31) invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10 or 11, EBDF = 1	38.67	—	31.38	—	17.83	—	14.19	—	ns
B31	CLKOUT falling edge to $\overline{CS}$ valid as requested by control bit CST4 in the corresponding word in the UPM (MAX = 0.00 × B1 + 6.00)	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B31a	CLKOUT falling edge to $\overline{CS}$ valid as requested by control bit CST1 in the corresponding word in the UPM (MAX = 0.25 × B1 + 6.80)	7.60	14.30	6.30	13.00	3.80	10.50	3.13	10.00	ns
B31b	CLKOUT rising edge to $\overline{CS}$ valid, as requested by control bit CST2 in the corresponding word in the UPM (MAX = 0.00 × B1 + 8.00)	1.50	8.00	1.50	8.00	1.50	8.00	1.50	8.00	ns
B31c	CLKOUT rising edge to $\overline{CS}$ valid, as requested by control bit CST3 in the corresponding word in the UPM (MAX = 0.25 × B1 + 6.30)	7.60	13.80	6.30	12.50	3.80	10.00	3.13	9.40	ns
B31d	CLKOUT falling edge to $\overline{CS}$ valid as requested by control bit CST1 in the corresponding word in the UPM EBDF = 1 (MAX = 0.375 × B1 + 6.6)	13.30	18.00	11.30	16.00	7.60	12.30	4.69	11.30	ns
B32	CLKOUT falling edge to $\overline{BS}$ valid as requested by control bit BST4 in the corresponding word in the UPM (MAX = 0.00 × B1 + 6.00)	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B32a	CLKOUT falling edge to $\overline{BS}$ valid as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 0 (MAX = 0.25 × B1 + 6.80)	7.60	14.30	6.30	13.00	3.80	10.50	3.13	10.00	ns
B32b	CLKOUT rising edge to $\overline{BS}$ valid, as requested by control bit BST2 in the corresponding word in the UPM (MAX = 0.00 × B1 + 8.00)	1.50	8.00	1.50	8.00	1.50	8.00	1.50	8.00	ns
B32c	CLKOUT rising edge to $\overline{BS}$ valid, as requested by control bit BST3 in the corresponding word in the UPM (MAX = 0.25 × B1 + 6.80)	7.60	14.30	6.30	13.00	3.80	10.50	3.13	10.00	ns
B32d	CLKOUT falling edge to $\overline{BS}$ valid as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 1 (MAX = 0.375 × B1 + 6.60)	13.30	18.00	11.30	16.00	7.60	12.30	4.49	11.30	ns
B33	CLKOUT falling edge to $\overline{GPL}$ valid as requested by control bit GxT4 in the corresponding word in the UPM (MAX = 0.00 × B1 + 6.00)	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns

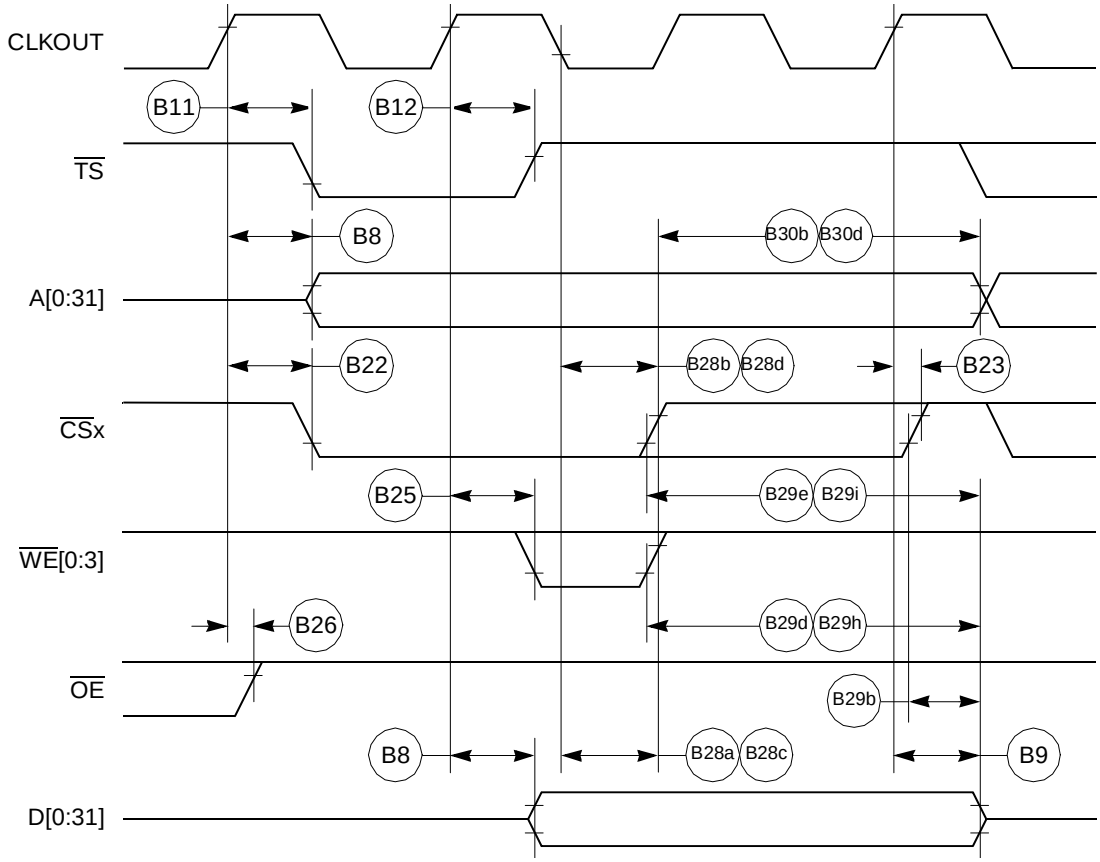

Figure 18. External Bus Write Timing (GPCM Controlled—TRLX = 1, CSNT = 1)

Figure 27 provides the PCMCIA access cycle timing for the external bus read.

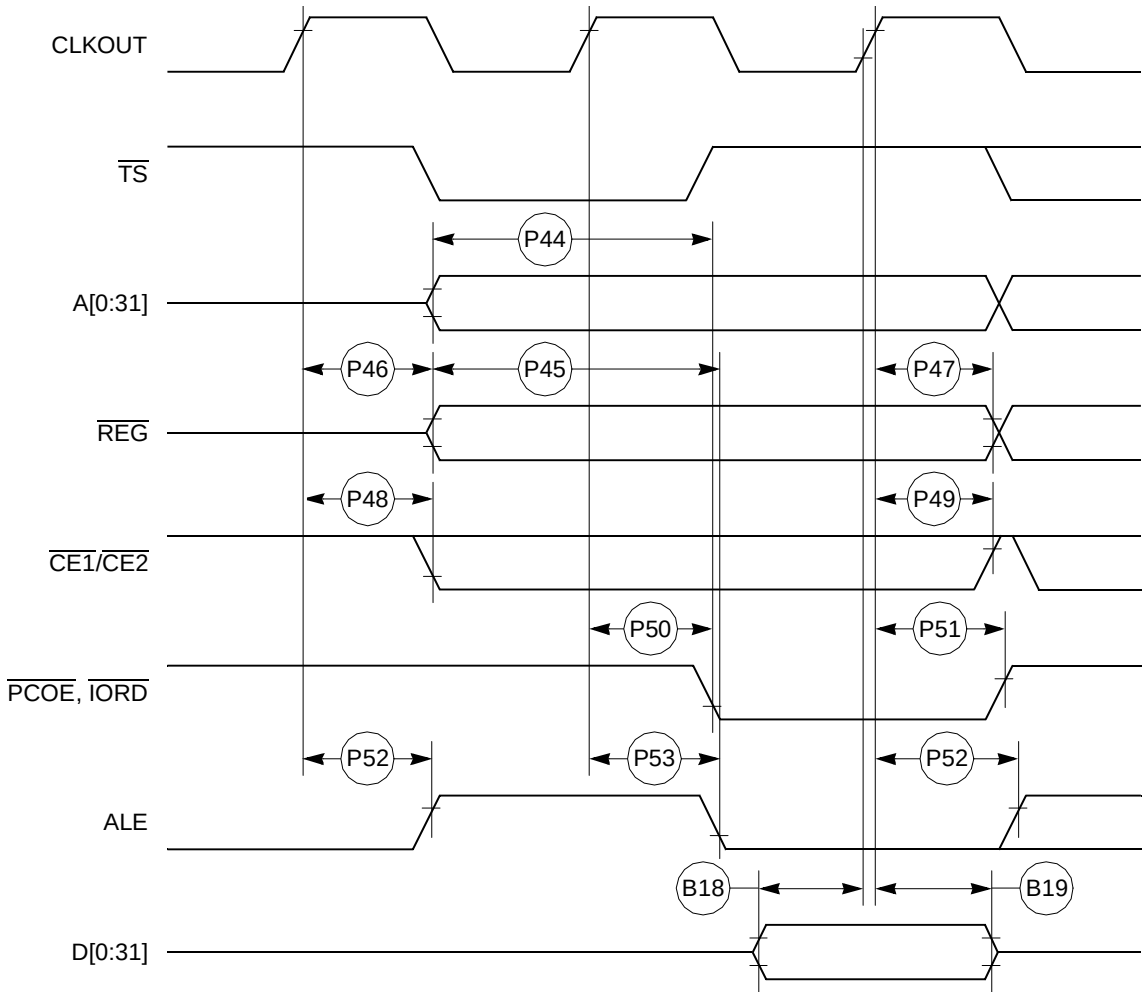

Figure 27. PCMCIA Access Cycles Timing External Bus Read

Table 14 shows the debug port timing for the MPC875/MPC870.

Table 14. Debug Port Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
D61	DSCK cycle time	$3 \times T_{CLOCKOUT}$		—
D62	DSCK clock pulse width	$1.25 \times T_{CLOCKOUT}$		—
D63	DSCK rise and fall times	0.00	3.00	ns
D64	DSDI input data setup time	8.00		ns
D65	DSDI data hold time	5.00		ns
D66	DSCK low to DSDO data valid	0.00	15.00	ns
D67	DSCK low to DSDO invalid	0.00	2.00	ns

Figure 32 provides the input timing for the debug port clock.

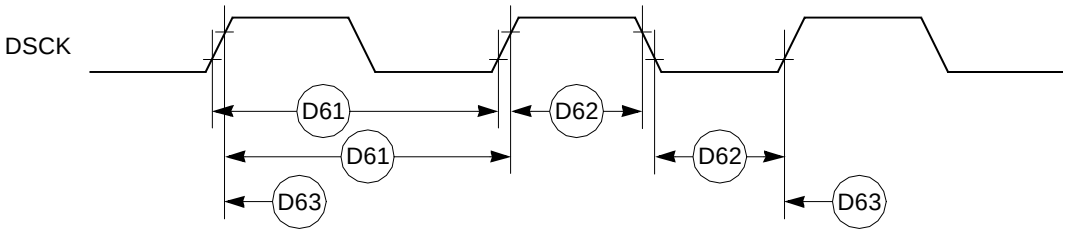

Figure 32. Debug Port Clock Input Timing

Figure 33 provides the timing for the debug port.

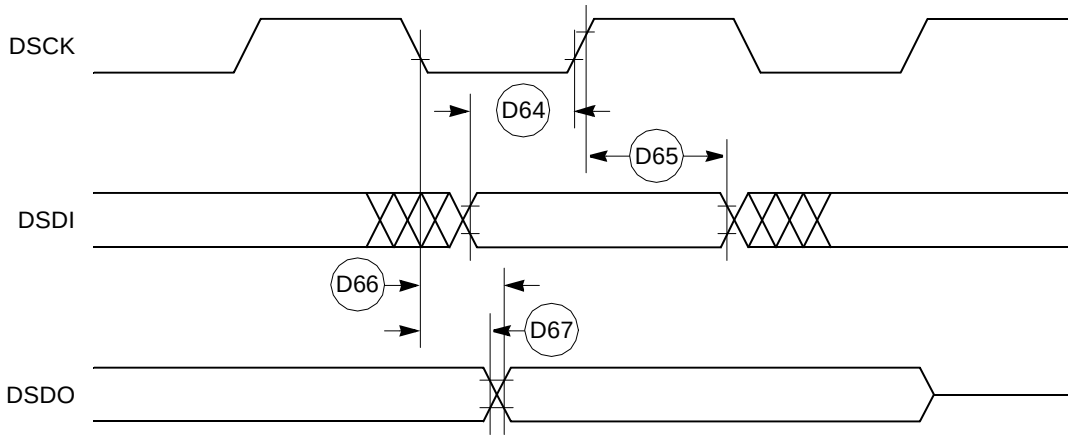

Figure 33. Debug Port Timings

Table 15 shows the reset timing for the MPC875/MPC870.

Table 15. Reset Timing

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
R69	CLKOUT to $\overline{\text{HRESET}}$ high impedance (MAX = 0.00 × B1 + 20.00)	—	20.00	—	20.00	—	20.00	—	20.00	ns
R70	CLKOUT to $\overline{\text{SRESET}}$ high impedance (MAX = 0.00 × B1 + 20.00)	—	20.00	—	20.00	—	20.00	—	20.00	ns
R71	$\overline{\text{RSTCONF}}$ pulse width (MIN = 17.00 × B1)	515.20	—	425.00	—	257.60	—	212.50	—	ns
R72	—	—	—	—	—	—	—	—	—	—
R73	Configuration data to $\overline{\text{HRESET}}$ rising edge setup time (MIN = 15.00 × B1 + 50.00)	504.50	—	425.00	—	277.30	—	237.50	—	ns
R74	Configuration data to $\overline{\text{RSTCONF}}$ rising edge setup time (MIN = 0.00 × B1 + 350.00)	350.00	—	350.00	—	350.00	—	350.00	—	ns
R75	Configuration data hold time after $\overline{\text{RSTCONF}}$ negation (MIN = 0.00 × B1 + 0.00)	0.00	—	0.00	—	0.00	—	0.00	—	ns
R76	Configuration data hold time after $\overline{\text{HRESET}}$ negation (MIN = 0.00 × B1 + 0.00)	0.00	—	0.00	—	0.00	—	0.00	—	ns
R77	$\overline{\text{HRESET}}$ and $\overline{\text{RSTCONF}}$ asserted to data out drive (MAX = 0.00 × B1 + 25.00)	—	25.00	—	25.00	—	25.00	—	25.00	ns
R78	$\overline{\text{RSTCONF}}$ negated to data out high impedance (MAX = 0.00 × B1 + 25.00)	—	25.00	—	25.00	—	25.00	—	25.00	ns
R79	CLKOUT of last rising edge before chip three-states $\overline{\text{HRESET}}$ to data out high impedance (MAX = 0.00 × B1 + 25.00)	—	25.00	—	25.00	—	25.00	—	25.00	ns
R80	DSDI, DSCK setup (MIN = 3.00 × B1)	90.90	—	75.00	—	45.50	—	37.50	—	ns
R81	DSDI, DSCK hold time (MIN = 0.00 × B1 + 0.00)	0.00	—	0.00	—	0.00	—	0.00	—	ns
R82	$\overline{\text{SRESET}}$ negated to CLKOUT rising edge for DSDI and DSCK sample (MIN = 8.00 × B1)	242.40	—	200.00	—	121.20	—	100.00	—	ns

Table 21. SI Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
83a	L1RCLKB, L1TCLKB width high (DSC = 1)[3]	P + 10	—	ns
84	L1CLKB edge to L1CLKOB valid (DSC = 1)	—	30.00	ns
85	$\overline{\text{L1RQB}}$ valid before falling edge of L1TSYNCB[4]	1.00	—	L1TCLK
86	L1GRB setup time[2]	42.00	—	ns
87	L1GRB hold time	42.00	—	ns
88	L1CLKB edge to L1SYNCB valid (FSD = 00) CNT = 0000, BYT = 0, DSC = 0)	—	0.00	ns

1 The ratio SYNCCLK/L1RCLKB must be greater than 2.5/1.
2 These specs are valid for IDL mode only.
3 Where P = 1/CLKOUT. Thus, for a 25-MHz CLKO1 rate, P = 40 ns.
4 These strobes and TxD on the first bit of the frame become valid after the L1CLKB edge or L1SYNCB, whichever comes later.

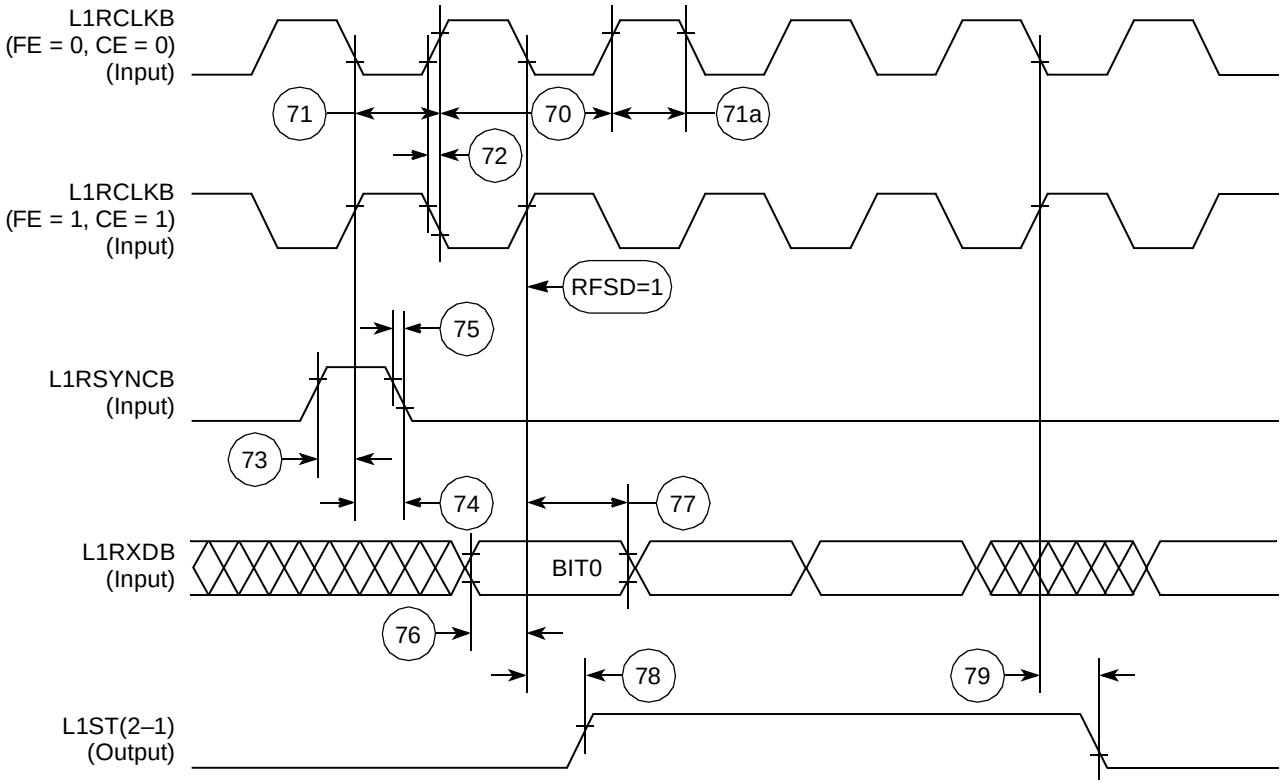

Figure 48. SI Receive Timing Diagram with Normal Clocking (DSC = 0)

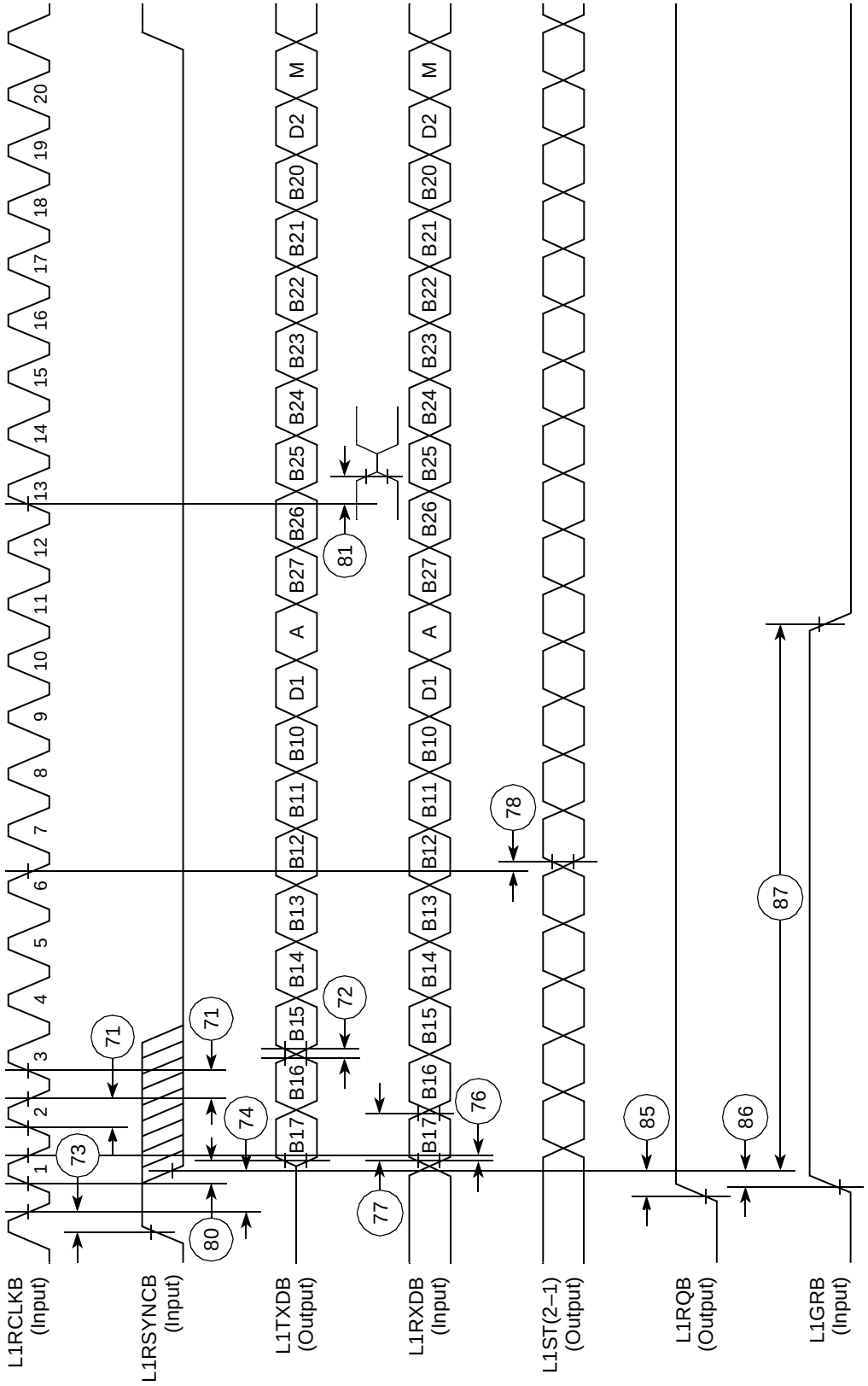

Figure 52. IDL Timing

14 USB Electrical Characteristics

This section provides the AC timings for the USB interface.

14.1 USB Interface AC Timing Specifications

The USB Port uses the transmit clock on SCC1. Table 30 lists the USB interface timings.

Table 30. USB Interface AC Timing Specifications

Name	Characteristic	All Frequencies		Unit
		Min	Max	
US1	USBCLK frequency of operation[1] Low speed Full speed	 6 48		MHz
US4	USBCLK duty cycle (measured at 1.5 V)	45	55	%

1 USBCLK accuracy should be ±500 ppm or better. USBCLK may be stopped to conserve power.

15 FEC Electrical Characteristics

This section provides the AC electrical specifications for the Fast Ethernet controller (FEC). Note that the timing specifications for the MII signals are independent of system clock frequency (part speed designation). Also, MII signals use TTL signal levels compatible with devices operating at either 5.0 or 3.3 V.

15.1 MII and Reduced MII Receive Signal Timing

The receiver functions correctly up to a MII_RX_CLK maximum frequency of 25 MHz + 1%. The reduced MII (RMII) receiver functions correctly up to a RMII_REFCLK maximum frequency of 50 MHz + 1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_RX_CLK frequency – 1%.

Table 31 provides information on the MII receive signal timing.

Table 31. MII Receive Signal Timing

Num	Characteristic	Min	Max	Unit
M1	MII_RXD[3:0], MII_RX_DV, MII_RX_ER to MII_RX_CLK setup	5	—	ns
M2	MII_RX_CLK to MII_RXD[3:0], MII_RX_DV, MII_RX_ER hold	5	—	ns
M3	MII_RX_CLK pulse width high	35%	65%	MII_RX_CLK period
M4	MII_RX_CLK pulse width low	35%	65%	MII_RX_CLK period
M1_RMII	RMII_RXD[1:0], RMII_CRS_DV, RMII_RX_ERR to RMII_REFCLK setup	4	—	ns
M2_RMII	RMII_REFCLK to RMII_RXD[1:0], RMII_CRS_DV, RMII_RX_ERR hold	2	—	ns

Figure 65 shows MII receive signal timing.

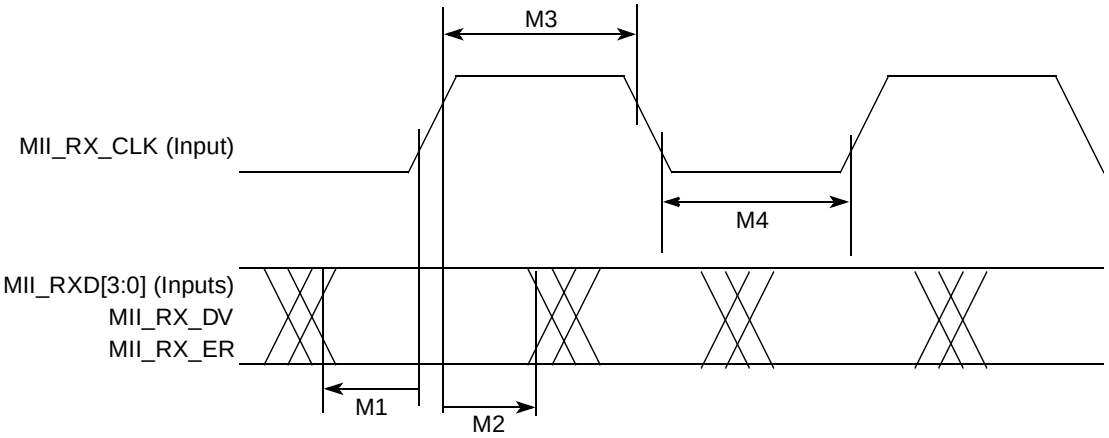

Figure 65. MII Receive Signal Timing Diagram

15.2 MII and Reduced MII Transmit Signal Timing

The transmitter functions correctly up to a MII_TX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_TX_CLK frequency – 1%.

Table 32 provides information on the MII transmit signal timing.

Table 32. MII Transmit Signal Timing

Num	Characteristic	Min	Max	Unit
M5	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER invalid	5	—	ns
M6	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER valid	—	25	ns
M7	MII_TX_CLK pulse width high	35%	65%	MII_TX_CLK period
M8	MII_TX_CLK pulse width low	35%	65%	MII_TX_CLK period
M20_RMII	RMII_TXD[1:0], RMII_TX_EN to RMII_REFCLK setup	4	—	ns
M21_RMII	RMII_TXD[1:0], RMII_TX_EN data hold from RMII_REFCLK rising edge	2	—	ns

16.1 Pin Assignments

Figure 69 shows the JEDEC pinout of the PBGA package as viewed from the top surface. For additional information, see the *MPC885 PowerQUICC Family User's Manual*.

NOTE

The pin numbering starts with B2 in order to conform to the JEDEC standard for 23-mm body size using a 16 × 16 array.

NOTE: This is the top view of the device.

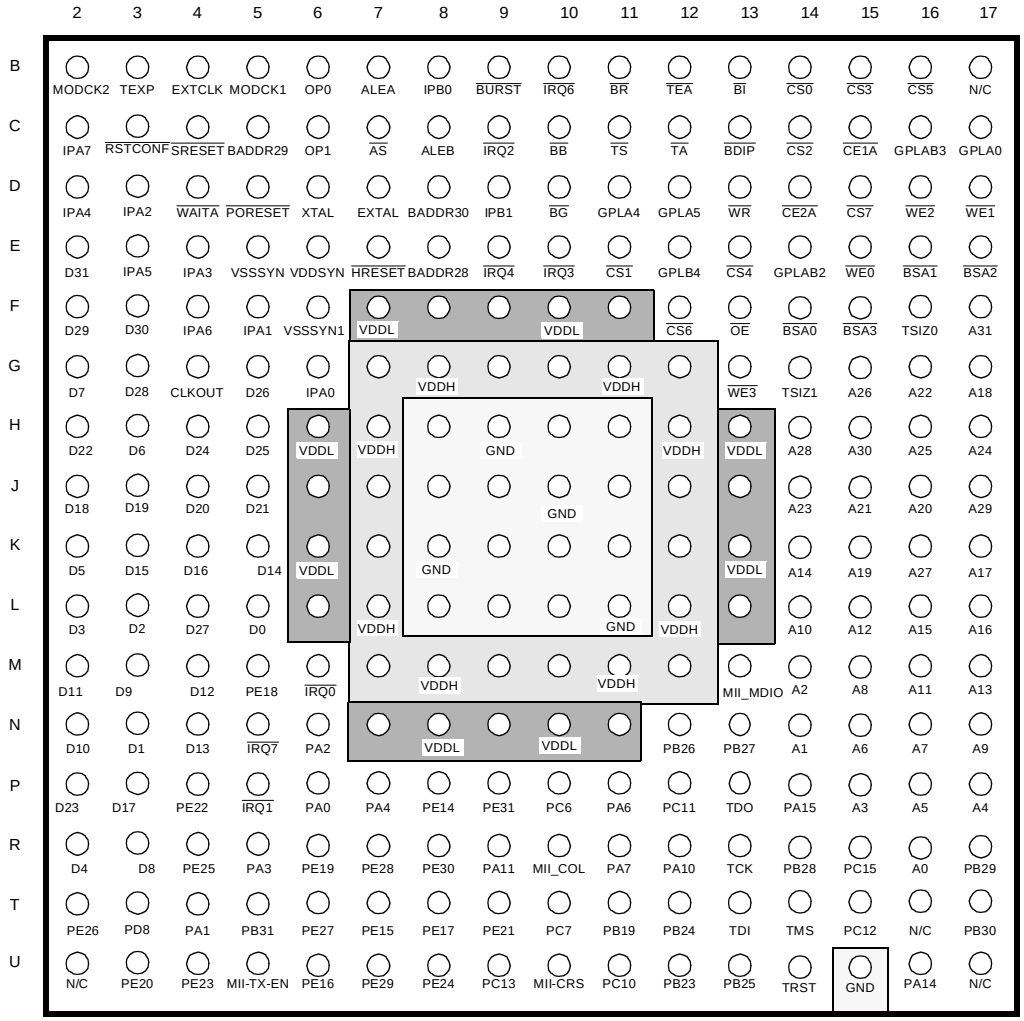

Figure 69. Pinout of the PBGA Package—JEDEC Standard

Table 36. Pin Assignments—JEDEC Standard (continued)

Name	Pin Number	Type
PB30, SPICLK	T17	Bidirectional (Optional: open-drain) (5-V tolerant)
PB29, SPIMOSI	R17	Bidirectional (Optional: open-drain) (5-V tolerant)
PB28, SPIMISO, BRGO4	R14	Bidirectional (Optional: open-drain) (5-V tolerant)
PB27, I2CSDA, BRGO1	N13	Bidirectional (Optional: open-drain)
PB26, I2CSCL, BRGO2	N12	Bidirectional (Optional: open-drain)
PB25, SMTXD1	U13	Bidirectional (Optional: open-drain) (5-V tolerant)
PB24, SMRXD1	T12	Bidirectional (Optional: open-drain) (5-V tolerant)
PB23, $\overline{\text{SDACK1}}$, $\overline{\text{SMSYN1}}$	U12	Bidirectional (Optional: open-drain)
PB19, MII1-RXD3, RTS4	T11	Bidirectional (Optional: open-drain)
PC15, $\overline{\text{DREQ0}}$, L1ST1	R15	Bidirectional (5-V tolerant)
PC13, MII1-TXD3, SDACK1	U9	Bidirectional (5-V tolerant)
PC12, MII1-TXD2, TOUT1	T15	Bidirectional (5-V tolerant)
PC11, USBRXP	P12	Bidirectional
PC10, USBRXN, $\overline{\text{TGATE1}}$	U11	Bidirectional
PC7, $\overline{\text{CTS4}}$, L1TSYNCB, USBTXP	T10	Bidirectional (5-V tolerant)
PC6, $\overline{\text{CD4}}$, L1RSYNCB, USBTXN	P10	Bidirectional (5-V tolerant)
PD8, RXD4, MII-MDC, RMII-MDC	T3	Bidirectional (5-V tolerant)
PE31, CLK8, L1TCLKB, MII1-RXCLK	P9	Bidirectional (Optional: open-drain)
PE30, L1RXDB, MII1-RXD2	R8	Bidirectional (Optional: open-drain)

How to Reach Us:

Home Page:
www.freescale.com

Web Support:
http://www.freescale.com/support

USA/Europe or Locations Not Listed:
Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
+1-800-521-6274 or
+1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku
Tokyo 153-0064
Japan
0120 191014 or
+81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor
Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
+1-800 441-2447 or
+1-303-675-2140
Fax: +1-303-675-2150
LDCForFreescaleSemiconductor
@hibbertgroup.com

Document Number: MPC875EC
Rev. 4
08/2007