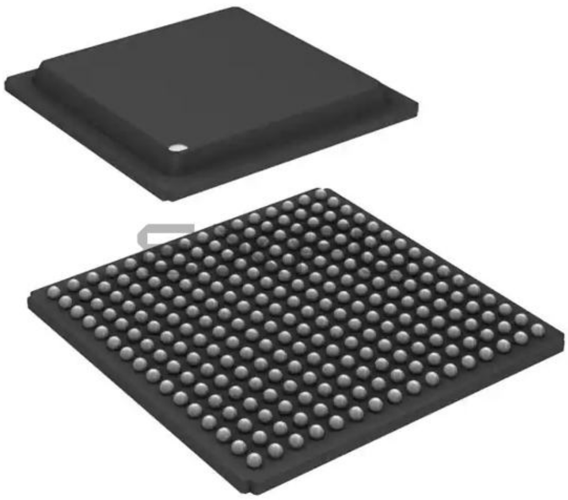

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	66MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (2)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TA)
Security Features	-
Package / Case	256-BBGA
Supplier Device Package	256-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc870vr66

  - ECB, CBC, and counter modes
  - 128-, 192-, and 256-bit key lengths
- — Message digest execution unit (MDEU)
  - SHA with 160- or 256-bit message digest
  - MD5 with 128-bit message digest
  - HMAC with either algorithm
- — Master/slave logic, with DMA
  - 32-bit address/32-bit data
  - Operation at MPC8xx bus frequency
- — Crypto-channel supporting multi-command descriptors
  - Integrated controller managing crypto-execution units
  - Buffer size of 256 bytes for each execution unit, with flow control for large data sizes

- Interrupts
  - Six external interrupt request (IRQ) lines
  - Twelve port pins with interrupt capability
  - Twenty-three internal interrupt sources
  - Programmable priority between SCCs
  - Programmable highest priority request
- Communications processor module (CPM)
  - RISC controller
  - Communication-specific commands (for example, GRACEFUL STOP TRANSMIT, ENTER HUNT MODE, and RESTART TRANSMIT)
  - Supports continuous mode transmission and reception on all serial channels
  - 8-Kbytes of dual-port RAM
  - Several serial DMA (SDMA) channels to support the CPM
  - Three parallel I/O registers with open-drain capability
- On-chip 16 × 16 multiply accumulate controller (MAC)
  - One operation per clock (two-clock latency, one-clock blockage)
  - MAC operates concurrently with other instructions
  - FIR loop—Four clocks per four multiplies
- Four baud-rate generators
  - Independent (can be connected to SCC or SMC)
  - Allows changes during operation
  - Autobaud support option
- SCC (serial communication controller)
  - Ethernet/IEEE 802.3® standard, supporting full 10-Mbps operation
  - HDLC/SDLC

7.2 Estimation with Junction-to-Case Thermal Resistance

Historically, thermal resistance has frequently been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)

$R_{\theta CA}$ = case-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user adjusts the thermal environment to affect the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the airflow around the device, add a heat sink, change the mounting arrangement on the printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device. This thermal model is most useful for ceramic packages with heat sinks where some 90% of the heat flows through the case and the heat sink to the ambient environment. For most packages, a better model is required.

7.3 Estimation with Junction-to-Board Thermal Resistance

A simple package thermal model that has demonstrated reasonable accuracy (about 20%) is a two-resistor model consisting of a junction-to-board and a junction-to-case thermal resistance. The junction-to-case thermal resistance covers the situation where a heat sink is used or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed-circuit board. It has been observed that the thermal performance of most plastic packages and especially PBGA packages is strongly dependent on the board temperature. If the board temperature is known, an estimate of the junction temperature in the environment can be made using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

$R_{\theta JB}$ = junction-to-board thermal resistance (°C/W)

T_B = board temperature (°C)

P_D = power dissipation in package

If the board temperature is known and the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. For this method to work, the board and board mounting must be similar to the test board used to determine the junction-to-board thermal resistance, namely a 2s2p (board with a power and a ground plane) and vias attaching the thermal balls to the ground plane.

7.4 Estimation Using Simulation

When the board temperature is not known, a thermal simulation of the application is needed. The simple two-resistor model can be used with the thermal simulation of the application [2], or a more accurate and complex model of the package can be used in the thermal simulation.

7.5 Experimental Determination

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

Ψ_{JT} = thermal characterization parameter

T_T = thermocouple temperature on top of package

P_D = power dissipation in package

The thermal characterization parameter is measured per the JESD51-2 specification published by JEDEC using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by the cooling effects of the thermocouple wire.

7.6 References

Semiconductor Equipment and Materials International 805 East Middlefield Rd Mountain View, CA 94043	(415) 964-5111
MIL-SPEC and EIA/JESD (JEDEC) specifications (Available from Global Engineering Documents)	800-854-7179 or 303-397-7956
JEDEC Specifications	http://www.jedec.org

1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
2. 2. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

8 Power Supply and Power Sequencing

This section provides design considerations for the MPC875/MPC870 power supply. The MPC875/MPC870 has a core voltage (V_{DDL}) and PLL voltage (V_{DDSYN}), which both operate at a lower voltage than the I/O voltage (V_{DDH}). The I/O section of the MPC875/MPC870 is supplied with 3.3 V across V_{DDH} and V_{SS} (GND).

The signals PA[0:3], PA[8:11], PB15, PB[24:25], PB[28:31], PC[4:7], PC[12:13], PC15, PD[3:15], TDI, TDO, TCK, $\overline{\text{TRST}}$, TMS, MII_TXEN, and MII_MDIO are 5 V tolerant. No input can be more than 2.5 V greater than V_{DDH}. In addition, 5-V tolerant pins cannot exceed 5.5 V, and remaining input pins cannot exceed 3.465 V. This restriction applies to power up, power down, and normal operation.

One consequence of multiple power supplies is that when power is initially applied, the voltage rails ramp up at different rates. The rates depend on the nature of the power supply, the type of load on each power supply, and the manner in which different voltages are derived. The following restrictions apply:

- V_{DDL} must not exceed V_{DDH} during power up and power down
- V_{DDL} must not exceed 1.9 V, and V_{DDH} must not exceed 3.465 V

These cautions are necessary for the long-term reliability of the part. If they are violated, the electrostatic discharge (ESD) protection diodes are forward-biased, and excessive current can flow through these diodes. If the system power supply design does not control the voltage sequencing, the circuit shown in Figure 4 can be added to meet these requirements. The MUR420 Schottky diodes control the maximum potential difference between the external bus and core power supplies on power up, and the 1N5820 diodes regulate the maximum potential difference on power down.

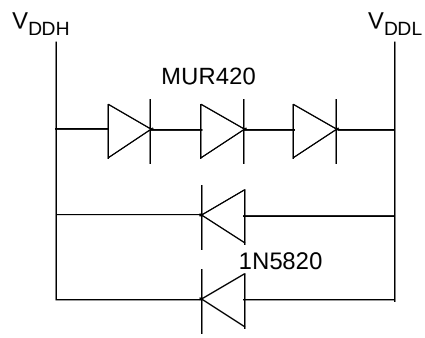


Figure 4. Example Voltage Sequencing Circuit

9 Mandatory Reset Configurations

The MPC875/MPC870 requires a mandatory configuration during reset.

If hardware reset configuration word (HRCW) is enabled, the HRCW[DBGC] value needs to be set to binary X1 in the HRCW and the SIUMCR[DBGC] should be programmed with the same value in the boot code after reset. This can be done by asserting the $\overline{\text{RSTCONF}}$ during $\overline{\text{HRESET}}$ assertion.

If HRCW is disabled, the SIUMCR[DBGC] should be programmed with binary X1 in the boot code after reset by negating the $\overline{\text{RSTCONF}}$ during the $\overline{\text{HRESET}}$ assertion.

The MBMR[GPLB4DIS], PAPAR, PADIR, PBPAR, PBDIR, PCPAR, and PCDIR need to be configured with the mandatory values in Table 7 in the boot code after the reset is negated.

Table 7. Mandatory Reset Configuration of MPC875/MPC870

Register/Configuration	Field	Value (Binary)
HRCW (Hardware reset configuration word)	HRCW[DBGC]	X1
SIUMCR (SIU module configuration register)	SIUMCR[DBGC]	X1
MBMR (Machine B mode register)	MBMR[GPLB4DIS}	0
PAPAR (Port A pin assignment register)	PAPAR[5:9] PAPAR[12:13]	0

Table 7. Mandatory Reset Configuration of MPC875/MPC870 (continued)

Register/Configuration	Field	Value (Binary)
PADIR (Port A data direction register)	PADIR[5:9] PADIR[12:13]	0
PBPAR (Port B pin assignment register)	PBPAR[14:18] PBPAR[20:22]	0
PBDIR (Port B data direction register)	PBDIR[14:8] PBDIR[20:22]	0
PCPAR (Port C pin assignment register)	PCPAR[4:5] PCPAR[8:9] PCPAR[14]	0
PCDIR (Port C data direction register)	PCDIR[4:5] PCDIR[8:9] PCDIR[14]	0
PDPAR (Port D pin assignment register)	PDPAR[3:7] PDPAR[9:5]	0
PDDIR (Port D data direction register)	PDDIR[3:7] PDDIR[9:15]	0

10 Layout Practices

Each V_{DD} pin on the MPC875/MPC870 should be provided with a low-impedance path to the board's supply. Each GND pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The V_{DD} power supply should be bypassed to ground using at least four 0.1-µF bypass capacitors located as close as possible to the four sides of the package. Each board designed should be characterized and additional appropriate decoupling capacitors should be used if required. The capacitor leads and associated printed-circuit traces connecting to chip V_{DD} and GND should be kept to less than half an inch per capacitor lead. At a minimum, a four-layer board employing two inner layers as V_{DD} and GND planes should be used.

All output pins on the MPC875/MPC870 have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses. Maximum PC trace lengths of 6 inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the V_{DD} and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins. For more information, refer to Section 14.4.3, "Clock Synthesizer Power (V_{DDSYN}, V_{SSSYN}, V_{SSSYN1})," in the *MPC885 PowerQUICC™ Family Reference Manual*.

Table 10. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B29d	WE(0:3)/BS_B[0:3] negated to D(0:31) High-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 0 (MIN = 1.50 × B1 – 2.00)	43.50	—	35.50	—	20.70	—	16.75	—	ns
B29e	CS negated to D(0:31) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 0 (MIN = 1.50 × B1 – 2.00)	43.50	—	35.50	—	20.70	—	16.75	—	ns
B29f	WE(0:3/BS_B[0:3]) negated to D(0:31) High-Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 1 (MIN = 0.375 × B1 – 6.30)[7]	5.00	—	3.00	—	0.00	—	0.00	—	ns
B29g	CS negated to D(0:31) High-Z GPCM write access, TRLX = 0, CSNT = 1 ACS = 10 or ACS = 11, EBDF = 1 (MIN = 0.375 × B1 – 6.30)[7]	5.00	—	3.00	—	0.00	—	0.00	—	ns
B29h	WE(0:3)/BS_B[0:3] negated to D(0:31) High-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 1 (MIN = 0.375 × B1 – 3.30)	38.40	—	31.10	—	17.50	—	13.85	—	ns
B29i	CS negated to D(0:31) (0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1 (MIN = 0.375 × B1 – 3.30)	38.40	—	31.10	—	17.50	—	13.85	—	ns
B30	CS, WE(0:3)/BS_B[0:3] negated to A(0:31), BADDR(28:30) invalid GPCM write access[8] (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	1.80	—	1.13	—	ns
B30a	WE(0:3)/BS_B[0:3] negated to A(0:31), BADDR(28:30) invalid GPCM, write access, TRLX = 0, CSNT = 1, CS negated to A(0:31), invalid GPCM write access TRLX = 0, CSNT = 1, ACS = 10 or ACS == 11, EBDF = 0 (MIN = 0.50 × B1 – 2.00)	13.20	—	10.50	—	5.60	—	4.25	—	ns
B30b	WE(0:3)/BS_B[0:3] negated to A(0:31), invalid GPCM BADDR(28:30), invalid GPCM write access, TRLX = 1, CSNT = 1. CS negated to A(0:31), invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10 or ACS == 11, EBDF = 0 (MIN = 1.50 × B1 – 2.00)	43.50	—	35.50	—	20.70	—	16.75	—	ns
B30c	WE(0:3)/BS_B[0:3] negated to A(0:31), BADDR(28:30) invalid GPCM write access, TRLX = 0, CSNT = 1. CS negated to A(0:31) invalid GPCM write access, TRLX = 0, CSNT = 1 ACS = 10 or ACS == 11, EBDF = 1 (MIN = 0.375 × B1 – 3.00)	8.40	—	6.40	—	2.70	—	1.70	—	ns

Table 10. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B42	CLKOUT rising edge to $\overline{TS}$ valid (hold time) (MIN = 0.00 × B1 + 2.00)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B43	$\overline{AS}$ negation to memory controller signals negation (MAX = TBD)	—	TBD	—	TBD	—	TBD	—	TBD	ns

[1] For part speeds above 50 MHz, use 9.80 ns for B11a.

[2] The timing required for $\overline{BR}$ input is relevant when the MPC875/MPC870 is selected to work with the internal bus arbiter. The timing for $\overline{BG}$ input is relevant when the MPC875/MPC870 is selected to work with the external bus arbiter.

[3] For part speeds above 50 MHz, use 2 ns for B17.

[4] The D(0:31) input timings B18 and B19 refer to the rising edge of the CLKOUT in which the $\overline{TA}$ input signal is asserted.

[5] For part speeds above 50 MHz, use 2 ns for B19.

[6] The D(0:31) input timings B20 and B21 refer to the falling edge of the CLKOUT. This timing is valid only for read accesses controlled by chip-selects under control of the user-programmable machine (UPM) in the memory controller, for data beats where DLT3 = 1 in the RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

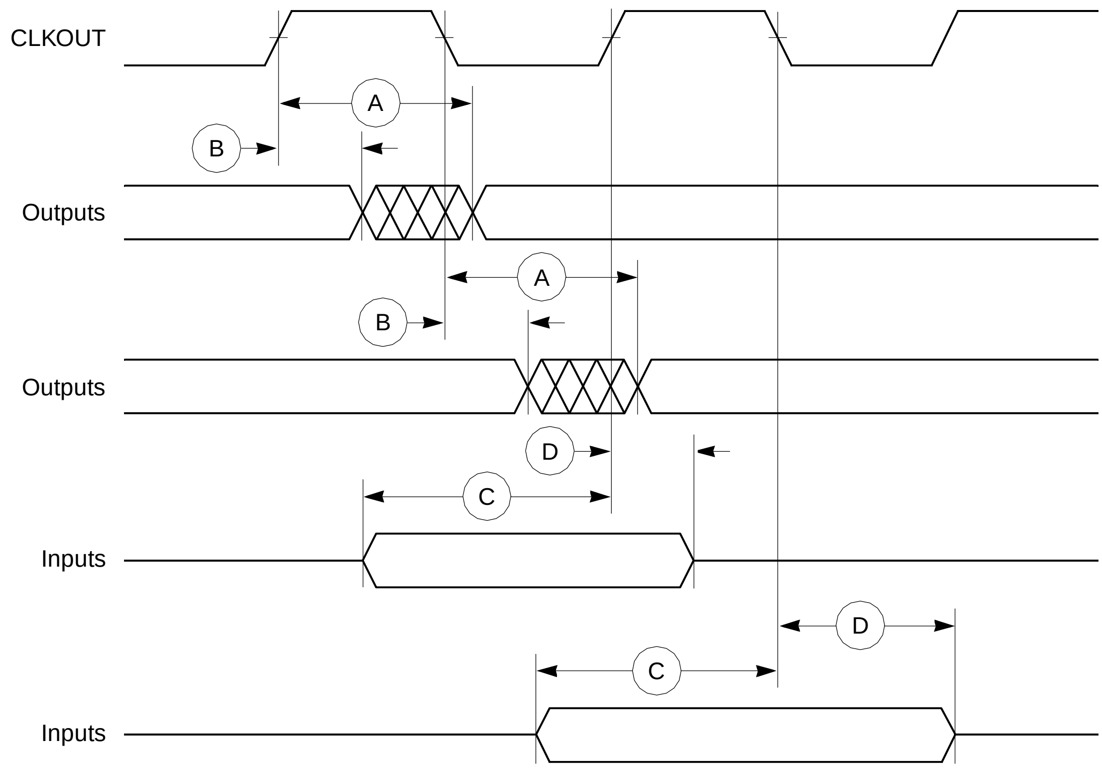
[7] This formula applies to bus operation up to 50 MHz.

[8] The timing B30 refers to $\overline{CS}$ when ACS = 00 and to $\overline{WE}$(0:3) when CSNT = 0.

[9] The signal UPWAIT is considered asynchronous to the CLKOUT and synchronized internally. The timings specified in B37 and B38 are specified to enable the freeze of the UPM output signals as described in Figure 20.

[10] The $\overline{AS}$ signal is considered asynchronous to the CLKOUT. The timing B39 is specified in order to allow the behavior specified in Figure 23.

Figure 5 provides the control timing diagram.



(A) Maximum output delay specification.

(B) Minimum output hold time.

(C) Minimum input setup time specification.

(D) Minimum input hold time specification.

Figure 5. Control Timing

Figure 6 provides the timing for the external clock.

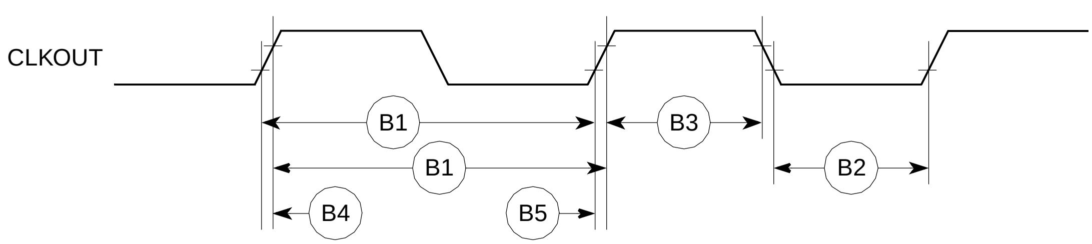


Figure 6. External Clock Timing

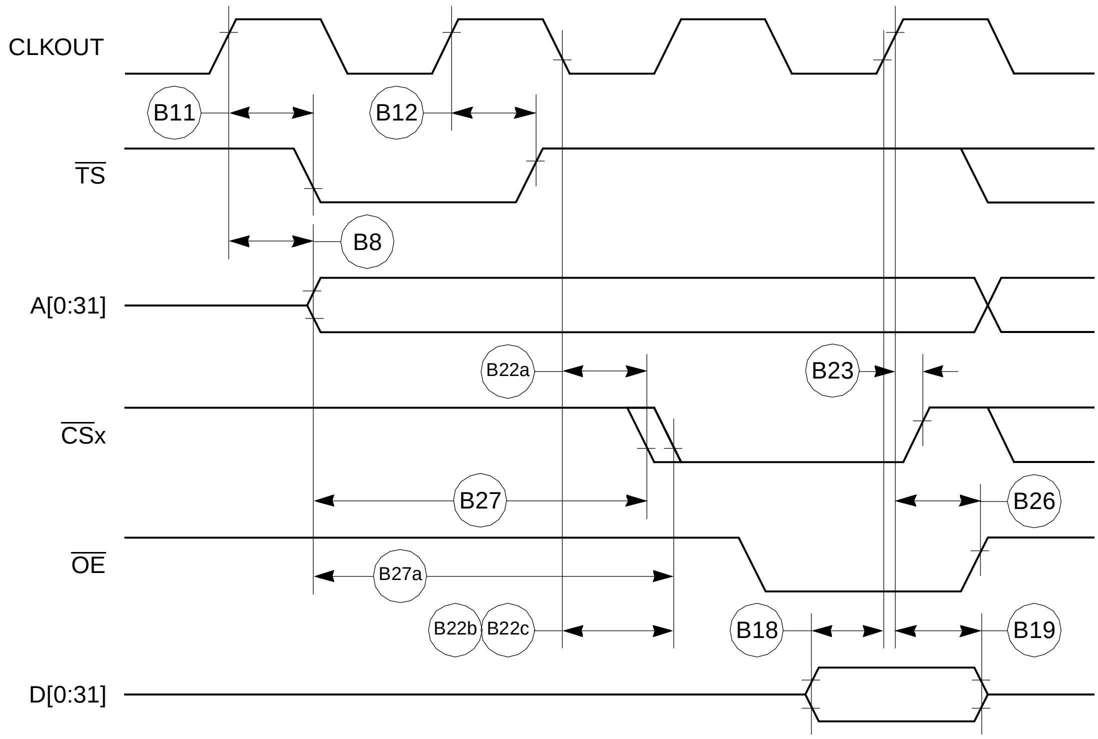


Figure 15. External Bus Read Timing (GPCM Controlled—TRLX = 1, ACS = 10, ACS = 11)

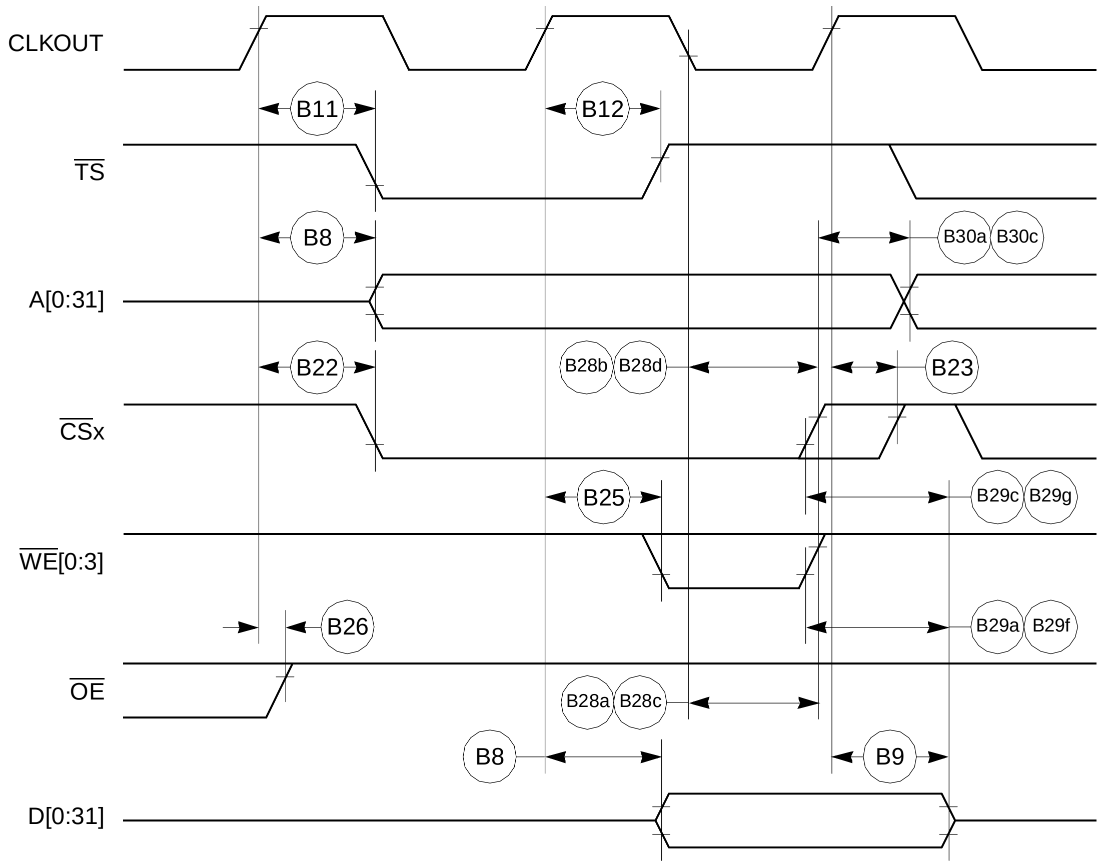


Figure 17. External Bus Write Timing (GPCM Controlled—TRLX = 0, CSNT = 1)

Table 15 shows the reset timing for the MPC875/MPC870.

Table 15. Reset Timing

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
R69	CLKOUT to $\overline{\text{HRESET}}$ high impedance (MAX = 0.00 × B1 + 20.00)	—	20.00	—	20.00	—	20.00	—	20.00	ns
R70	CLKOUT to $\overline{\text{SRESET}}$ high impedance (MAX = 0.00 × B1 + 20.00)	—	20.00	—	20.00	—	20.00	—	20.00	ns
R71	$\overline{\text{RSTCONF}}$ pulse width (MIN = 17.00 × B1)	515.20	—	425.00	—	257.60	—	212.50	—	ns
R72	—	—	—	—	—	—	—	—	—	—
R73	Configuration data to $\overline{\text{HRESET}}$ rising edge setup time (MIN = 15.00 × B1 + 50.00)	504.50	—	425.00	—	277.30	—	237.50	—	ns
R74	Configuration data to $\overline{\text{RSTCONF}}$ rising edge setup time (MIN = 0.00 × B1 + 350.00)	350.00	—	350.00	—	350.00	—	350.00	—	ns
R75	Configuration data hold time after $\overline{\text{RSTCONF}}$ negation (MIN = 0.00 × B1 + 0.00)	0.00	—	0.00	—	0.00	—	0.00	—	ns
R76	Configuration data hold time after $\overline{\text{HRESET}}$ negation (MIN = 0.00 × B1 + 0.00)	0.00	—	0.00	—	0.00	—	0.00	—	ns
R77	$\overline{\text{HRESET}}$ and $\overline{\text{RSTCONF}}$ asserted to data out drive (MAX = 0.00 × B1 + 25.00)	—	25.00	—	25.00	—	25.00	—	25.00	ns
R78	$\overline{\text{RSTCONF}}$ negated to data out high impedance (MAX = 0.00 × B1 + 25.00)	—	25.00	—	25.00	—	25.00	—	25.00	ns
R79	CLKOUT of last rising edge before chip three-states $\overline{\text{HRESET}}$ to data out high impedance (MAX = 0.00 × B1 + 25.00)	—	25.00	—	25.00	—	25.00	—	25.00	ns
R80	DSDI, DSCK setup (MIN = 3.00 × B1)	90.90	—	75.00	—	45.50	—	37.50	—	ns
R81	DSDI, DSCK hold time (MIN = 0.00 × B1 + 0.00)	0.00	—	0.00	—	0.00	—	0.00	—	ns
R82	$\overline{\text{SRESET}}$ negated to CLKOUT rising edge for DSDI and DSCK sample (MIN = 8.00 × B1)	242.40	—	200.00	—	121.20	—	100.00	—	ns

Figure 34 shows the reset timing for the data bus configuration.

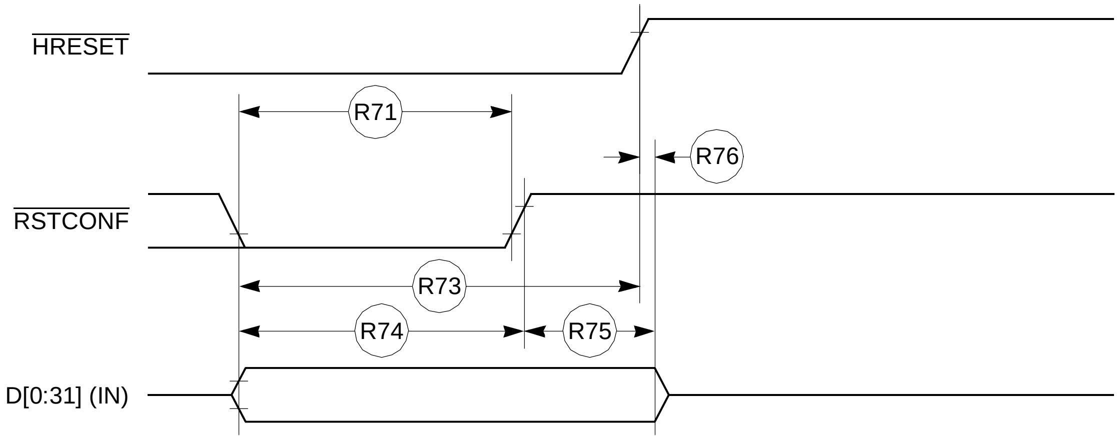


Figure 34. Reset Timing—Configuration from Data Bus

Figure 35 provides the reset timing for the data bus weak drive during configuration.

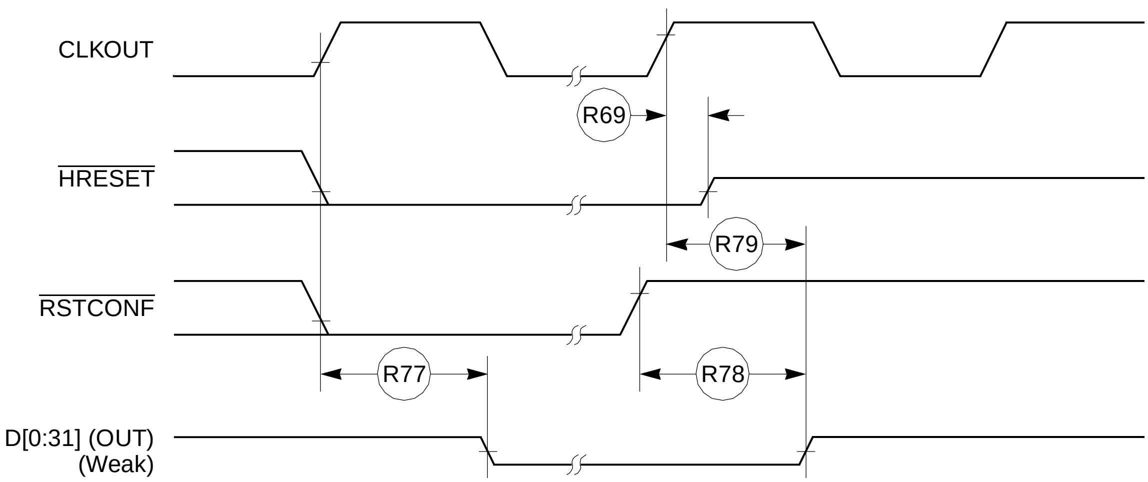


Figure 35. Reset Timing—Data Bus Weak Drive During Configuration

Figure 36 provides the reset timing for the debug port configuration.

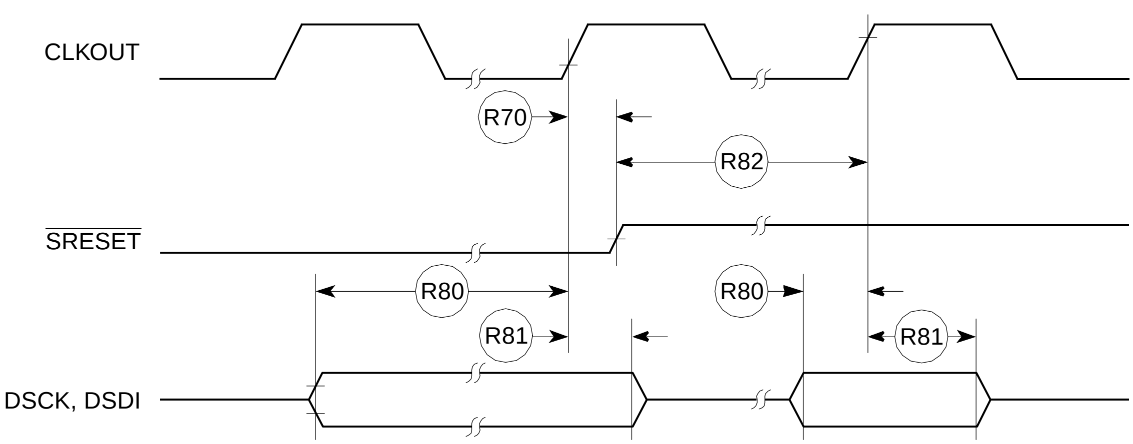


Figure 36. Reset Timing—Debug Port Configuration

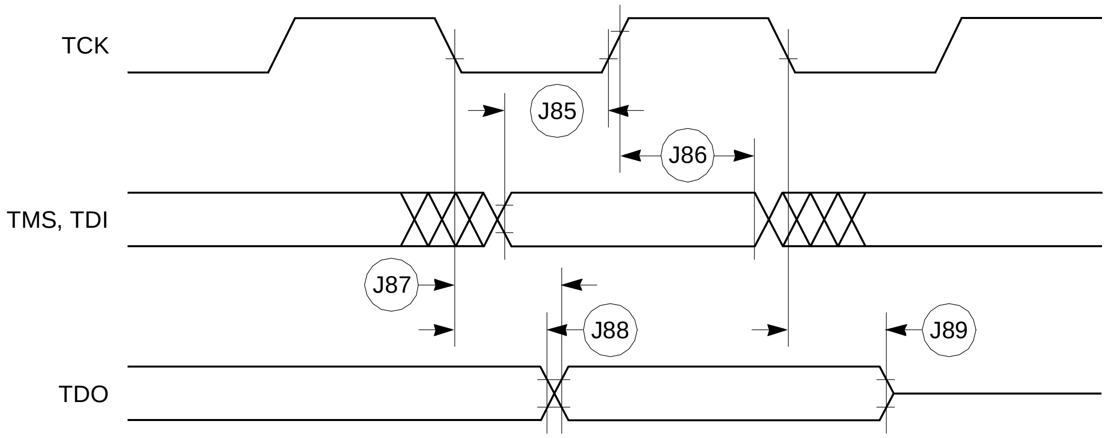


Figure 38. JTAG Test Access Port Timing Diagram

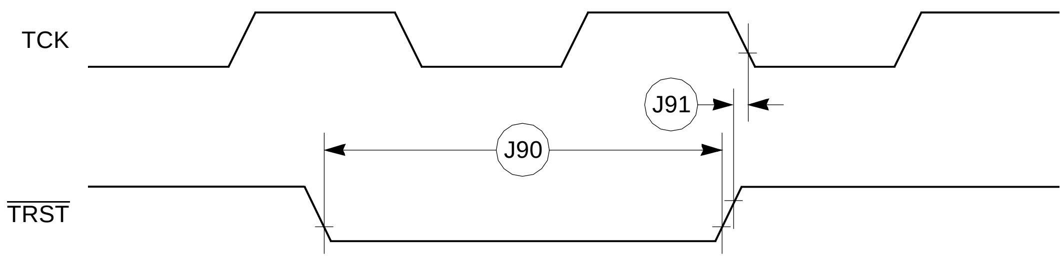


Figure 39. JTAG TRST Timing Diagram

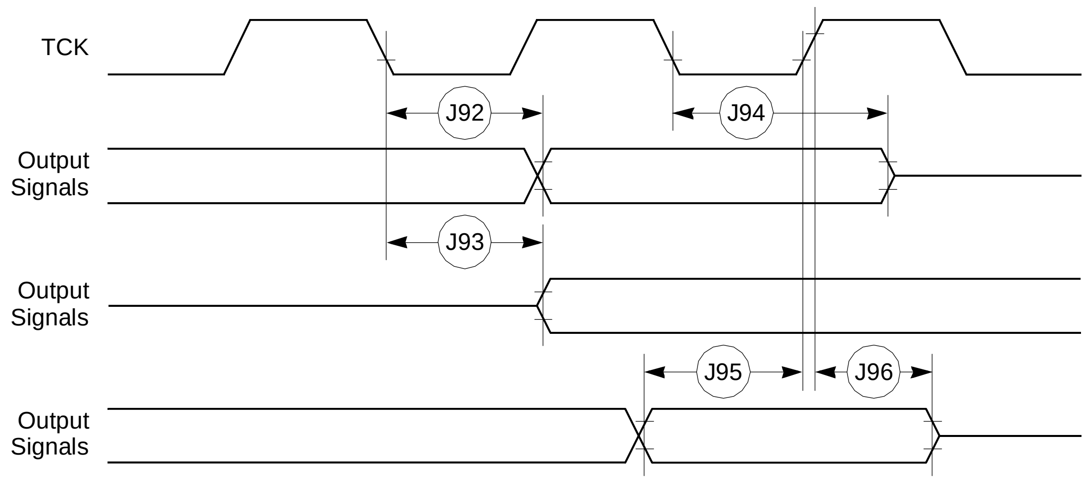


Figure 40. Boundary Scan (JTAG) Timing Diagram

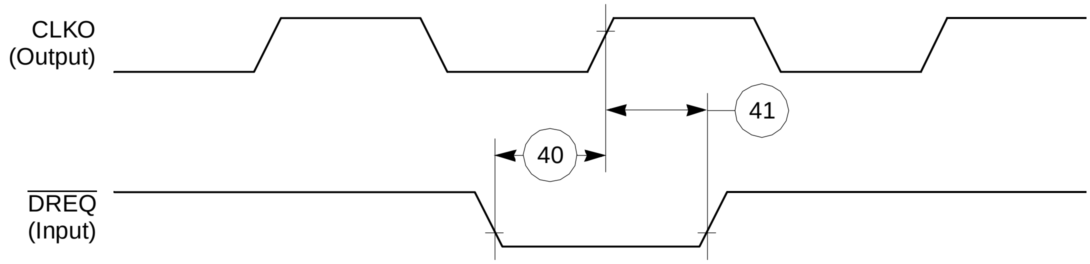


Figure 42. IDMA External Requests Timing Diagram

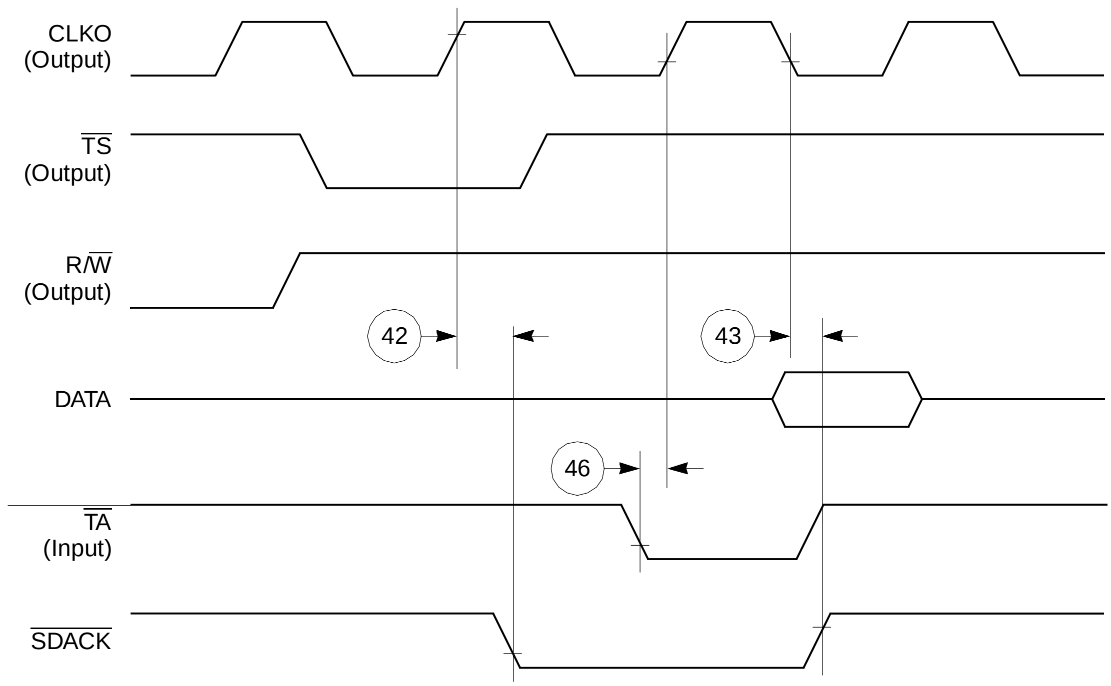
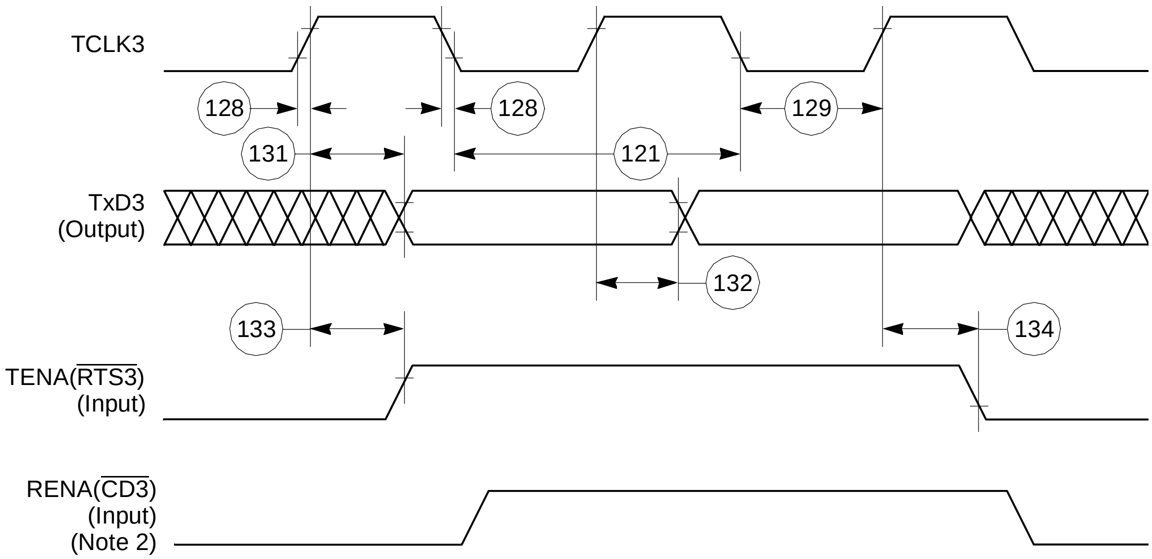


Figure 43. SDACK Timing Diagram—Peripheral Write, Externally-Generated TA



Notes:
1. Transmit clock invert (TCI) bit in GSMR is set.
2. If RENA is negated before TENA or RENA is not asserted at all during transmit, then the CSL bit is set in the buffer descriptor at the end of the frame transmission.

Figure 58. Ethernet Transmit Timing Diagram

13.8 SMC Transparent AC Electrical Specifications

Table 25 provides the SMC transparent timings as shown in Figure 59.

Table 25. SMC Transparent Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
150	SMCLK clock period[1]	100	—	ns
151	SMCLK width low	50	—	ns
151A	SMCLK width high	50	—	ns
152	SMCLK rise/fall time	—	15	ns
153	SMTXD active delay (from SMCLK falling edge)	10	50	ns
154	SMRXD/SMSYNC setup time	20	—	ns
155	RXD1/SMSYNC hold time	5	—	ns

[1] SYNCCLK must be at least twice as fast as SMCLK.

13.10 SPI Slave AC Electrical Specifications

Table 27 provides the SPI slave timings as shown in Figure 62 and Figure 63.

Table 27. SPI Slave Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
170	Slave cycle time	2	—	t_{cyc}
171	Slave enable lead time	15	—	ns
172	Slave enable lag time	15	—	ns
173	Slave clock (SPICLK) high or low time	1	—	t_{cyc}
174	Slave sequential transfer delay (does not require deselect)	1	—	t_{cyc}
175	Slave data setup time (inputs)	20	—	ns
176	Slave data hold time (inputs)	20	—	ns
177	Slave access time	—	50	ns

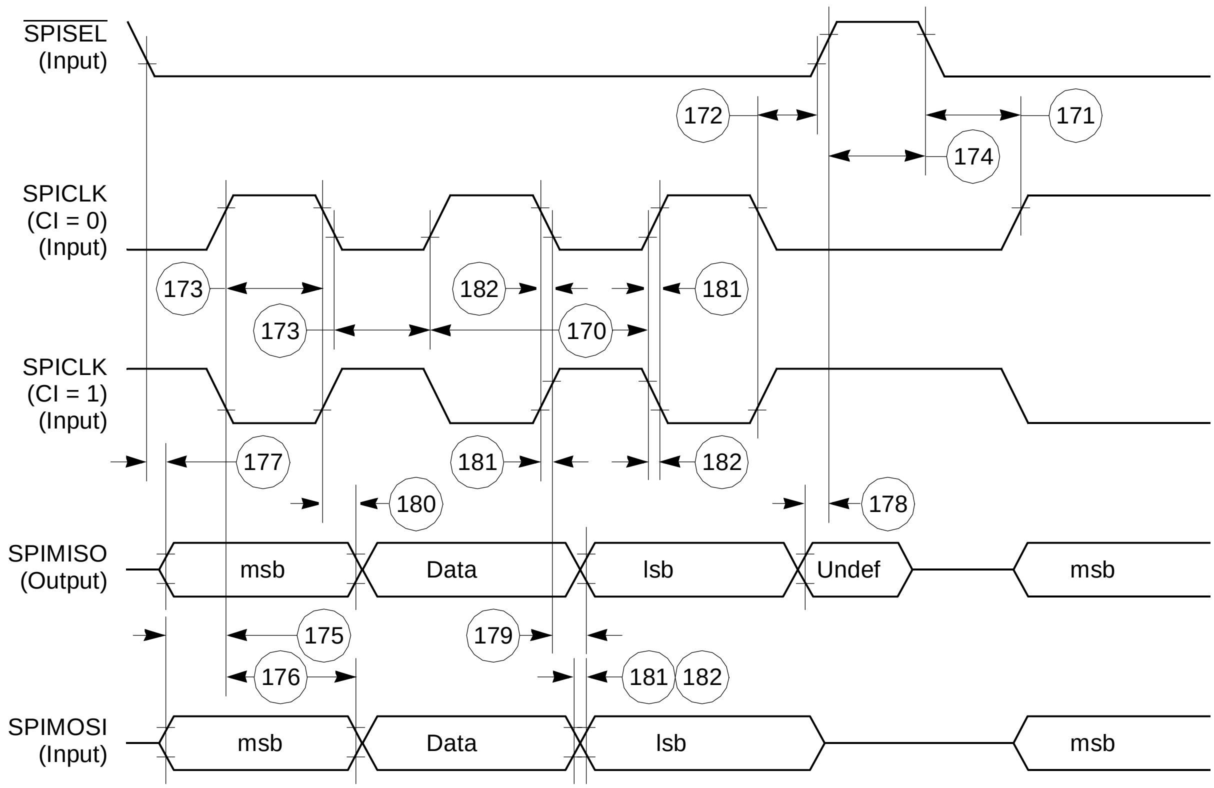


Figure 62. SPI Slave (CP = 0) Timing Diagram

Figure 66 shows the MII transmit signal timing diagram.

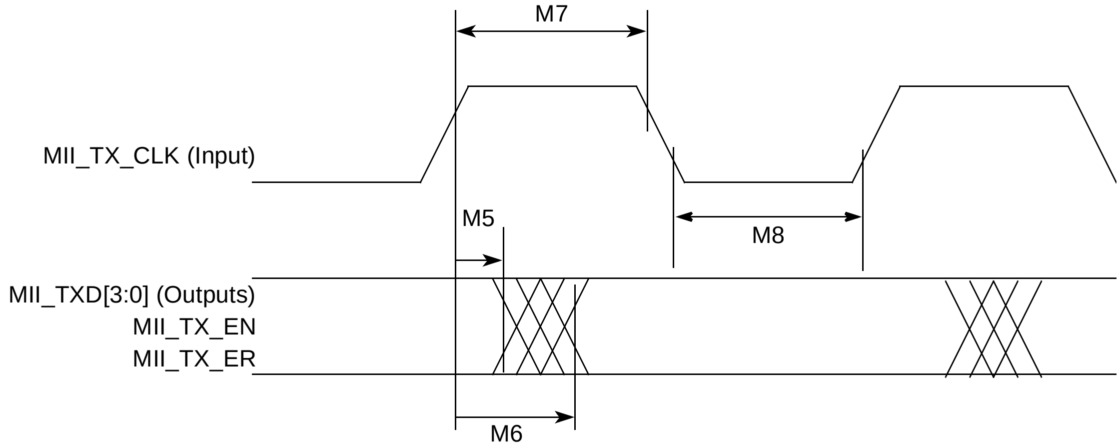


Figure 66. MII Transmit Signal Timing Diagram

15.3 MII Async Inputs Signal Timing (MII_CRS, MII_COL)

Table 33 provides information on the MII async inputs signal timing.

Table 33. MII Async Inputs Signal Timing

Num	Characteristic	Min	Max	Unit
M9	MII_CRS, MII_COL minimum pulse width	1.5	—	MII_TX_CLK period

Figure 67 shows the MII asynchronous inputs signal timing diagram.

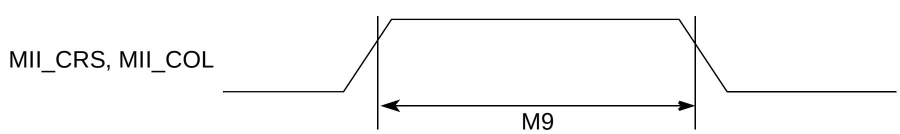


Figure 67. MII Async Inputs Timing Diagram

15.4 MII Serial Management Channel Timing (MII_MDIO, MII_MDC)

Table 34 provides information on the MII serial management channel signal timing. The FEC functions correctly with a maximum MDC frequency in excess of 2.5 MHz.

Table 34. MII Serial Management Channel Timing

Num	Characteristic	Min	Max	Unit
M10	MII_MDC falling edge to MII_MDIO output invalid (minimum propagation delay)	0	—	ns
M11	MII_MDC falling edge to MII_MDIO output valid (max prop delay)	—	25	ns
M12	MII_MDIO (input) to MII_MDC rising edge setup	10	—	ns
M13	MII_MDIO (input) to MII_MDC rising edge hold	0	—	ns
M14	MII_MDC pulse width high	40%	60%	MII_MDC period
M15	MII_MDC pulse width low	40%	60%	MII_MDC period

Table 36. Pin Assignments—JEDEC Standard (continued)

Name	Pin Number	Type
PB30, SPICLK	T17	Bidirectional (Optional: open-drain) (5-V tolerant)
PB29, SPIMOSI	R17	Bidirectional (Optional: open-drain) (5-V tolerant)
PB28, SPIMISO, BRGO4	R14	Bidirectional (Optional: open-drain) (5-V tolerant)
PB27, I2CSDA, BRGO1	N13	Bidirectional (Optional: open-drain)
PB26, I2CSCL, BRGO2	N12	Bidirectional (Optional: open-drain)
PB25, SMTXD1	U13	Bidirectional (Optional: open-drain) (5-V tolerant)
PB24, SMRXD1	T12	Bidirectional (Optional: open-drain) (5-V tolerant)
PB23, $\overline{\text{SDACK1}}$, $\overline{\text{SMSYN1}}$	U12	Bidirectional (Optional: open-drain)
PB19, MII1-RXD3, RTS4	T11	Bidirectional (Optional: open-drain)
PC15, $\overline{\text{DREQ0}}$, L1ST1	R15	Bidirectional (5-V tolerant)
PC13, MII1-TXD3, SDACK1	U9	Bidirectional (5-V tolerant)
PC12, MII1-TXD2, TOUT1	T15	Bidirectional (5-V tolerant)
PC11, USBRXP	P12	Bidirectional
PC10, USBRXN, $\overline{\text{TGATE1}}$	U11	Bidirectional
PC7, $\overline{\text{CTS4}}$, L1TSYNCB, USBTXP	T10	Bidirectional (5-V tolerant)
PC6, $\overline{\text{CD4}}$, L1RSYNCB, USBTXN	P10	Bidirectional (5-V tolerant)
PD8, RXD4, MII-MDC, RMII-MDC	T3	Bidirectional (5-V tolerant)
PE31, CLK8, L1TCLKB, MII1-RXCLK	P9	Bidirectional (Optional: open-drain)
PE30, L1RXDB, MII1-RXD2	R8	Bidirectional (Optional: open-drain)

Table 36. Pin Assignments—JEDEC Standard (continued)

Name	Pin Number	Type
PE29, MII2-CRS	U7	Bidirectional (Optional: open-drain)
PE28, TOUT3, MII2-COL	R7	Bidirectional (Optional: open-drain)
PE27, L1RQB, MII2-RXERR, RMII2-RXERR	T6	Bidirectional (Optional: open-drain)
PE26, L1CLKOB, MII2-RXDV, RMII2-CRS_DV	T2	Bidirectional (Optional: open-drain)
PE25, RXD4, MII2-RXD3, L1ST2	R4	Bidirectional (Optional: open-drain)
PE24, SMRXD1, BRGO1, MII2-RXD2	U8	Bidirectional (Optional: open-drain)
PE23, TXD4, MII2-RXCLK, L1ST1	U4	Bidirectional (Optional: open-drain)
PE22, TOUT2, MII2-RXD1, RMII2-RXD1, SDACK1	P4	Bidirectional (Optional: open-drain)
PE21, TOUT1, MII2-RXD0, RMII2-RXD0	T9	Bidirectional (Optional: open-drain)
PE20, MII2-TXER	U3	Bidirectional (Optional: open-drain)
PE19, L1TXDB, MII2-TXEN, RMII2-TXEN	R6	Bidirectional (Optional: open-drain)
PE18, SMTXD1, MII2-TXD3	M5	Bidirectional (Optional: open-drain)
PE17, TIN3, CLK5, BRGO3, SMSYN1, MII2-TXD2	T8	Bidirectional (Optional: open-drain)
PE16, L1RCLKB, CLK6, MII2-TXCLK, RMII2-REFCLK	U6	Bidirectional (Optional: open-drain)
PE15, TGATE1, MII2-TXD1, RMII2-TXD1	T7	Bidirectional
PE14, MII2-TXD0, RMII2-TXD0	P8	Bidirectional
TMS	T14	Input (5-V tolerant)
TDI, DSDI	T13	Input (5-V tolerant)
TCK, DSCK	R13	Input (5-V tolerant)
TRST	U14	Input (5-V tolerant)

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Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku
Tokyo 153-0064
Japan
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+81 3 5437 9125
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