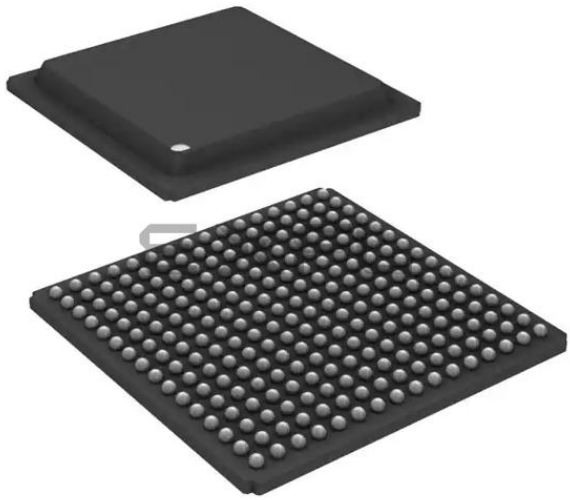

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	80MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (2)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TA)
Security Features	-
Package / Case	256-BBGA
Supplier Device Package	256-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc870vr80

Figure 19 provides the timing for the external bus controlled by the UPM.

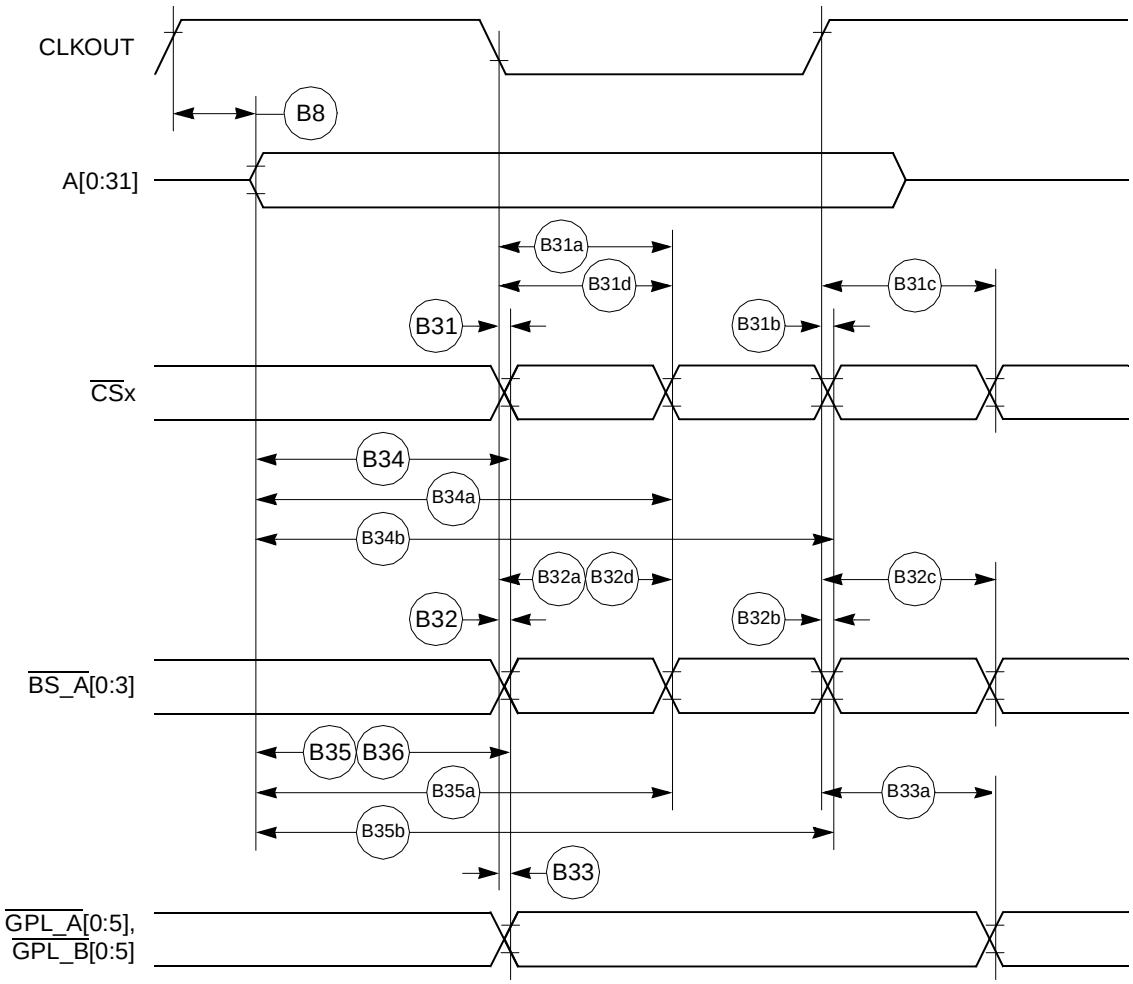


Figure 19. External Bus Timing (UPM Controlled Signals)

Figure 27 provides the PCMCIA access cycle timing for the external bus read.

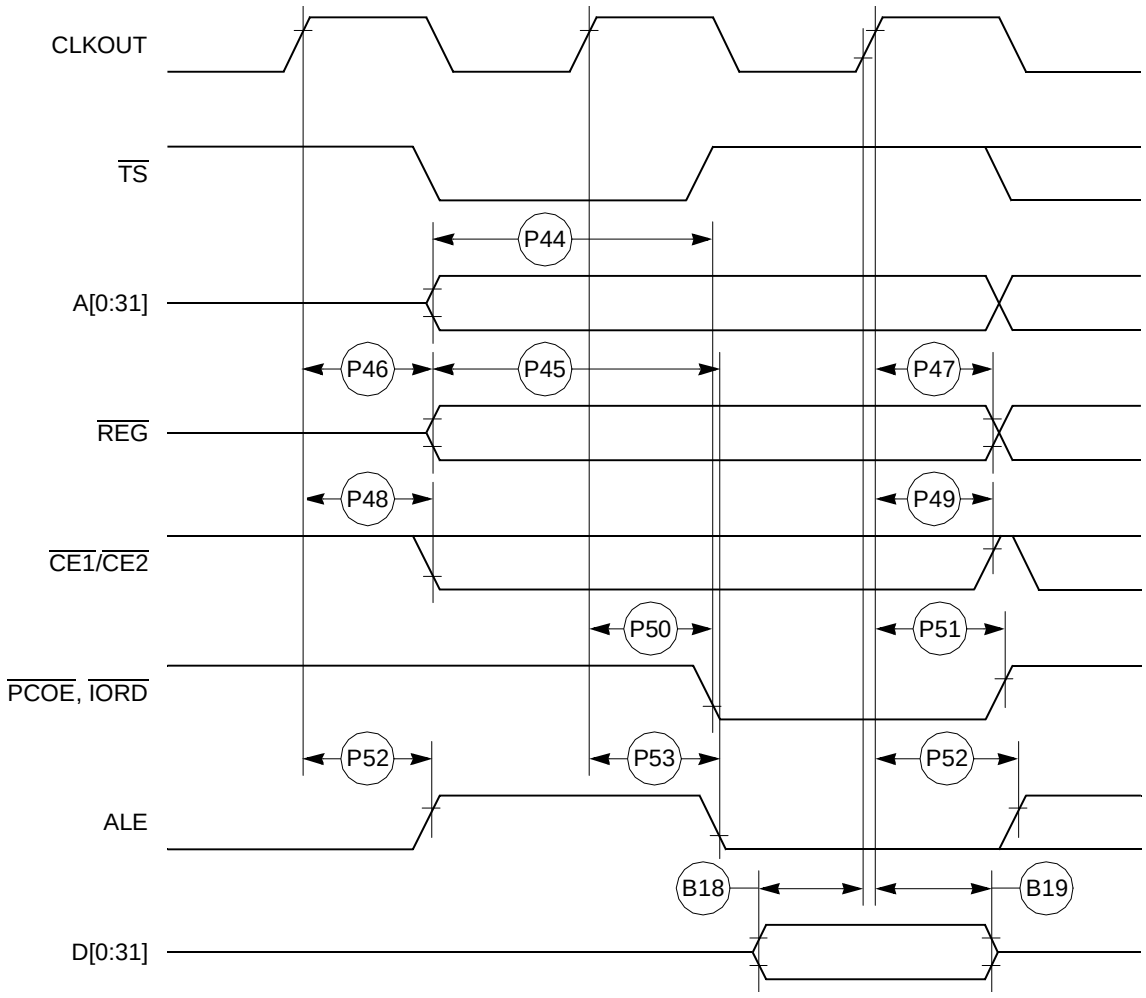


Figure 27. PCMCIA Access Cycles Timing External Bus Read

Figure 28 provides the PCMCIA access cycle timing for the external bus write.

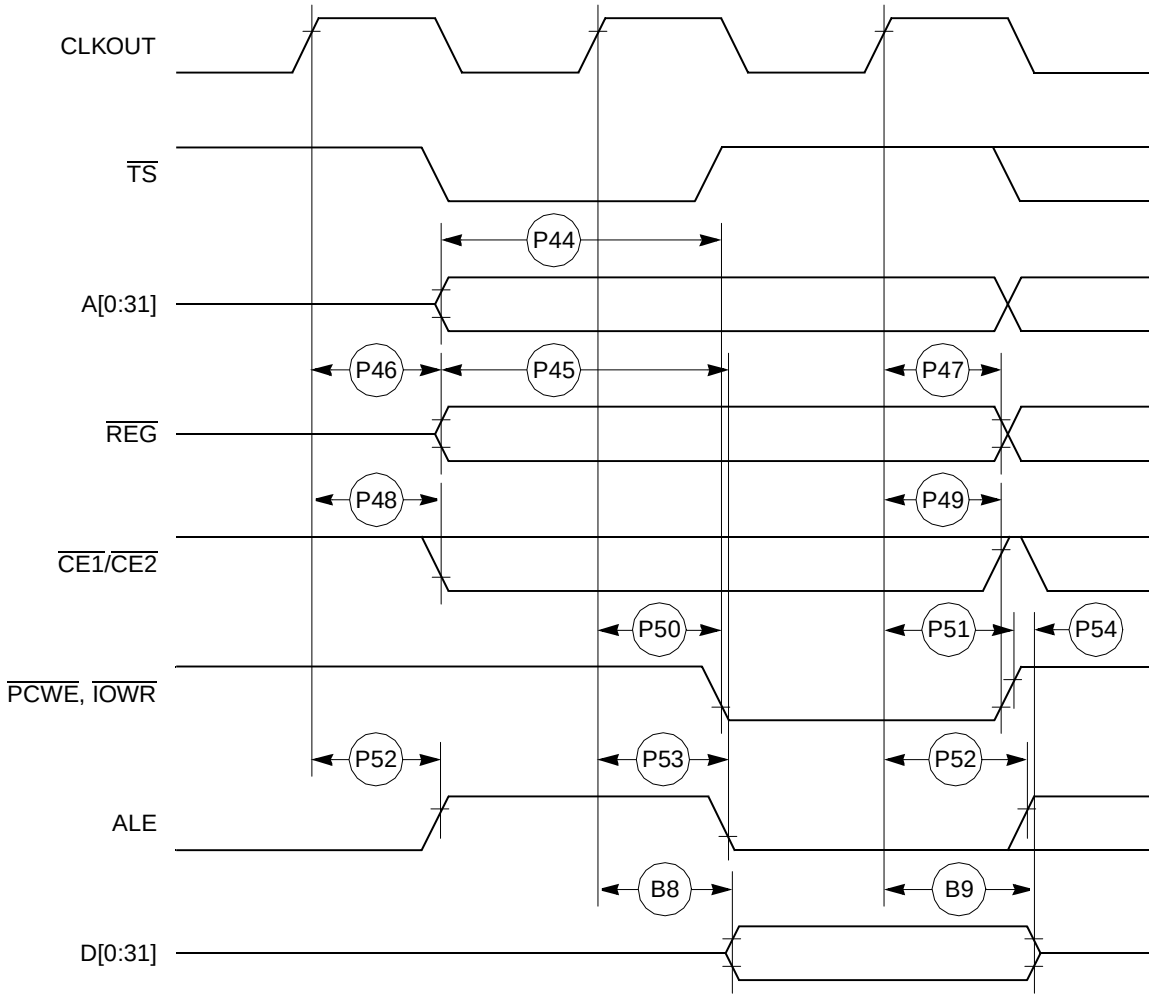


Figure 28. PCMCIA Access Cycles Timing External Bus Write

Figure 29 provides the PCMCIA WAIT signals detection timing.

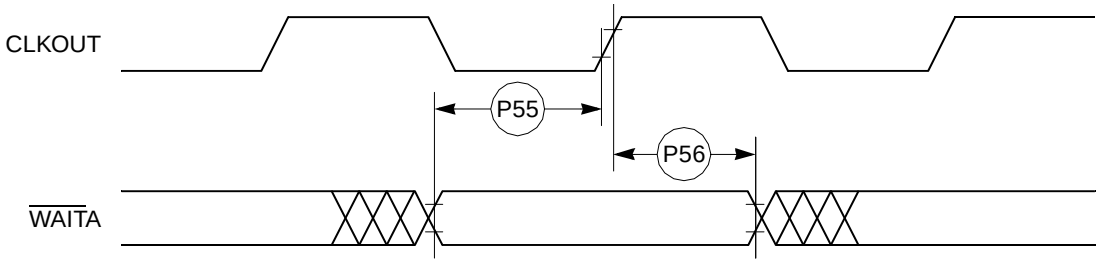


Figure 29. PCMCIA WAIT Signals Detection Timing

Table 14 shows the debug port timing for the MPC875/MPC870.

Table 14. Debug Port Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
D61	DSCK cycle time	$3 \times T_{CLOCKOUT}$		—
D62	DSCK clock pulse width	$1.25 \times T_{CLOCKOUT}$		—
D63	DSCK rise and fall times	0.00	3.00	ns
D64	DSDI input data setup time	8.00		ns
D65	DSDI data hold time	5.00		ns
D66	DSCK low to DSDO data valid	0.00	15.00	ns
D67	DSCK low to DSDO invalid	0.00	2.00	ns

Figure 32 provides the input timing for the debug port clock.

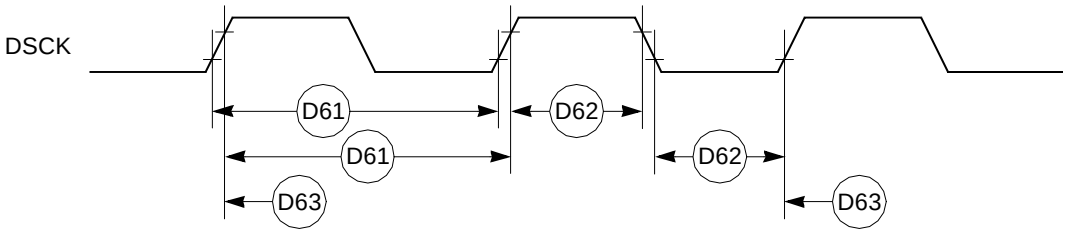


Figure 32. Debug Port Clock Input Timing

Figure 33 provides the timing for the debug port.

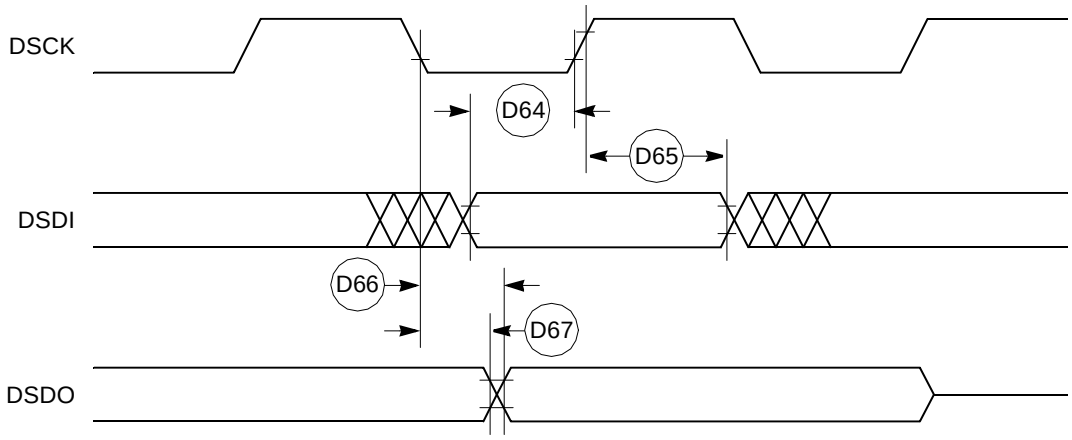


Figure 33. Debug Port Timings

12 IEEE 1149.1 Electrical Specifications

Table 16 provides the JTAG timings for the MPC875/MPC870 shown in Figure 37 through Figure 40.

Table 16. JTAG Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
J82	TCK cycle time	100.00	—	ns
J83	TCK clock pulse width measured at 1.5 V	40.00	—	ns
J84	TCK rise and fall times	0.00	10.00	ns
J85	TMS, TDI data setup time	5.00	—	ns
J86	TMS, TDI data hold time	25.00	—	ns
J87	TCK low to TDO data valid	—	27.00	ns
J88	TCK low to TDO data invalid	0.00	—	ns
J89	TCK low to TDO high impedance	—	20.00	ns
J90	$\overline{\text{TRST}}$ assert time	100.00	—	ns
J91	$\overline{\text{TRST}}$ setup time to TCK low	40.00	—	ns
J92	TCK falling edge to output valid	—	50.00	ns
J93	TCK falling edge to output valid out of high impedance	—	50.00	ns
J94	TCK falling edge to output high impedance	—	50.00	ns
J95	Boundary scan input valid to TCK rising edge	50.00	—	ns
J96	TCK rising edge to boundary scan input invalid	50.00	—	ns

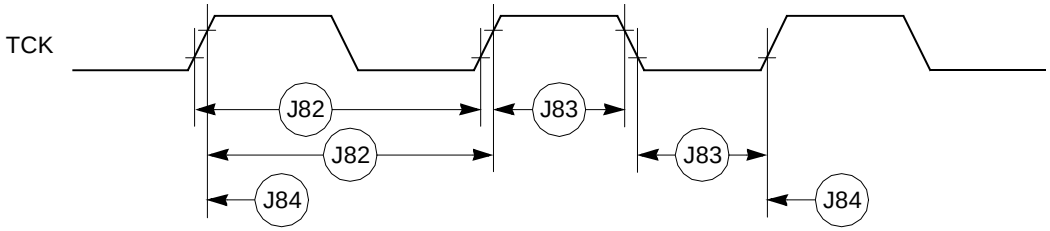


Figure 37. JTAG Test Clock Input Timing

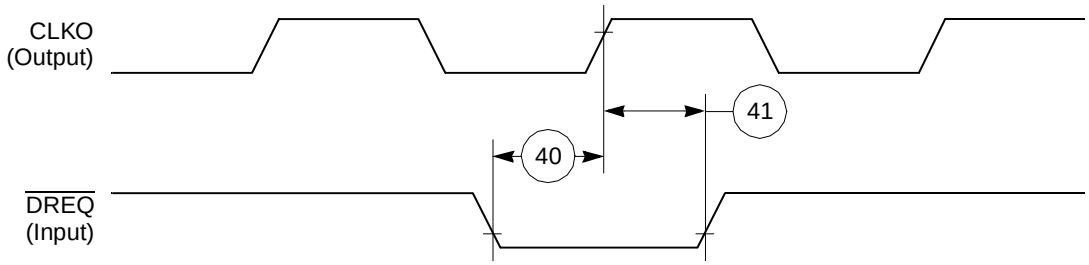


Figure 42. IDMA External Requests Timing Diagram

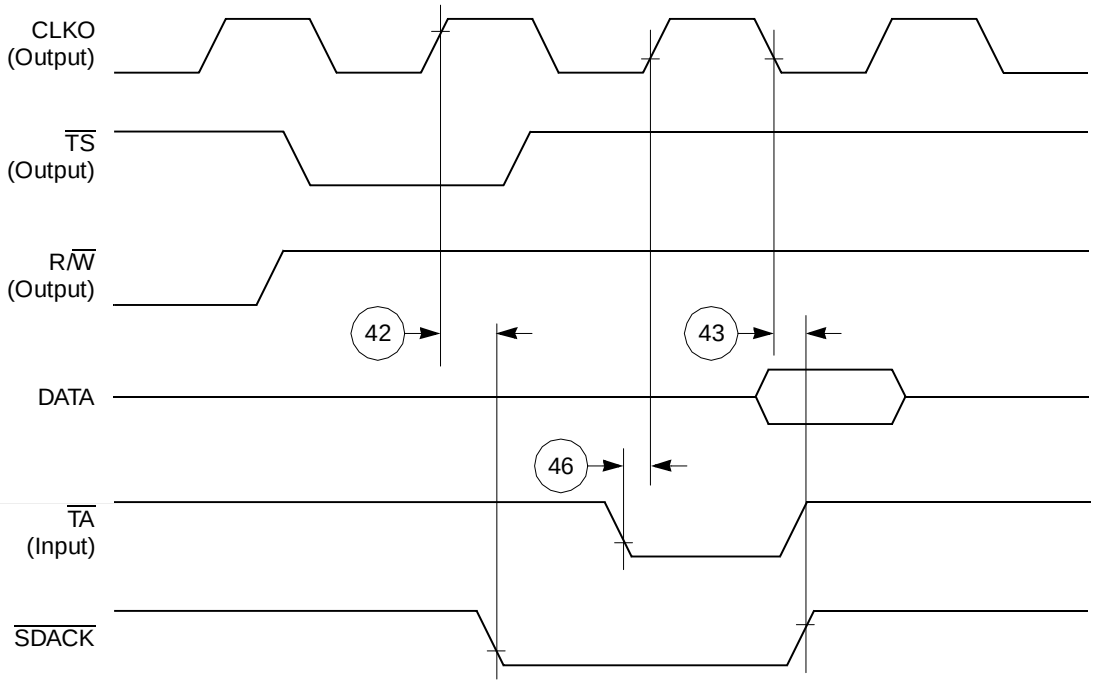


Figure 43. SDACK Timing Diagram—Peripheral Write, Externally-Generated TA

Figure 53 through Figure 55 show the NMSI timings.

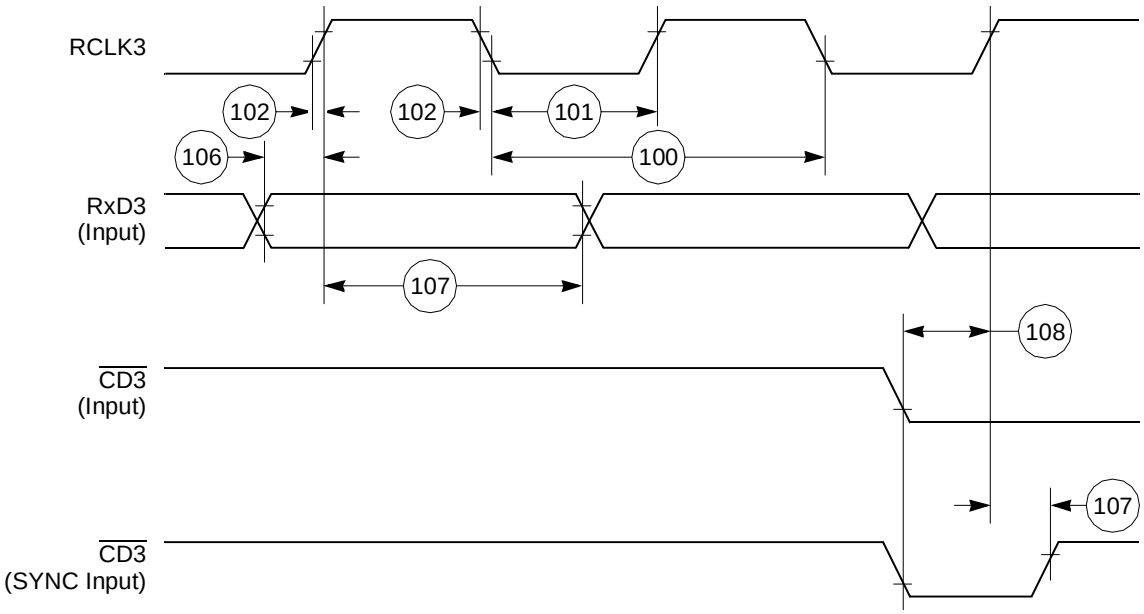


Figure 53. SCC NMSI Receive Timing Diagram

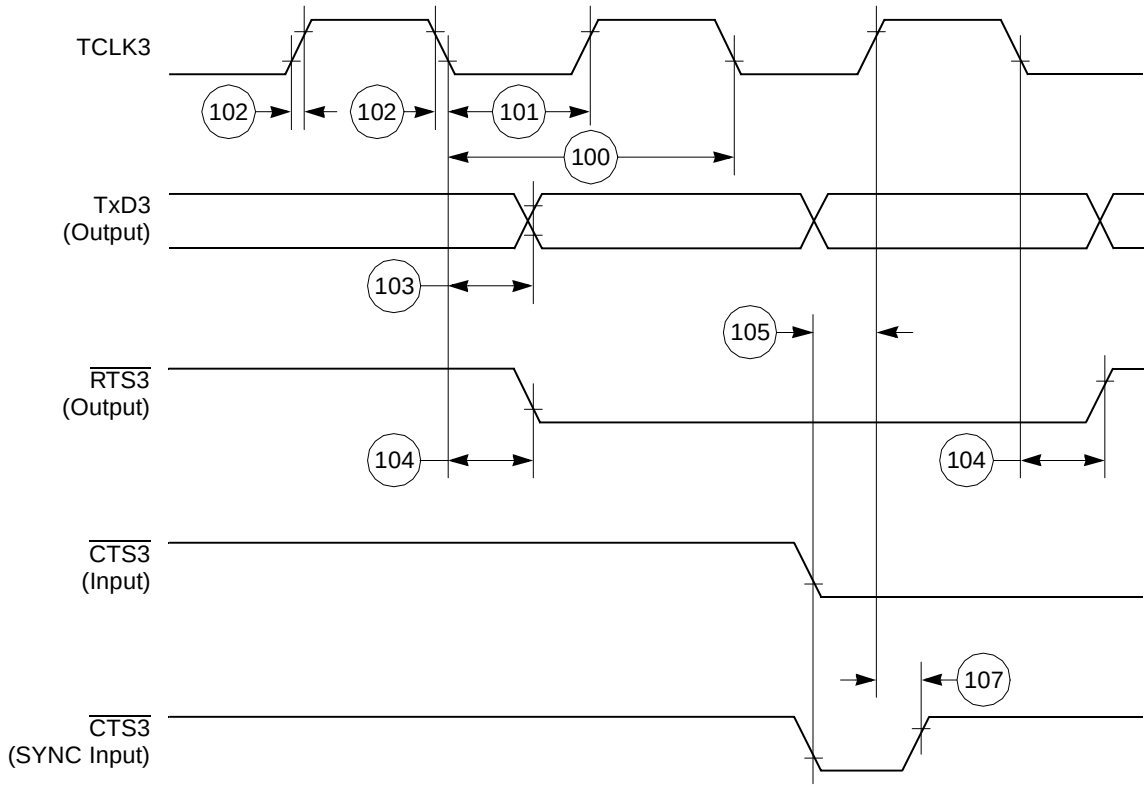


Figure 54. SCC NMSI Transmit Timing Diagram

Table 24. Ethernet Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
138	CLKO1 low to $\overline{\text{SDACK}}$ asserted[2]	—	20	ns
139	CLKO1 low to $\overline{\text{SDACK}}$ negated[2]	—	20	ns

1 The ratios SYNCCLK/RCLK3 and SYNCCLK/TCLK3 must be greater than or equal to 2/1.

2 $\overline{\text{SDACK}}$ is asserted whenever the SDMA writes the incoming frame DA into memory.

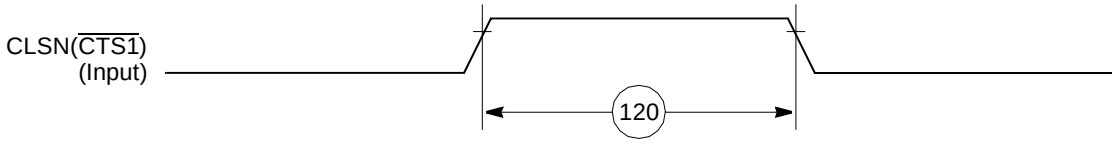


Figure 56. Ethernet Collision Timing Diagram

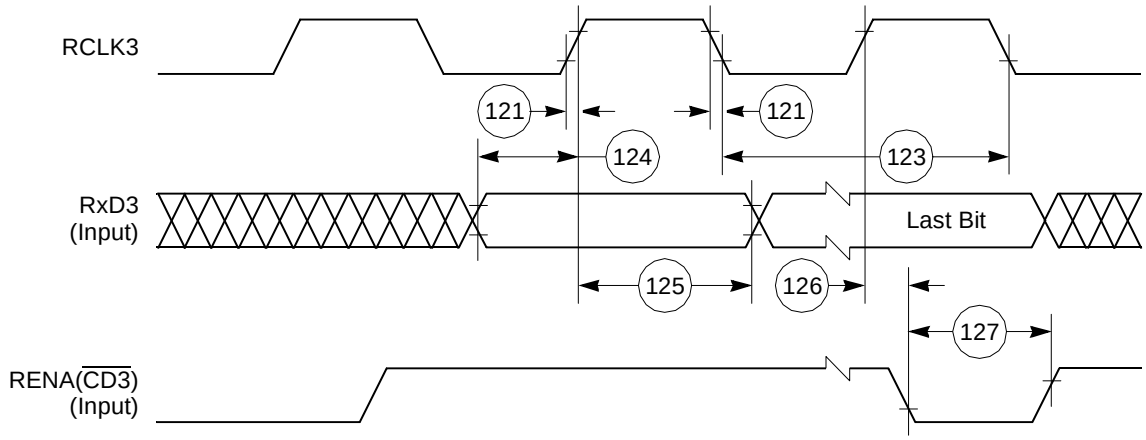
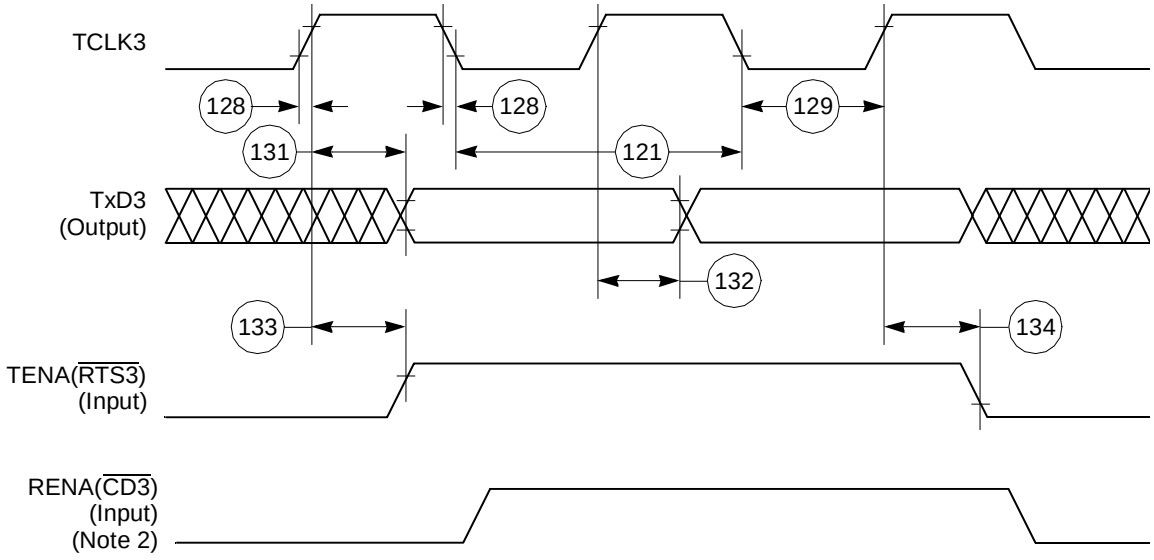


Figure 57. Ethernet Receive Timing Diagram



Notes:
1. Transmit clock invert (TCI) bit in GSMR is set.
2. If RENA is negated before TENA or RENA is not asserted at all during transmit, then the CSL bit is set in the buffer descriptor at the end of the frame transmission.

Figure 58. Ethernet Transmit Timing Diagram

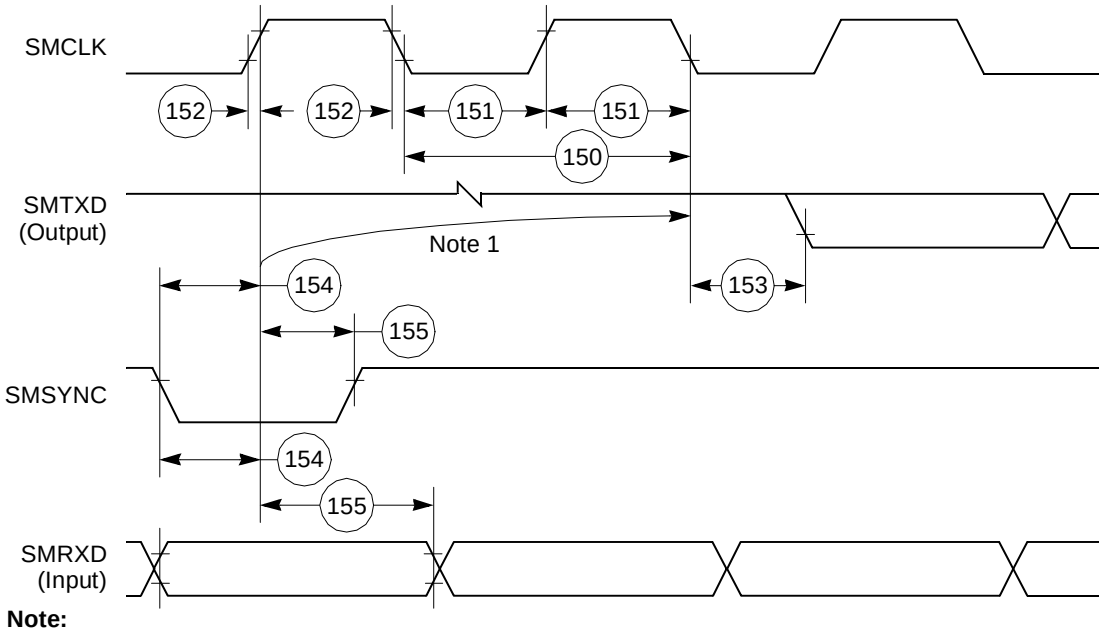
13.8 SMC Transparent AC Electrical Specifications

Table 25 provides the SMC transparent timings as shown in Figure 59.

Table 25. SMC Transparent Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
150	SMCLK clock period[1]	100	—	ns
151	SMCLK width low	50	—	ns
151A	SMCLK width high	50	—	ns
152	SMCLK rise/fall time	—	15	ns
153	SMTXD active delay (from SMCLK falling edge)	10	50	ns
154	SMRXD/SMSYNC setup time	20	—	ns
155	RXD1/SMSYNC hold time	5	—	ns

1 SYNCCLK must be at least twice as fast as SMCLK.



Note:
1. This delay is equal to an integer number of character-length clocks.

Figure 59. SMC Transparent Timing Diagram

13.9 SPI Master AC Electrical Specifications

Table 26 provides the SPI master timings as shown in Figure 60 and Figure 61.

Table 26. SPI Master Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
160	Master cycle time	4	1024	t_{cyc}
161	Master clock (SCK) high or low time	2	512	t_{cyc}
162	Master data setup time (inputs)	15	—	ns
163	Master data hold time (inputs)	0	—	ns
164	Master data valid (after SCK edge)	—	10	ns
165	Master data hold time (outputs)	0	—	ns
166	Rise time output	—	15	ns
167	Fall time output	—	15	ns

Table 28. I²C Timing (SCL < 100 kHz) (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
210	SDL/SCL fall time	—	300	ns
211	Stop condition setup time	4.7	—	µs

1 SCL frequency is given by SCL = BRGCLK_frequency/((BRG register + 3) × pre_scalar × 2).
The ratio SYNCCLK/(BRGCLK/pre_scalar) must be greater than or equal to 4/1.

Table 29 provides the I²C (SCL > 100 kHz) timings.

Table 29. I²C Timing (SCL > 100 kHz)

Num	Characteristic	Expression	All Frequencies		Unit
			Min	Max	
200	SCL clock frequency (slave)	fSCL	0	BRGCLK/48	Hz
200	SCL clock frequency (master)[1]	fSCL	BRGCLK/16512	BRGCLK/48	Hz
202	Bus free time between transmissions	—	1/(2.2 × fSCL)	—	s
203	Low period of SCL	—	1/(2.2 × fSCL)	—	s
204	High period of SCL	—	1/(2.2 × fSCL)	—	s
205	Start condition setup time	—	1/(2.2 × fSCL)	—	s
206	Start condition hold time	—	1/(2.2 × fSCL)	—	s
207	Data hold time	—	0	—	s
208	Data setup time	—	1/(40 × fSCL)	—	s
209	SDL/SCL rise time	—	—	1/(10 × fSCL)	s
210	SDL/SCL fall time	—	—	1/(33 × fSCL)	s
211	Stop condition setup time	—	1/2(2.2 × fSCL)	—	s

1 SCL frequency is given by SCL = BRGCLK_frequency/((BRG register + 3) × pre_scalar × 2).
The ratio SYNCCLK/(BRGCLK/pre_scalar) must be greater than or equal to 4/1.

Figure 64 shows the I²C bus timing.

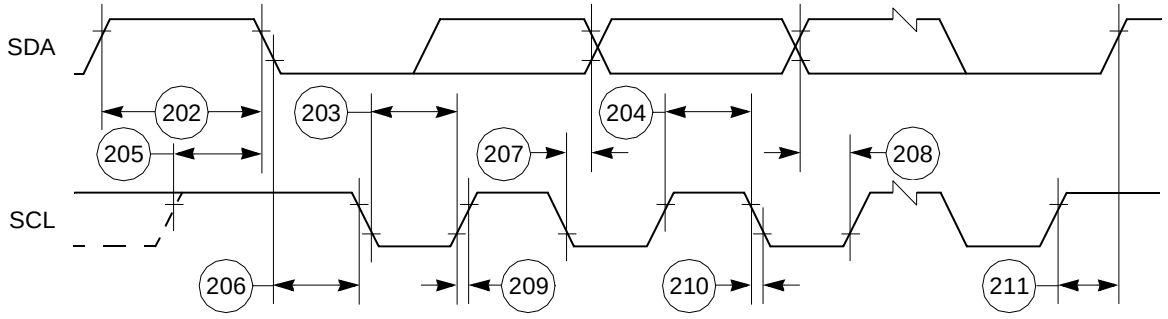


Figure 64. I²C Bus Timing Diagram

14 USB Electrical Characteristics

This section provides the AC timings for the USB interface.

14.1 USB Interface AC Timing Specifications

The USB Port uses the transmit clock on SCC1. Table 30 lists the USB interface timings.

Table 30. USB Interface AC Timing Specifications

Name	Characteristic	All Frequencies		Unit
		Min	Max	
US1	USBCLK frequency of operation[1] Low speed Full speed	 6 48		MHz
US4	USBCLK duty cycle (measured at 1.5 V)	45	55	%

1 USBCLK accuracy should be ±500 ppm or better. USBCLK may be stopped to conserve power.

15 FEC Electrical Characteristics

This section provides the AC electrical specifications for the Fast Ethernet controller (FEC). Note that the timing specifications for the MII signals are independent of system clock frequency (part speed designation). Also, MII signals use TTL signal levels compatible with devices operating at either 5.0 or 3.3 V.

15.1 MII and Reduced MII Receive Signal Timing

The receiver functions correctly up to a MII_RX_CLK maximum frequency of 25 MHz + 1%. The reduced MII (RMII) receiver functions correctly up to a RMII_REFCLK maximum frequency of 50 MHz + 1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_RX_CLK frequency – 1%.

Table 31 provides information on the MII receive signal timing.

Table 31. MII Receive Signal Timing

Num	Characteristic	Min	Max	Unit
M1	MII_RXD[3:0], MII_RX_DV, MII_RX_ER to MII_RX_CLK setup	5	—	ns
M2	MII_RX_CLK to MII_RXD[3:0], MII_RX_DV, MII_RX_ER hold	5	—	ns
M3	MII_RX_CLK pulse width high	35%	65%	MII_RX_CLK period
M4	MII_RX_CLK pulse width low	35%	65%	MII_RX_CLK period
M1_RMII	RMII_RXD[1:0], RMII_CRS_DV, RMII_RX_ERR to RMII_REFCLK setup	4	—	ns
M2_RMII	RMII_REFCLK to RMII_RXD[1:0], RMII_CRS_DV, RMII_RX_ERR hold	2	—	ns

Figure 65 shows MII receive signal timing.

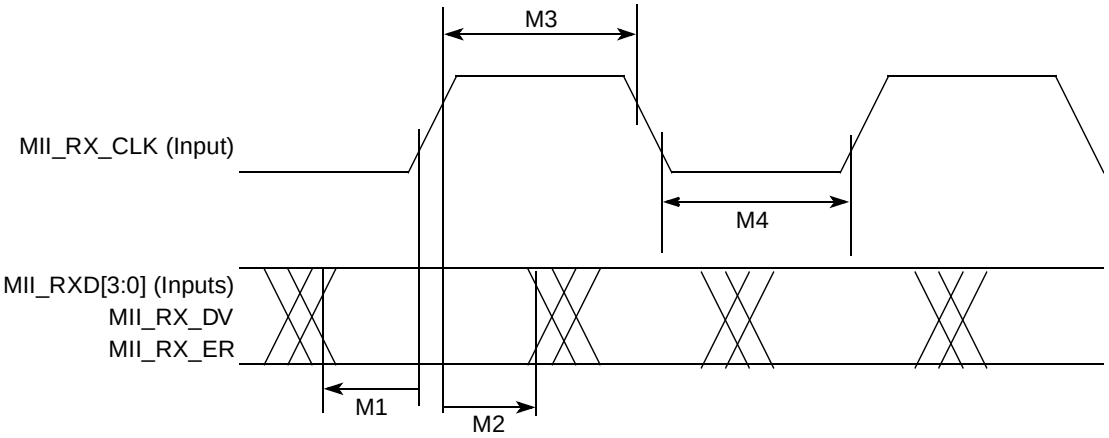


Figure 65. MII Receive Signal Timing Diagram

15.2 MII and Reduced MII Transmit Signal Timing

The transmitter functions correctly up to a MII_TX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_TX_CLK frequency – 1%.

Table 32 provides information on the MII transmit signal timing.

Table 32. MII Transmit Signal Timing

Num	Characteristic	Min	Max	Unit
M5	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER invalid	5	—	ns
M6	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER valid	—	25	ns
M7	MII_TX_CLK pulse width high	35%	65%	MII_TX_CLK period
M8	MII_TX_CLK pulse width low	35%	65%	MII_TX_CLK period
M20_RMII	RMII_TXD[1:0], RMII_TX_EN to RMII_REFCLK setup	4	—	ns
M21_RMII	RMII_TXD[1:0], RMII_TX_EN data hold from RMII_REFCLK rising edge	2	—	ns

Figure 66 shows the MII transmit signal timing diagram.

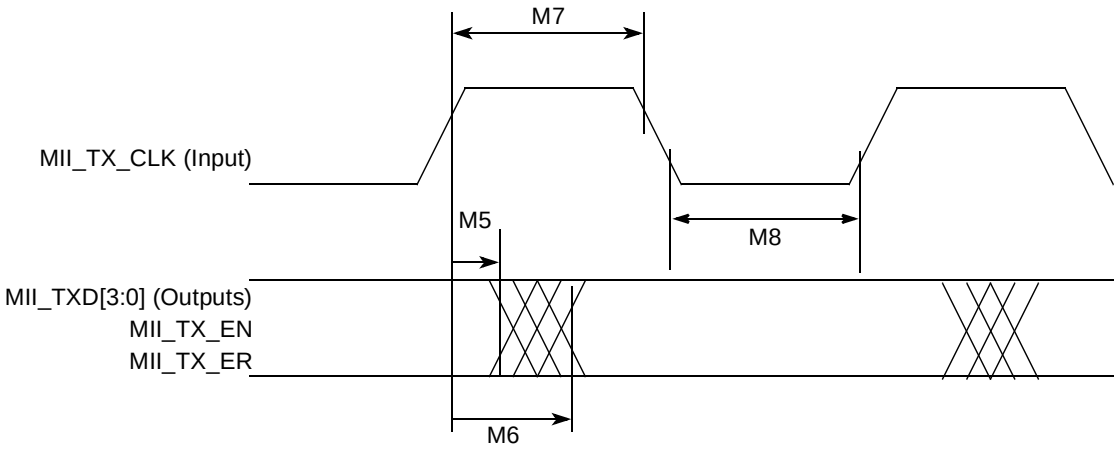


Figure 66. MII Transmit Signal Timing Diagram

15.3 MII Async Inputs Signal Timing (MII_CRS, MII_COL)

Table 33 provides information on the MII async inputs signal timing.

Table 33. MII Async Inputs Signal Timing

Num	Characteristic	Min	Max	Unit
M9	MII_CRS, MII_COL minimum pulse width	1.5	—	MII_TX_CLK period

Figure 67 shows the MII asynchronous inputs signal timing diagram.

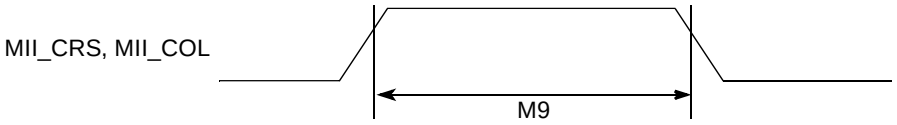


Figure 67. MII Async Inputs Timing Diagram

15.4 MII Serial Management Channel Timing (MII_MDIO, MII_MDC)

Table 34 provides information on the MII serial management channel signal timing. The FEC functions correctly with a maximum MDC frequency in excess of 2.5 MHz.

Table 34. MII Serial Management Channel Timing

Num	Characteristic	Min	Max	Unit
M10	MII_MDC falling edge to MII_MDIO output invalid (minimum propagation delay)	0	—	ns
M11	MII_MDC falling edge to MII_MDIO output valid (max prop delay)	—	25	ns
M12	MII_MDIO (input) to MII_MDC rising edge setup	10	—	ns
M13	MII_MDIO (input) to MII_MDC rising edge hold	0	—	ns
M14	MII_MDC pulse width high	40%	60%	MII_MDC period
M15	MII_MDC pulse width low	40%	60%	MII_MDC period

16 Mechanical Data and Ordering Information

Table 35 identifies the packages and operating frequencies available for the MPC875/MPC870.

Table 35. Available MPC875/MPC870 Packages/Frequencies

Package Type	Temperature (T_J)	Frequency (MHz)	Order Number
Plastic ball grid array ZT suffix—Leaded VR suffix—Lead-Free are available as needed	0°C to 95°C	66	KMPC875ZT66 KMPC870ZT66 MPC875ZT66 MPC870ZT66
		80	KMPC875ZT80 KMPC870ZT80 MPC875ZT80 MPC870ZT80
		133	KMPC875ZT133 KMPC870ZT133 MPC875ZT133 MPC870ZT133
Plastic ball grid array CZT suffix—Leaded CVR suffix—Lead-Free are available as needed	-40°C to 100°C	66	KMPC875CZT66 KMPC870CZT66 MPC875CZT66 MPC870CZT66
		133	KMPC875CZT133 KMPC870CZT133 MPC875CZT133 MPC870CZT133

Table 36. Pin Assignments—JEDEC Standard (continued)

Name	Pin Number	Type
PB30, SPICLK	T17	Bidirectional (Optional: open-drain) (5-V tolerant)
PB29, SPIMOSI	R17	Bidirectional (Optional: open-drain) (5-V tolerant)
PB28, SPIMISO, BRGO4	R14	Bidirectional (Optional: open-drain) (5-V tolerant)
PB27, I2CSDA, BRGO1	N13	Bidirectional (Optional: open-drain)
PB26, I2CSCL, BRGO2	N12	Bidirectional (Optional: open-drain)
PB25, SMTXD1	U13	Bidirectional (Optional: open-drain) (5-V tolerant)
PB24, SMRXD1	T12	Bidirectional (Optional: open-drain) (5-V tolerant)
PB23, $\overline{\text{SDACK1}}$, $\overline{\text{SMSYN1}}$	U12	Bidirectional (Optional: open-drain)
PB19, MII1-RXD3, RTS4	T11	Bidirectional (Optional: open-drain)
PC15, $\overline{\text{DREQ0}}$, L1ST1	R15	Bidirectional (5-V tolerant)
PC13, MII1-TXD3, SDACK1	U9	Bidirectional (5-V tolerant)
PC12, MII1-TXD2, TOUT1	T15	Bidirectional (5-V tolerant)
PC11, USBRXP	P12	Bidirectional
PC10, USBRXN, $\overline{\text{TGATE1}}$	U11	Bidirectional
PC7, $\overline{\text{CTS4}}$, L1TSYNCB, USBTXP	T10	Bidirectional (5-V tolerant)
PC6, $\overline{\text{CD4}}$, L1RSYNCB, USBTXN	P10	Bidirectional (5-V tolerant)
PD8, RXD4, MII-MDC, RMII-MDC	T3	Bidirectional (5-V tolerant)
PE31, CLK8, L1TCLKB, MII1-RXCLK	P9	Bidirectional (Optional: open-drain)
PE30, L1RXDB, MII1-RXD2	R8	Bidirectional (Optional: open-drain)

17 Document Revision History

Table 37 lists significant changes between revisions of this hardware specification.

Table 37. Document Revision History

Revision Number	Date	Changes
0	2/2003	Initial release.
0.1	3/2003	Took out the time-slot assigner and changed the SCC for SCC3 to SCC4.
0.2	5/2003	Changed the package drawing, removed all references to Data Parity. Changed the SPI Master Timing Specs. 162 and 164. Added the RMII and USB timing. Added the 80-MHz timing.
0.3	5/2003	Made sure the pin types were correct. Changed the Features list to agree with the MPC885.
0.4	5/2003	Corrected the signals that had overlines on them. Made corrections on two pins that were typos.
0.5	5/2003	Changed the pin descriptions for PD8 and PD9.
0.6	5/2003	Changed a few typos. Put back the I^2C. Put in the new reset configuration, corrected the USB timing.
0.7	6/2003	Changed the pin descriptions per the June 22 spec, removed Utopia from the pin descriptions, changed PADIR, PBDIR, PCDIR and PDDIR to be 0 in the Mandatory Reset Config.
0.8	8/2003	Added the reference to USB 2.0 to the Features list and removed 1.1 from USB on the block diagrams.
0.9	8/2003	Changed the USB description to full-/low-speed compatible.
1.0	9/2003	Added the DSP information in the Features list. Put a new sentence under Mechanical Dimensions. Fixed table formatting. Nontechnical edits. Released to the external web.
1.1	10/2003	Added TDMb to the MPC875 Features list, the MPC875 Block Diagram, added 13.5 Serial Interface AC Electrical Specifications, and removed TDMa from the pin descriptions.
2.0	12/2003	Changed DBGC in the Mandatory Reset Configuration to X1. Changed the maximum operating frequency to 133 MHz. Put the timing in the 80 MHz column. Put in the orderable part numbers. Rounded the timings to hundredths in the 80 MHz column. Put the pin numbers in footnotes by the maximum currents in Table 6. Changed 22 and 41 in the Timing. Put TBD in the Thermal table.

Table 37. Document Revision History (continued)

Revision Number	Date	Changes
3.0	1/07/2004 7/19/2004	• Added sentence to Spec B1A about EXTCLK and CLKOUT being in alignment for integer values. • Added a footnote to Spec 41 specifying that EDM = 1. • Added the thermal numbers to Table 4. • Added RMII1_EN under M1II_EN in Table 36, Pin Assignments. • Added a table footnote to Table 6, DC Electrical Specifications, about meeting the V_{IL} Max of the I^2C Standard. • Put the new part numbers in the Ordering Information Section.
4	08/2007	• Updated template. • On page 1, updated first paragraph and added a second paragraph. • After Table 2, inserted a new figure showing the undershoot/overshoot voltage (Figure 3) and renumbered the rest of the figures. • In Table 10, for reset timings B29f and B29g added footnote indicating that the formula only applies to bus operation up to 50 MHz. • In Figure 5, changed all reference voltage measurement points from 0.2 and 0.8 V to 50% level. • In Table 18, changed num 46 description to read, "$\overline{TA}$ assertion to rising edge ..." • In Figure 43, changed $\overline{TA}$ to reflect the rising edge of the clock.

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