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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	133MHz
Co-Processors/DSP	Communications; CPM, Security; SEC
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (1), 10/100Mbps (2)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 100°C (TA)
Security Features	Cryptography
Package / Case	256-BBGA
Supplier Device Package	256-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc875czt133

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Features

- The MPC875 has a time-slot assigner (TSA) that supports one TDM bus (TDMb)
 - Allows SCC and SMC to run in multiplexed and/or non-multiplexed operation
 - Supports T1, CEPT, PCM highway, ISDN basic rate, ISDN primary rate, user-defined
 - 1- or 8-bit resolution
 - Allows independent transmit and receive routing, frame synchronization, and clocking
 - Allows dynamic changes
 - Can be internally connected to two serial channels (one SCC and one SMC)
- PCMCIA interface
 - Master (socket) interface, release 2.1-compliant
 - Supports one independent PCMCIA socket on the MPC875/MPC870
 - Eight memory or I/O windows supported
- Debug interface
 - Eight comparators: four operate on instruction address, two operate on data address, and two
 operate on data
 - Supports conditions: = \neq < >
 - Each watchpoint can generate a break point internally
- Normal high and normal low power modes to conserve power
- 1.8-V core and 3.3-V I/O operation with 5-V TTL compatibility
- The MPC875/MPC870 comes in a 256-pin ball grid array (PBGA) package



Power Supply and Power Sequencing

7.5 Experimental Determination

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

 Ψ_{JT} = thermal characterization parameter

 T_T = thermocouple temperature on top of package

 P_D = power dissipation in package

The thermal characterization parameter is measured per the JESD51-2 specification published by JEDEC using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by the cooling effects of the thermocouple wire.

7.6 References

Semiconductor Equipment and Materials International	(415) 964-5111
805 East Middlefield Rd	
Mountain View, CA 94043	
MIL-SPEC and EIA/JESD (JEDEC) specifications	800-854-7179 or
(Available from Global Engineering Documents)	303-397-7956
JEDEC Specifications	http://www.jedec.org

- 1. C.E. Triplett and B. Joiner, "An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module," Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
- 2. B. Joiner and V. Adams, "Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling," Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

8 Power Supply and Power Sequencing

This section provides design considerations for the MPC875/MPC870 power supply. The MPC875/MPC870 has a core voltage (V_{DDL}) and PLL voltage (V_{DDSYN}), which both operate at a lower voltage than the I/O voltage (V_{DDH}). The I/O section of the MPC875/MPC870 is supplied with 3.3 V across V_{DDH} and V_{SS} (GND).

The signals PA[0:3], PA[8:11], PB15, PB[24:25], PB[28:31], PC[4:7], PC[12:13], PC15, PD[3:15], TDI, TDO, TCK, TRST, TMS, MII_TXEN, and MII_MDIO are 5 V tolerant. No input can be more than 2.5 V greater than V_{DDH}. In addition, 5-V tolerant pins cannot exceed 5.5 V, and remaining input pins cannot exceed 3.465 V. This restriction applies to power up, power down, and normal operation.

NP

One consequence of multiple power supplies is that when power is initially applied, the voltage rails ramp up at different rates. The rates depend on the nature of the power supply, the type of load on each power supply, and the manner in which different voltages are derived. The following restrictions apply:

- + V_{DDL} must not exceed V_{DDH} during power up and power down
- + V_{DDL} must not exceed 1.9 V, and V_{DDH} must not exceed 3.465 V

These cautions are necessary for the long-term reliability of the part. If they are violated, the electrostatic discharge (ESD) protection diodes are forward-biased, and excessive current can flow through these diodes. If the system power supply design does not control the voltage sequencing, the circuit shown in Figure 4 can be added to meet these requirements. The MUR420 Schottky diodes control the maximum potential difference between the external bus and core power supplies on power up, and the 1N5820 diodes regulate the maximum potential difference on power down.



Figure 4. Example Voltage Sequencing Circuit

9 Mandatory Reset Configurations

The MPC875/MPC870 requires a mandatory configuration during reset.

If hardware reset configuration word (HRCW) is enabled, the HRCW[DBGC] value needs to be set to binary X1 in the HRCW and the SIUMCR[DBGC] should be programmed with the same value in the boot code after reset. This can be done by asserting the RSTCONF during HRESET assertion.

If HRCW is disabled, the SIUMCR[DBGC] should be programmed with binary X1 in the boot code after reset by negating the $\overline{\text{RSTCONF}}$ during the $\overline{\text{HRESET}}$ assertion.

The MBMR[GPLB4DIS], PAPAR, PADIR, PBPAR, PBDIR, PCPAR, and PCDIR need to be configured with the mandatory values in Table 7 in the boot code after the reset is negated.

Register/Configuration	Field	Value (Binary)
HRCW (Hardware reset configuration word)	HRCW[DBGC]	X1
SIUMCR (SIU module configuration register)	SIUMCR[DBGC]	X1
MBMR (Machine B mode register)	MBMR[GPLB4DIS}	0
PAPAR (Port A pin assignment register)	PAPAR[5:9] PAPAR[12:13]	0

Table 7. Mandatory Reset Configuration of MPC875/MPC870



Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Unit
B42	CLKOUT rising edge to \overline{TS} valid (hold time) (MIN = 0.00 × B1 + 2.00)	2.00	—	2.00	—	2.00	_	2.00	_	ns
B43	AS negation to memory controller signals negation (MAX = TBD)	—	TBD	—	TBD	_	TBD	_	TBD	ns

¹ For part speeds above 50 MHz, use 9.80 ns for B11a.

² The timing required for BR input is relevant when the MPC875/MPC870 is selected to work with the internal bus arbiter. The timing for BG input is relevant when the MPC875/MPC870 is selected to work with the external bus arbiter.

³ For part speeds above 50 MHz, use 2 ns for B17.

⁴ The D(0:31) input timings B18 and B19 refer to the rising edge of the CLKOUT in which the TA input signal is asserted.

⁵ For part speeds above 50 MHz, use 2 ns for B19.

⁶ The D(0:31) input timings B20 and B21 refer to the falling edge of the CLKOUT. This timing is valid only for read accesses controlled by chip-selects under control of the user-programmable machine (UPM) in the memory controller, for data beats where DLT3 = 1 in the RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

⁷ This formula applies to bus operation up to 50 MHz.

⁸ The timing B30 refers to \overline{CS} when ACS = 00 and to $\overline{WE}(0:3)$ when CSNT = 0.

⁹ The signal UPWAIT is considered asynchronous to the CLKOUT and synchronized internally. The timings specified in B37 and B38 are specified to enable the freeze of the UPM output signals as described in Figure 20.

¹⁰ The AS signal is considered asynchronous to the CLKOUT. The timing B39 is specified in order to allow the behavior specified in Figure 23.



Figure 7 provides the timing for the synchronous output signals.



Figure 7. Synchronous Output Signals Timing

Figure 8 provides the timing for the synchronous active pull-up and open-drain output signals.



Figure 8. Synchronous Active Pull-Up Resistor and Open-Drain Outputs Signals Timing





Figure 15. External Bus Read Timing (GPCM Controlled—TRLX = 1, ACS = 10, ACS = 11)



Figure 16 through Figure 18 provide the timing for the external bus write controlled by various GPCM factors.



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Figure 16. External Bus Write Timing (GPCM Controlled—TRLX = 0, CSNT = 0)
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Figure 17. External Bus Write Timing (GPCM Controlled—TRLX = 0, CSNT = 1)



Table 11 provides the interrupt timing for the MPC875/MPC870.

Num	Characteristic ¹	All Freq	Unit	
	Gharacteristic	Min	Мах	0.111
139	IRQx valid to CLKOUT rising edge (setup time)	6.00		ns
I40	IRQx hold time after CLKOUT	2.00		ns
141	IRQx pulse width low	3.00		ns
l42	IRQx pulse width high	3.00		ns
143	IRQx edge-to-edge time	$4 \times T_{CLOCKOUT}$		_

¹ The I39 and I40 timings describe the testing conditions under which the IRQ lines are tested when being defined as level sensitive. The IRQ lines are synchronized internally and do not have to be asserted or negated with reference to the CLKOUT. The I41, I42, and I43 timings are specified to allow correct functioning of the IRQ lines detection circuitry and have no direct relation with the total system interrupt latency that the MPC875/MPC870 is able to support.

Figure 25 provides the interrupt detection timing for the external level-sensitive lines.



Figure 25. Interrupt Detection Timing for External Level Sensitive Lines

Figure 26 provides the interrupt detection timing for the external edge-sensitive lines.



Figure 26. Interrupt Detection Timing for External Edge-Sensitive Lines



Table 12 shows the PCMCIA timing for the MPC875/MPC870.

Table 12. PCMCIA Timing

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
Nulli		Min	Max	Min	Max	Min	Max	Min	Max	Omt
P44	A(0:31), $\overline{\text{REG}}$ valid to PCMCIA strobe asserted ¹ (MIN = 0.75 × B1 - 2.00)	20.70	_	16.70	_	9.40	—	7.40	—	ns
P45	A(0:31), $\overline{\text{REG}}$ valid to ALE negation ¹ (MIN = 1.00 × B1 – 2.00)	28.30	_	23.00	_	13.20	_	10.50	_	ns
P46	CLKOUT to $\overline{\text{REG}}$ valid (MAX = 0.25 × B1 + 8.00)	7.60	15.60	6.30	14.30	3.80	11.80	3.13	11.13	ns
P47	CLKOUT to $\overline{\text{REG}}$ invalid (MIN = 0.25 × B1 + 1.00)	8.60	_	7.30	_	4.80	_	4.125	_	ns
P48	CLKOUT to $\overline{CE1}$, $\overline{CE2}$ asserted (MAX = 0.25 × B1 + 8.00)	7.60	15.60	6.30	14.30	3.80	11.80	3.13	11.13	ns
P49	CLKOUT to $\overline{CE1}$, $\overline{CE2}$ negated (MAX = 0.25 × B1 + 8.00)	7.60	15.60	6.30	14.30	3.80	11.80	3.13	11.13	ns
P50	CLKOUT to \overrightarrow{PCOE} , \overrightarrow{IORD} , \overrightarrow{PCWE} , \overrightarrow{IOWR} assert time (MAX = 0.00 × B1 + 11.00)	—	11.00	—	11.00	_	11.00	_	11.00	ns
P51	CLKOUT to \overrightarrow{PCOE} , \overrightarrow{IORD} , \overrightarrow{PCWE} , \overrightarrow{IOWR} negate time (MAX = 0.00 × B1 + 11.00)	2.00	11.00	2.00	11.00	2.00	11.00	2.00	11.00	ns
P52	CLKOUT to ALE assert time $(MAX = 0.25 \times B1 + 6.30)$	7.60	13.80	6.30	12.50	3.80	10.00	3.13	9.40	ns
P53	CLKOUT to ALE negate time $(MAX = 0.25 \times B1 + 8.00)$	_	15.60	—	14.30	_	11.80	_	11.13	ns
P54	PCWE, $\overline{\text{IOWR}}$ negated to D(0:31) invalid ¹ (MIN = 0.25 × B1 - 2.00)	5.60	_	4.30	—	1.80	—	1.125	—	ns
P55	$\overline{\text{WAITA}}$ and $\overline{\text{WAITB}}$ valid to CLKOUT rising edge ¹ (MIN = 0.00 × B1 + 8.00)	8.00	_	8.00	_	8.00	—	8.00	—	ns
P56	CLKOUT rising edge to \overline{WAITA} and \overline{WAITB} invalid ¹ (MIN = 0.00 × B1 + 2.00)	2.00	_	2.00	_	2.00	_	2.00	_	ns

¹ PSST = 1. Otherwise add PSST times cycle time.

PSHT = 0. Otherwise add PSHT times cycle time.

These synchronous timings define when the WAITA signals are detected in order to freeze (or relieve) the PCMCIA current cycle. The WAITA assertion will be effective only if it is detected 2 cycles before the PSL timer expiration. See Chapter 16, "PCMCIA Interface," in the *MPC885 PowerQUICC™ Family Reference Manual*.



12 IEEE 1149.1 Electrical Specifications

Table 16 provides the JTAG timings for the MPC875/MPC870 shown in Figure 37 through Figure 40.

Table 16. JTAG Timing

Num	Characteristic	All Freq	l lmit	
Num	Characteristic		Мах	Unit
J82	TCK cycle time	100.00	—	ns
J83	TCK clock pulse width measured at 1.5 V	40.00	—	ns
J84	TCK rise and fall times	0.00	10.00	ns
J85	TMS, TDI data setup time	5.00	—	ns
J86	TMS, TDI data hold time	25.00	—	ns
J87	TCK low to TDO data valid	_	27.00	ns
J88	TCK low to TDO data invalid	0.00	—	ns
J89	TCK low to TDO high impedance	_	20.00	ns
J90	TRST assert time	100.00	_	ns
J91	TRST setup time to TCK low	40.00	—	ns
J92	TCK falling edge to output valid	_	50.00	ns
J93	TCK falling edge to output valid out of high impedance	_	50.00	ns
J94	TCK falling edge to output high impedance	_	50.00	ns
J95	Boundary scan input valid to TCK rising edge	50.00	—	ns
J96	TCK rising edge to boundary scan input invalid	50.00	_	ns



Figure 37. JTAG Test Clock Input Timing





Figure 47. CPM General-Purpose Timers Timing Diagram

13.5 Serial Interface AC Electrical Specifications

Table 21 provides the serial interface (SI) timings as shown in Figure 48 through Figure 52.

Num	Characteristic	All Fre	Unit	
Num	Characteristic	Min	Мах	Unit
70	L1RCLKB, L1TCLKB frequency (DSC = 0) ^{1, 2}	—	SYNCCLK/2.5	MHz
71	L1RCLKB, L1TCLKB width low $(DSC = 0)^2$	P + 10	_	ns
71a	L1RCLKB, L1TCLKB width high $(DSC = 0)^3$	P + 10	_	ns
72	L1TXDB, L1ST1 and L1ST2, L1RQ, L1CLKO rise/fall time	—	15.00	ns
73	L1RSYNCB, L1TSYNCB valid to L1CLKB edge (SYNC setup time)	20.00	—	ns
74	L1CLKB edge to L1RSYNCB, L1TSYNCB, invalid (SYNC hold time)	35.00	—	ns
75	L1RSYNCB, L1TSYNCB rise/fall time	—	15.00	ns
76	L1RXDB valid to L1CLKB edge (L1RXDB setup time)	17.00	—	ns
77	L1CLKB edge to L1RXDB invalid (L1RXDB hold time)	13.00	—	ns
78	L1CLKB edge to L1ST1 and L1ST2 valid ⁴	10.00	45.00	ns
78A	L1SYNCB valid to L1ST1 and L1ST2 valid	10.00	45.00	ns
79	L1CLKB edge to L1ST1 and L1ST2 invalid	10.00	45.00	ns
80	L1CLKB edge to L1TXDB valid	10.00	55.00	ns
80A	L1TSYNCB valid to L1TXDB valid ⁴	10.00	55.00	ns
81	L1CLKB edge to L1TXDB high impedance	0.00	42.00	ns
82	L1RCLKB, L1TCLKB frequency (DSC = 1)	_	16.00 or SYNCCLK/2	MHz
83	L1RCLKB, L1TCLKB width low (DSC = 1)	P + 10	_	ns

Table 21. SI Timing

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Figure 55. HDLC Bus Timing Diagram

13.7 Ethernet Electrical Specifications

Table 24 provides the Ethernet timings as shown in Figure 56 through Figure 58.

Table 24. Ethernet Timing

Num	Characteristic	All Freq	uencies	Unit
Nulli		Min	Мах	Unit
120	CLSN width high	40	_	ns
121	RCLK3 rise/fall time	—	15	ns
122	RCLK3 width low	40	_	ns
123	RCLK3 clock period ¹	80	120	ns
124	RXD3 setup time	20	_	ns
125	RXD3 hold time	5	_	ns
126	RENA active delay (from RCLK3 rising edge of the last data bit)	10	_	ns
127	RENA width low	100	_	ns
128	TCLK3 rise/fall time	—	15	ns
129	TCLK3 width low	40	_	ns
130	TCLK3 clock period ¹	99	101	ns
131	TXD3 active delay (from TCLK3 rising edge)	_	50	ns
132	TXD3 inactive delay (from TCLK3 rising edge)	6.5	50	ns
133	TENA active delay (from TCLK3 rising edge)	10	50	ns
134	TENA inactive delay (from TCLK3 rising edge)	10	50	ns

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2. If RENA is negated before TENA or RENA is not asserted at all during transmit, then the CSL bit is set in the buffer descriptor at the end of the frame transmission.

Figure 58. Ethernet Transmit Timing Diagram

13.8 SMC Transparent AC Electrical Specifications

Table 25 provides the SMC transparent timings as shown in Figure 59.

Num	Characteristic	All Freq	Unit	
	Characteristic		Мах	Onit
150	SMCLK clock period ¹	100	—	ns
151	SMCLK width low	50	—	ns
151A	SMCLK width high	50	—	ns
152	SMCLK rise/fall time	_	15	ns
153	SMTXD active delay (from SMCLK falling edge)	10	50	ns
154	SMRXD/SMSYNC setup time	20	—	ns
155	RXD1/SMSYNC hold time 5			ns

¹ SYNCCLK must be at least twice as fast as SMCLK.



FEC Electrical Characteristics

Figure 65 shows MII receive signal timing.



Figure 65. MII Receive Signal Timing Diagram

15.2 MII and Reduced MII Transmit Signal Timing

The transmitter functions correctly up to a MII_TX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_TX_CLK frequency -1%.

Table 32 provides information on the MII transmit signal timing.

Table 3	2. MII	Transmit	Signal	Timing
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Num	Characteristic	Min	Max	Unit
M5	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER invalid	5	_	ns
M6	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER valid	—	25	ns
M7	MII_TX_CLK pulse width high	35%	65%	MII_TX_CLK period
M8	MII_TX_CLK pulse width low	35%	65%	MII_TX_CLK period
M20_RMII	RMII_TXD[1:0], RMII_TX_EN to RMII_REFCLK setup	4	_	ns
M21_RMII	RMII_TXD[1:0], RMII_TX_EN data hold from RMII_REFCLK rising edge	2	—	ns



Figure 66 shows the MII transmit signal timing diagram.



Figure 66. MII Transmit Signal Timing Diagram

15.3 MII Async Inputs Signal Timing (MII_CRS, MII_COL)

Table 33 provides information on the MII async inputs signal timing.

Table 33. MII Async Inputs Signal Timing

Num	Characteristic	Min	Max	Unit
M9	MII_CRS, MII_COL minimum pulse width	1.5		MII_TX_CLK period

Figure 67 shows the MII asynchronous inputs signal timing diagram.



Figure 67. MII Async Inputs Timing Diagram

15.4 MII Serial Management Channel Timing (MII_MDIO, MII_MDC)

Table 34 provides information on the MII serial management channel signal timing. The FEC functions correctly with a maximum MDC frequency in excess of 2.5 MHz.

Table 34.	MII	Serial	Management	Channel	Timing
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Num	Characteristic	Min	Мах	Unit
M10	MII_MDC falling edge to MII_MDIO output invalid (minimum propagation delay)	0	_	ns
M11	MII_MDC falling edge to MII_MDIO output valid (max prop delay)		25	ns
M12	MII_MDIO (input) to MII_MDC rising edge setup	10	—	ns
M13	MII_MDIO (input) to MII_MDC rising edge hold	0	—	ns
M14	MII_MDC pulse width high	40%	60%	MII_MDC period
M15	MII_MDC pulse width low	40%	60%	MII_MDC period

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FEC Electrical Characteristics

Figure 68 shows the MII serial management channel timing diagram.



Figure 68. MII Serial Management Channel Timing Diagram

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16.1 Pin Assignments

Figure 69 shows the JEDEC pinout of the PBGA package as viewed from the top surface. For additional information, see the *MPC885 PowerQUICC Family User's Manual*.

NOTE

The pin numbering starts with B2 in order to conform to the JEDEC standard for 23-mm body size using a 16×16 array.

2 7 8 9 10 11 12 13 14 3 4 5 6 15 16 17 O O O O EXTCLK MODCK1 \bigcup_{ALEA} \bigcirc CS3 O N/C в Ο O OP0 $O_{\overline{CS5}}$ MODCK2 $\bigcirc_{\overline{BB}}$ $\bigcup_{\overline{TS}}$ \bigcup_{TA} O_{CS2} С \bigcirc \cap О \bigcirc \bigcirc \bigcirc \bigcirc \bigcirc \bigcirc \bigcirc \bigcirc \bigcirc CE1A RSTCONF SRESET BADDR29 OP1 ALEB IRQ2 BDIP GPLAB3 GPLA0 IPA7 D \bigcirc \bigcirc Ο IPA2 WAITA PORESET XTAL EXTAL BADDR30 IPB1 BG GPLA4 GPLA5 $\overline{\mathsf{WR}}$ CE2A CS7 WE2 WE1 IPA4 Е Ο \bigcirc \bigcirc \bigcirc \bigcirc \bigcirc \bigcirc Ο \bigcirc \bigcirc О Ο Ο Ο Ο Ο HRESET BADDR28 IRQ4 CS1 GPLB4 CS4 GPLAB2 BSA1 BSA2 **IRQ3 WEO** D31 IPA5 IPA3 VSSSYN VDDSYN F Ο \bigcirc \bigcirc \bigcirc O_{CS6} Ο Ο O \bigcirc O Ο \bigcirc \bigcirc \odot Ο Ο BSAO BSA3 D30 IPA6 IPA1 VSSSYN VDDL VDDL OE TSIZ0 A31 D29 G \bigcirc Ο Ο \bigcirc Ο \bigcirc O VDDH \bigcirc \bigcirc O VDDH \bigcirc Ο \bigcirc \bigcirc Ο Ο D28 CLKOUT IPA0 WE3 TSI71 A22 D7 D26 A26 A18 н Ο Ο Ο Ο \bigcirc \bigcirc \bigcirc \bigcirc \bigcirc \bigcirc Ο \bigcirc Ο \bigcirc Ο Ο D22 D6 D24 D25 VDDL VDDH GND VDDH VDDL A28 A30 A25 A24 O D20 O D21 () A20 O A29 J Ο \bigcirc \bigcirc Ο Ο \bigcirc \bigcirc O A23 O A21 Ο Ο \bigcirc D19 D18 GND Κ Ο Ο Ο \bigcirc \bigcirc \bigcirc \bigcirc \bigcirc Ο Ο Ο 0 Ο Ο \bigcirc \bigcirc D15 D16 D14 VDDL GND VDDL D5 A14 A19 A27 A17 O D2 () A12 L \bigcirc Ο 0 \bigcirc \bigcirc \bigcirc \bigcirc \bigcirc \bigcirc \bigcirc \bigcirc Ο D27 DO A15 A10 A16 D3 () A8 Μ \bigcirc Ο Ο Ο 0 \bigcirc \bigcirc \bigcirc \bigcirc 0 \bigcirc \bigcirc Ο A11 **IRQ0** MII_MDIO A2 A13 D11 D9 D12 PE18 0 0 \bigcirc 0 \bigcirc \bigcirc Ο \bigcirc \bigcirc 0 Ν \bigcirc 0 Ο \bigcirc Ο \bigcirc D13 IRQ7 PA2 VDDL VDDL PB26 PB27 A1 A6 A7 D10 D1 A9 \bigcirc \bigcirc \bigcirc Ο \bigcirc \bigcirc \bigcirc \bigcirc Ο \bigcirc Р Ο \bigcirc Ο \bigcirc \bigcirc PE14 PE31 D23 D17 PE22 PA0 PA4 PC6 PA6 PC11 TDO PA15 A3 Α5 R О O Ο Ο \bigcirc \bigcirc \bigcirc \bigcirc \bigcirc \bigcirc \bigcirc \bigcirc O PB28 O PC15 \bigcirc_{A0} \bigcirc PE19 PE28 PE30 PA11 MII_COL PA7 PA10 тск PB29 PE25 PA3 D4 D8 \bigcirc Ο \bigcirc \bigcirc Ο \bigcirc \bigcirc \bigcirc Ο \bigcirc \bigcirc \bigcirc \bigcirc т \bigcirc Ο \bigcirc PD8 PB31 PE27 PE17 PE21 PC7 PB19 PC12 N/C PB30 PE26 PA1 PE15 PB24 TDI TMS U O PE20 O PE23 MII-TX-EN PE16 O PE29 O PE24 O PC13 O MII-CRS O PC10 O PB23 O PB25 O PA14 O N/C

NOTE: This is the top view of the device.

Figure 69. Pinout of the PBGA Package—JEDEC Standard



Table 36 contains a list of the MPC875/MPC870 input and output signals and shows multiplexing and pin assignments.

Name	Pin Number	Туре
A[0:31]	R16, N14, M14, P15, P17, P16, N15, N16, M15, N17, L14, M16, L15, M17, K14, L16, L17, K17, G17, K15, J16, J15, G16, J14, H17, H16, G15, K16, H14, J17, H15, F17	Bidirectional Three-state (3.3 V only)
TSIZ0, REG	F16	Bidirectional Three-state (3.3 V only)
TSIZ1	G14	Bidirectional Three-state (3.3 V only)
RD/WR	D13	Bidirectional Three-state (3.3 V only)
BURST	B9	Bidirectional Three-state (3.3 V only)
BDIP, GPL_B5	C13	Output
TS	C11	Bidirectional Active pull-up (3.3 V only)
TA	C12	Bidirectional Active pull-up (3.3 V only)
TEA	B12	Open-drain
BI	B13	Bidirectional Active pull-up (3.3 V only)
IRQ2, RSV	C9	Bidirectional Three-state (3.3 V only)
ĪRQ4, KR, RETRY, SPKROUT	E9	Bidirectional Three-state (3.3 V only)
D[0:31]	L5, N3, L3, L2, R2, K2, H3, G2, R3, M3, N2, M2, M4, N4, K5, K3, K4, P3, J2, J3, J4, J5, H2, P2, H4, H5, G5, L4, G3, F2, F3, E2	Bidirectional Three-state (3.3 V only)
CR, IRQ3	E10	Input
FRZ, IRQ6	B10	Bidirectional Three-state (3.3 V only)
BR	B11	Bidirectional (3.3 V only)
BG	D10	Bidirectional (3.3 V only)
BB	C10	Bidirectional Active pull-up (3.3 V only)
IRQ0	M6	Input (3.3 V only)
IRQ1	P5	Input (3.3 V only)
IRQ7	N5	Input (3.3 V only)
CS[0:5]	B14, E11, C14, B15, E13, B16	Output

Table 36. Pin Assignments—JEDEC Standard



Document Revision History

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Table 37 lists significant changes between revisions of this hardware specification.

Table 37. Document Revision History

Revision Number	Date	Changes
0	2/2003	Initial release.
0.1	3/2003	Took out the time-slot assigner and changed the SCC for SCC3 to SCC4.
0.2	5/2003	Changed the package drawing, removed all references to Data Parity. Changed the SPI Master Timing Specs. 162 and 164. Added the RMII and USB timing. Added the 80-MHz timing.
0.3	5/2003	Made sure the pin types were correct. Changed the Features list to agree with the MPC885.
0.4	5/2003	Corrected the signals that had overlines on them. Made corrections on two pins that were typos.
0.5	5/2003	Changed the pin descriptions for PD8 and PD9.
0.6	5/2003	Changed a few typos. Put back the I^2C . Put in the new reset configuration, corrected the USB timing.
0.7	6/2003	Changed the pin descriptions per the June 22 spec, removed Utopia from the pin descriptions, changed PADIR, PBDIR, PCDIR and PDDIR to be 0 in the Mandatory Reset Config.
0.8	8/2003	Added the reference to USB 2.0 to the Features list and removed 1.1 from USB on the block diagrams.
0.9	8/2003	Changed the USB description to full-/low-speed compatible.
1.0	9/2003	Added the DSP information in the Features list. Put a new sentence under Mechanical Dimensions. Fixed table formatting. Nontechnical edits. Released to the external web.
1.1	10/2003	Added TDMb to the MPC875 Features list, the MPC875 Block Diagram, added 13.5 Serial Interface AC Electrical Specifications, and removed TDMa from the pin descriptions.
2.0	12/2003	Changed DBGC in the Mandatory Reset Configuration to X1. Changed the maximum operating frequency to 133 MHz. Put the timing in the 80 MHz column. Put in the orderable part numbers. Rounded the timings to hundredths in the 80 MHz column. Put the pin numbers in footnotes by the maximum currents in Table 6. Changed 22 and 41 in the Timing. Put TBD in the Thermal table.

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