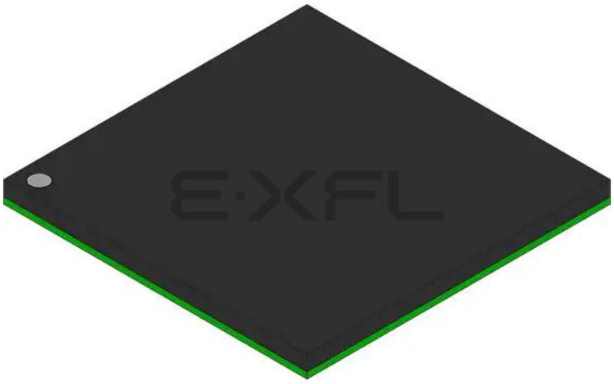
Freescale Semiconductor - MPC875CZT66 Datasheet



Details	
Product Status	Active
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	66MHz
Co-Processors/DSP	Communications; CPM, Security; SEC
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (1), 10/100Mbps (2)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 100°C (TA)
Security Features	Cryptography
Package / Case	256-BBGA
Supplier Device Package	256-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc875czt66

3 Maximum Tolerated Ratings

This section provides the maximum tolerated voltage and temperature ranges for the MPC875/MPC870. Table 2 displays the maximum tolerated ratings and Table 3 displays the operating temperatures.

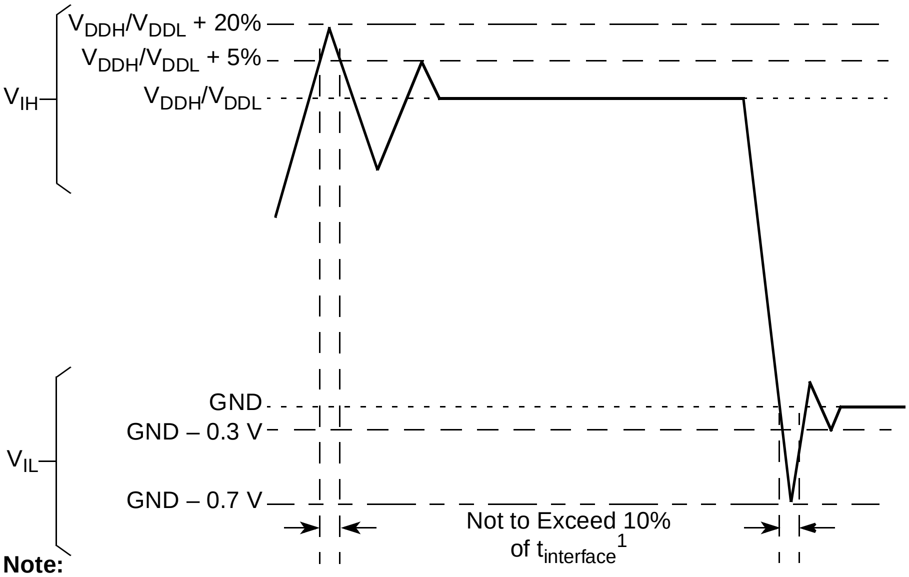
Table 2. Maximum Tolerated Ratings

Rating	Symbol	Value	Unit
Supply voltage[1]	V_{DDL} (core voltage)	–0.3 to 3.4	V
	V_{DDH} (I/O voltage)	–0.3 to 4	V
	V_{DDSYN}	–0.3 to 3.4	V
	Difference between V_{DDL} and V_{DDSYN}	<100	mV
Input voltage[2]	V_{in}	GND – 0.3 to V_{DDH}	V
Storage temperature range	T_{stg}	–55 to +150	°C

[1] The power supply of the device must start its ramp from 0.0 V.

[2] Functional operating conditions are provided with the DC electrical specifications in Table 6. Absolute maximum ratings are stress ratings only; functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.
Caution: All inputs that tolerate 5 V cannot be more than 2.5 V greater than V_{DDH}. This restriction applies to power up and normal operation (that is, if the MPC875/MPC870 is unpowered, a voltage greater than 2.5 V must not be applied to its inputs).

Figure 3 shows the undershoot and overshoot voltages at the interfaces of the MPC875/MPC870.



Note:
1. $t_{interface}$ refers to the clock period associated with the bus clock interface.

Figure 3. Undershoot/Overshoot Voltage for V_{DDH} and V_{DDL}

Table 7. Mandatory Reset Configuration of MPC875/MPC870 (continued)

Register/Configuration	Field	Value (Binary)
PADIR (Port A data direction register)	PADIR[5:9] PADIR[12:13]	0
PBPAR (Port B pin assignment register)	PBPAR[14:18] PBPAR[20:22]	0
PBDIR (Port B data direction register)	PBDIR[14:8] PBDIR[20:22]	0
PCPAR (Port C pin assignment register)	PCPAR[4:5] PCPAR[8:9] PCPAR[14]	0
PCDIR (Port C data direction register)	PCDIR[4:5] PCDIR[8:9] PCDIR[14]	0
PDPAR (Port D pin assignment register)	PDPAR[3:7] PDPAR[9:5]	0
PDDIR (Port D data direction register)	PDDIR[3:7] PDDIR[9:15]	0

10 Layout Practices

Each V_{DD} pin on the MPC875/MPC870 should be provided with a low-impedance path to the board's supply. Each GND pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The V_{DD} power supply should be bypassed to ground using at least four 0.1-µF bypass capacitors located as close as possible to the four sides of the package. Each board designed should be characterized and additional appropriate decoupling capacitors should be used if required. The capacitor leads and associated printed-circuit traces connecting to chip V_{DD} and GND should be kept to less than half an inch per capacitor lead. At a minimum, a four-layer board employing two inner layers as V_{DD} and GND planes should be used.

All output pins on the MPC875/MPC870 have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses. Maximum PC trace lengths of 6 inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the V_{DD} and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins. For more information, refer to Section 14.4.3, "Clock Synthesizer Power (V_{DDSYN}, V_{SSSYN}, V_{SSSYN1})," in the *MPC885 PowerQUICC™ Family Reference Manual*.

Table 10. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B2	CLKOUT pulse width low (MIN = 0.4 × B1, MAX = 0.6 × B1)	12.1	18.2	10.0	15.0	6.1	9.1	5.0	7.5	ns
B3	CLKOUT pulse width high (MIN = 0.4 × B1, MAX = 0.6 × B1)	12.1	18.2	10.0	15.0	6.1	9.1	5.0	7.5	ns
B4	CLKOUT rise time	—	4.00	—	4.00	—	4.00	—	4.00	ns
B5	CLKOUT fall time	—	4.00	—	4.00	—	4.00	—	4.00	ns
B7	CLKOUT to A(0:31), BADDR(28:30), RD/$\overline{WR}$, $\overline{BURST}$, D(0:31) output hold (MIN = 0.25 × B1)	7.60	—	6.30	—	3.80	—	3.13	—	ns
B7a	CLKOUT to TSIZ(0:1), $\overline{REG}$, $\overline{RSV}$, $\overline{BDIP}$, PTR output hold (MIN = 0.25 × B1)	7.60	—	6.30	—	3.80	—	3.13	—	ns
B7b	CLKOUT to $\overline{BR}$, $\overline{BG}$, $\overline{FRZ}$, VFLS(0:1), VF(0:2) IWP(0:2), LWP(0:1), $\overline{STS}$ output hold (MIN = 0.25 × B1)	7.60	—	6.30	—	3.80	—	3.13	—	ns
B8	CLKOUT to A(0:31), BADDR(28:30), RD/$\overline{WR}$, $\overline{BURST}$, D(0:31) valid (MAX = 0.25 × B1 + 6.3)	—	13.80	—	12.50	—	10.00	—	9.43	ns
B8a	CLKOUT to TSIZ(0:1), $\overline{REG}$, $\overline{RSV}$, $\overline{BDIP}$, PTR valid (MAX = 0.25 × B1 + 6.3)	—	13.80	—	12.50	—	10.00	—	9.43	ns
B8b	CLKOUT to $\overline{BR}$, $\overline{BG}$, VFLS(0:1), VF(0:2), IWP(0:2), FRZ, LWP(0:1), $\overline{STS}$ valid [2] (MAX = 0.25 × B1 + 6.3)	—	13.80	—	12.50	—	10.00	—	9.43	ns
B9	CLKOUT to A(0:31), BADDR(28:30), RD/$\overline{WR}$, $\overline{BURST}$, D(0:31), TSIZ(0:1), $\overline{REG}$, $\overline{RSV}$, PTR High-Z (MAX = 0.25 × B1 + 6.3)	7.60	13.80	6.30	12.50	3.80	10.00	3.13	9.43	ns
B11	CLKOUT to $\overline{TS}$, $\overline{BB}$ assertion (MAX = 0.25 × B1 + 6.0)	7.60	13.60	6.30	12.30	3.80	9.80	3.13	9.13	ns
B11a	CLKOUT to $\overline{TA}$, $\overline{BI}$ assertion (when driven by the memory controller or PCMCIA interface) (MAX = 0.00 × B1 + 9.30[1])	2.50	9.30	2.50	9.30	2.50	9.80	2.5	9.3	ns
B12	CLKOUT to $\overline{TS}$, $\overline{BB}$ negation (MAX = 0.25 × B1 + 4.8)	7.60	12.30	6.30	11.00	3.80	8.50	3.13	7.92	ns
B12a	CLKOUT to $\overline{TA}$, $\overline{BI}$ negation (when driven by the memory controller or PCMCIA interface) (MAX = 0.00 × B1 + 9.00)	2.50	9.00	2.50	9.00	2.50	9.00	2.5	9.00	ns
B13	CLKOUT to $\overline{TS}$, $\overline{BB}$ High-Z (MIN = 0.25 × B1)	7.60	21.60	6.30	20.30	3.80	14.00	3.13	12.93	ns
B13a	CLKOUT to $\overline{TA}$, $\overline{BI}$ High-Z (when driven by the memory controller or PCMCIA interface) (MIN = 0.00 × B1 + 2.5)	2.50	15.00	2.50	15.00	2.50	15.00	2.5	15.00	ns
B14	CLKOUT to $\overline{TEA}$ assertion (MAX = 0.00 × B1 + 9.00)	2.50	9.00	2.50	9.00	2.50	9.00	2.50	9.00	ns

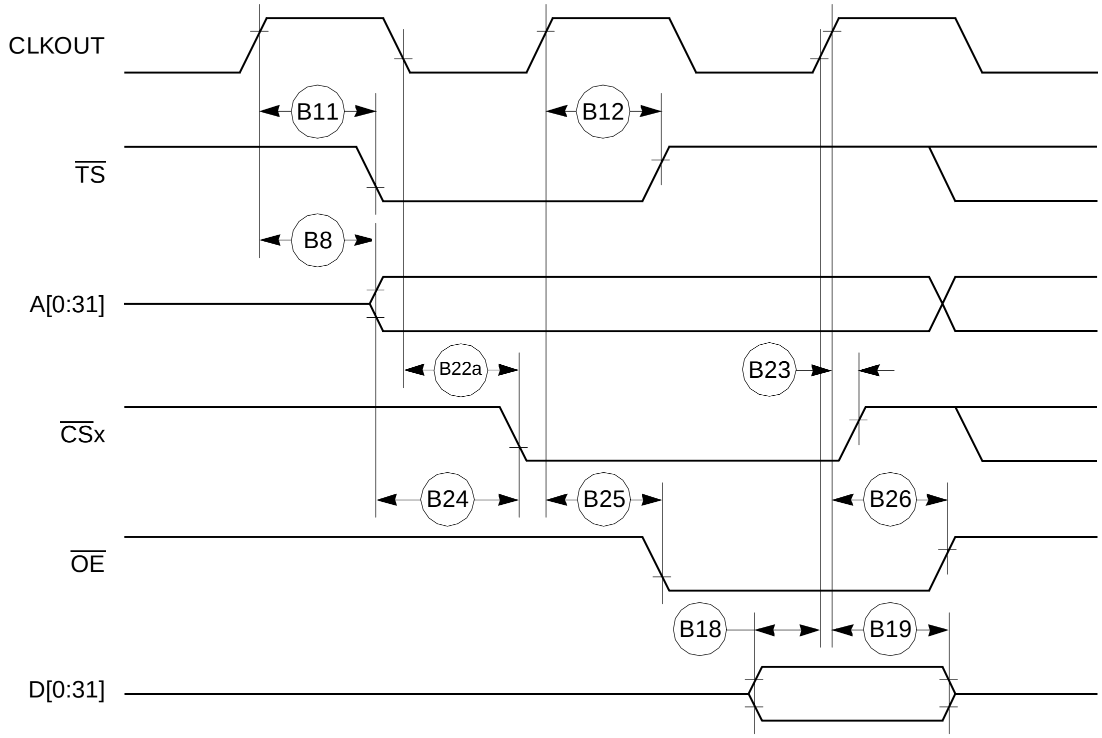


Figure 13. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 10)

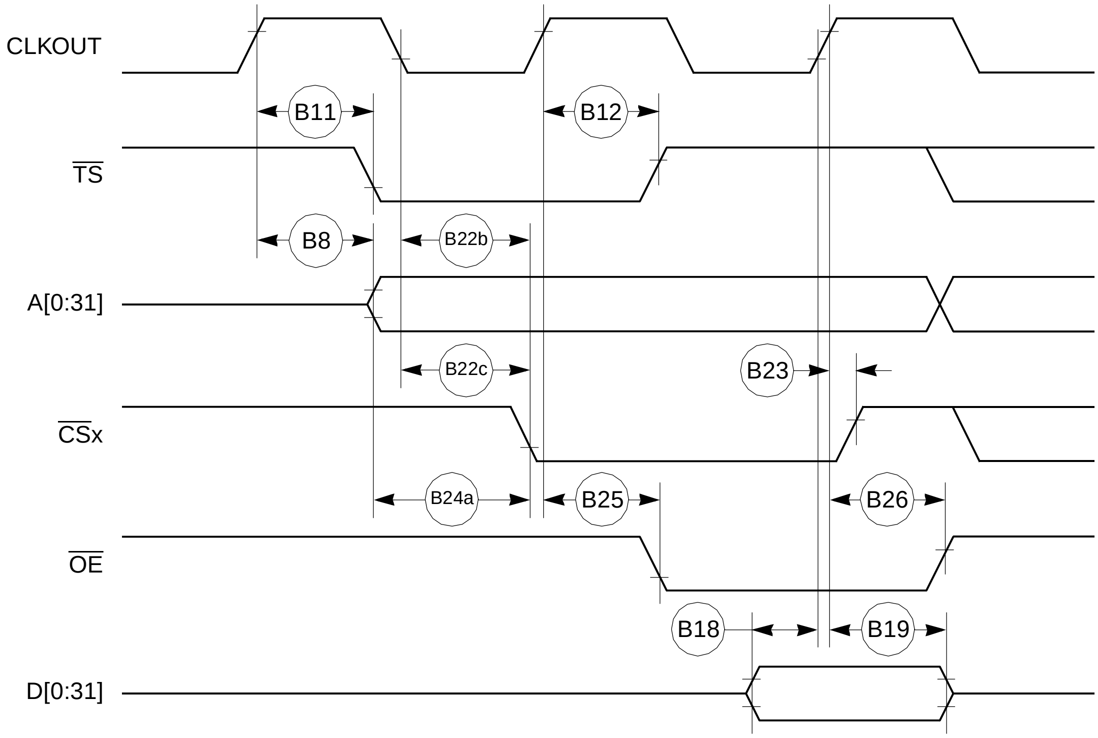


Figure 14. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 11)

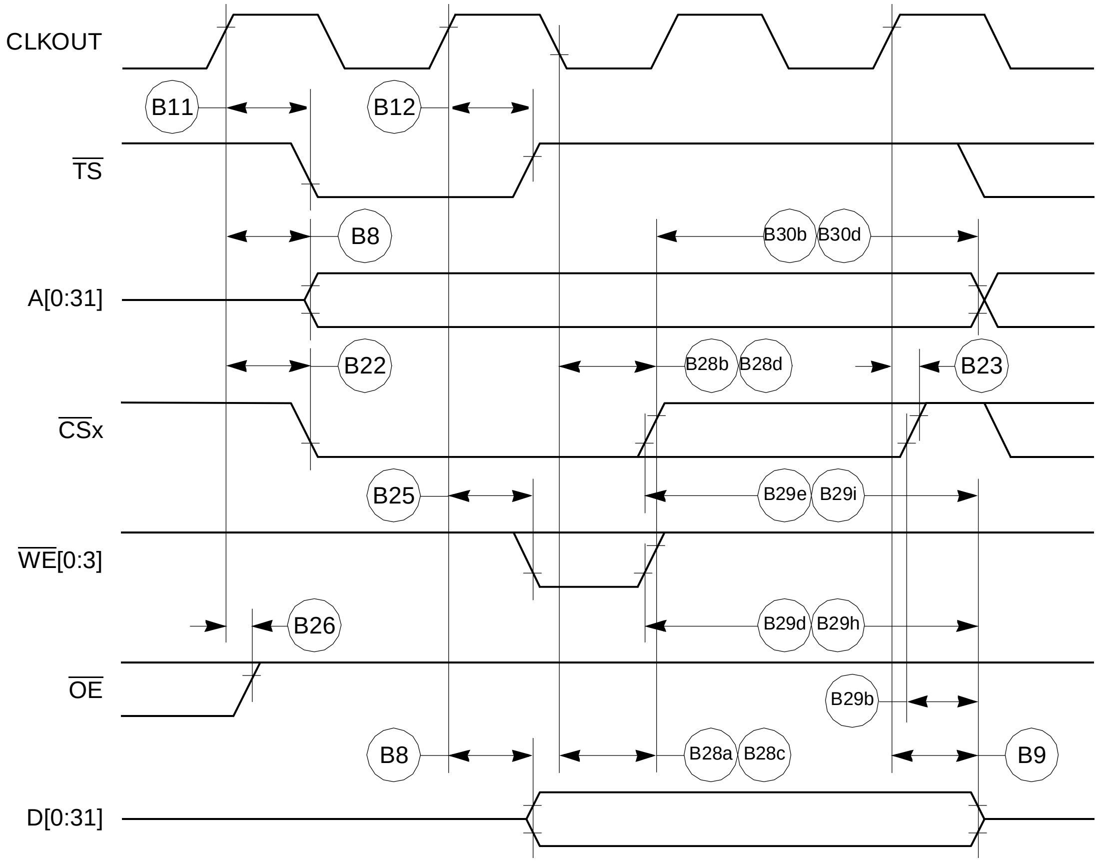


Figure 18. External Bus Write Timing (GPCM Controlled—TRLX = 1, CSNT = 1)

Table 12 shows the PCMCIA timing for the MPC875/MPC870.

Table 12. PCMCIA Timing

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
P44	A(0:31), $\overline{\text{REG}}$ valid to PCMCIA strobe asserted[1] (MIN = 0.75 × B1 – 2.00)	20.70	—	16.70	—	9.40	—	7.40	—	ns
P45	A(0:31), $\overline{\text{REG}}$ valid to ALE negation[1] (MIN = 1.00 × B1 – 2.00)	28.30	—	23.00	—	13.20	—	10.50	—	ns
P46	CLKOUT to $\overline{\text{REG}}$ valid (MAX = 0.25 × B1 + 8.00)	7.60	15.60	6.30	14.30	3.80	11.80	3.13	11.13	ns
P47	CLKOUT to $\overline{\text{REG}}$ invalid (MIN = 0.25 × B1 + 1.00)	8.60	—	7.30	—	4.80	—	4.125	—	ns
P48	CLKOUT to $\overline{\text{CE1}}$, $\overline{\text{CE2}}$ asserted (MAX = 0.25 × B1 + 8.00)	7.60	15.60	6.30	14.30	3.80	11.80	3.13	11.13	ns
P49	CLKOUT to $\overline{\text{CE1}}$, $\overline{\text{CE2}}$ negated (MAX = 0.25 × B1 + 8.00)	7.60	15.60	6.30	14.30	3.80	11.80	3.13	11.13	ns
P50	CLKOUT to $\overline{\text{PCOE}}$, $\overline{\text{IORD}}$, $\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ assert time (MAX = 0.00 × B1 + 11.00)	—	11.00	—	11.00	—	11.00	—	11.00	ns
P51	CLKOUT to $\overline{\text{PCOE}}$, $\overline{\text{IORD}}$, $\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ negate time (MAX = 0.00 × B1 + 11.00)	2.00	11.00	2.00	11.00	2.00	11.00	2.00	11.00	ns
P52	CLKOUT to ALE assert time (MAX = 0.25 × B1 + 6.30)	7.60	13.80	6.30	12.50	3.80	10.00	3.13	9.40	ns
P53	CLKOUT to ALE negate time (MAX = 0.25 × B1 + 8.00)	—	15.60	—	14.30	—	11.80	—	11.13	ns
P54	$\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ negated to D(0:31) invalid[1] (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	1.80	—	1.125	—	ns
P55	$\overline{\text{WAITA}}$ and $\overline{\text{WAITB}}$ valid to CLKOUT rising edge[1] (MIN = 0.00 × B1 + 8.00)	8.00	—	8.00	—	8.00	—	8.00	—	ns
P56	CLKOUT rising edge to $\overline{\text{WAITA}}$ and $\overline{\text{WAITB}}$ invalid[1] (MIN = 0.00 × B1 + 2.00)	2.00	—	2.00	—	2.00	—	2.00	—	ns

[1] PSST = 1. Otherwise add PSST times cycle time.
PSHT = 0. Otherwise add PSHT times cycle time.
These synchronous timings define when the $\overline{\text{WAITA}}$ signals are detected in order to freeze (or relieve) the PCMCIA current cycle. The $\overline{\text{WAITA}}$ assertion will be effective only if it is detected 2 cycles before the PSL timer expiration. See Chapter 16, “PCMCIA Interface,” in the *MPC885 PowerQUICC™ Family Reference Manual*.

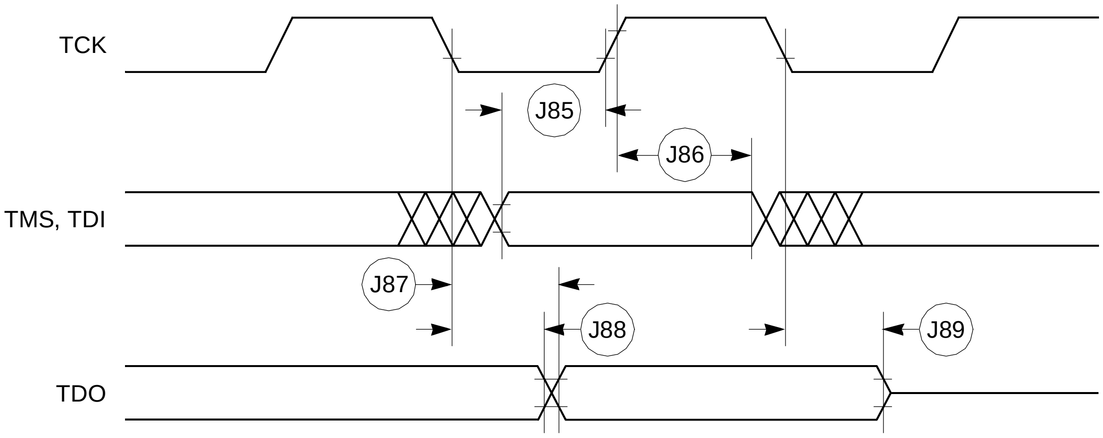


Figure 38. JTAG Test Access Port Timing Diagram

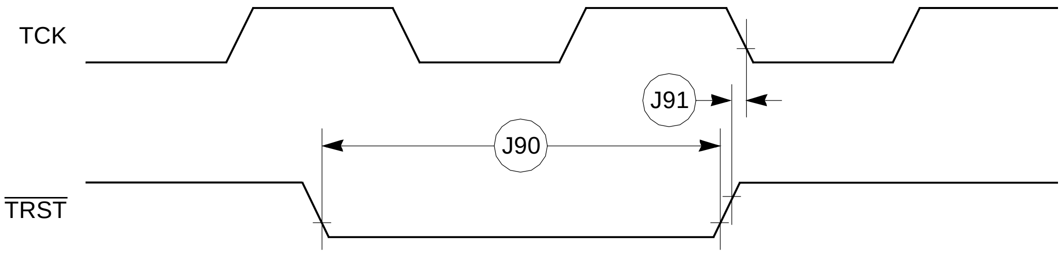


Figure 39. JTAG $\overline{\text{TRST}}$ Timing Diagram

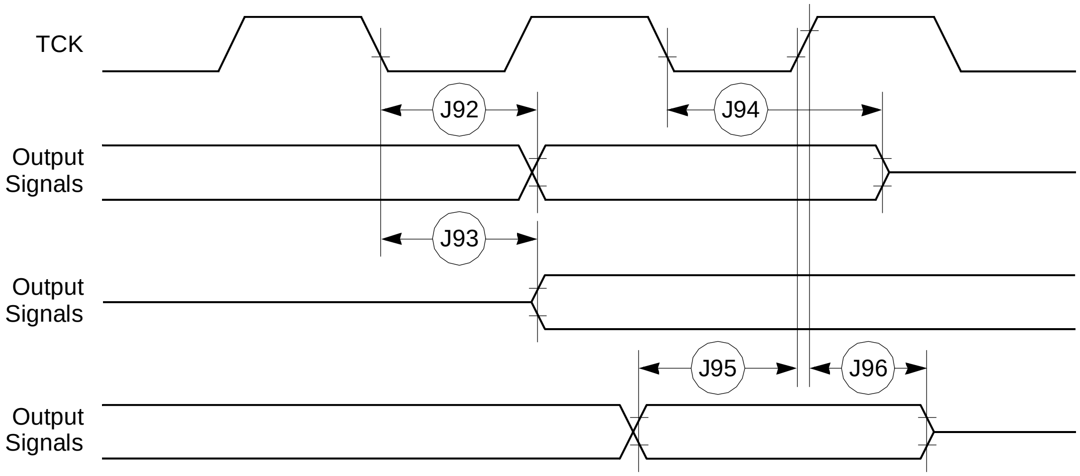


Figure 40. Boundary Scan (JTAG) Timing Diagram

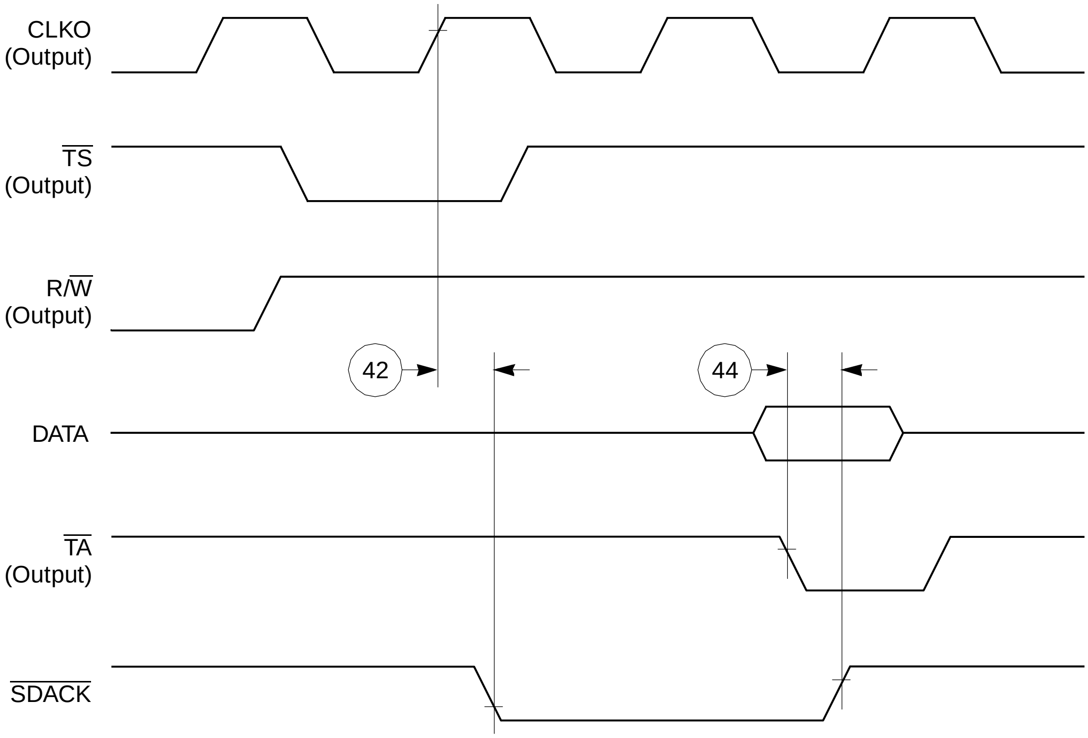


Figure 44. SDACK Timing Diagram—Peripheral Write, Internally-Generated TA

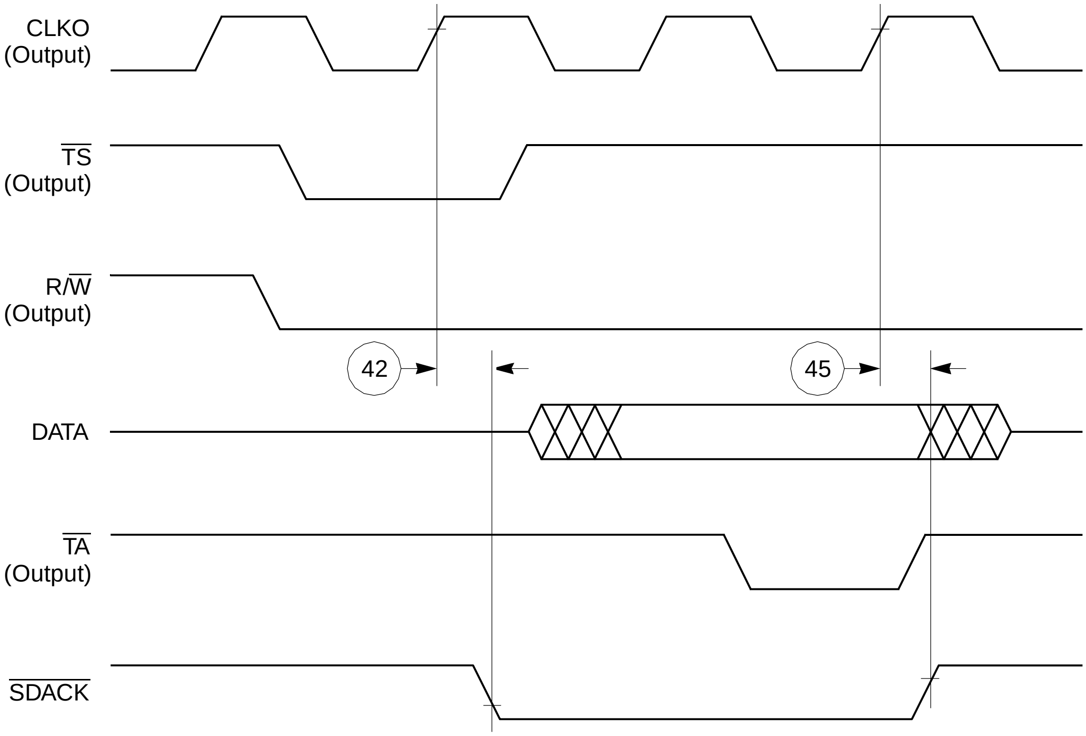


Figure 45. SDACK Timing Diagram—Peripheral Read, Internally-Generated TA

Table 21. SI Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
83a	L1RCLKB, L1TCLKB width high (DSC = 1)[3]	P + 10	—	ns
84	L1CLKB edge to L1CLKOB valid (DSC = 1)	—	30.00	ns
85	$\overline{\text{L1RQB}}$ valid before falling edge of L1TSYNCB[4]	1.00	—	L1TCLK
86	L1GRB setup time[2]	42.00	—	ns
87	L1GRB hold time	42.00	—	ns
88	L1CLKB edge to L1SYNCB valid (FSD = 00) CNT = 0000, BYT = 0, DSC = 0)	—	0.00	ns

[1] The ratio SYNCCLK/L1RCLKB must be greater than 2.5/1.

[2] These specs are valid for IDL mode only.

[3] Where P = 1/CLKOUT. Thus, for a 25-MHz CLKO1 rate, P = 40 ns.

[4] These strobes and TxD on the first bit of the frame become valid after the L1CLKB edge or L1SYNCB, whichever comes later.

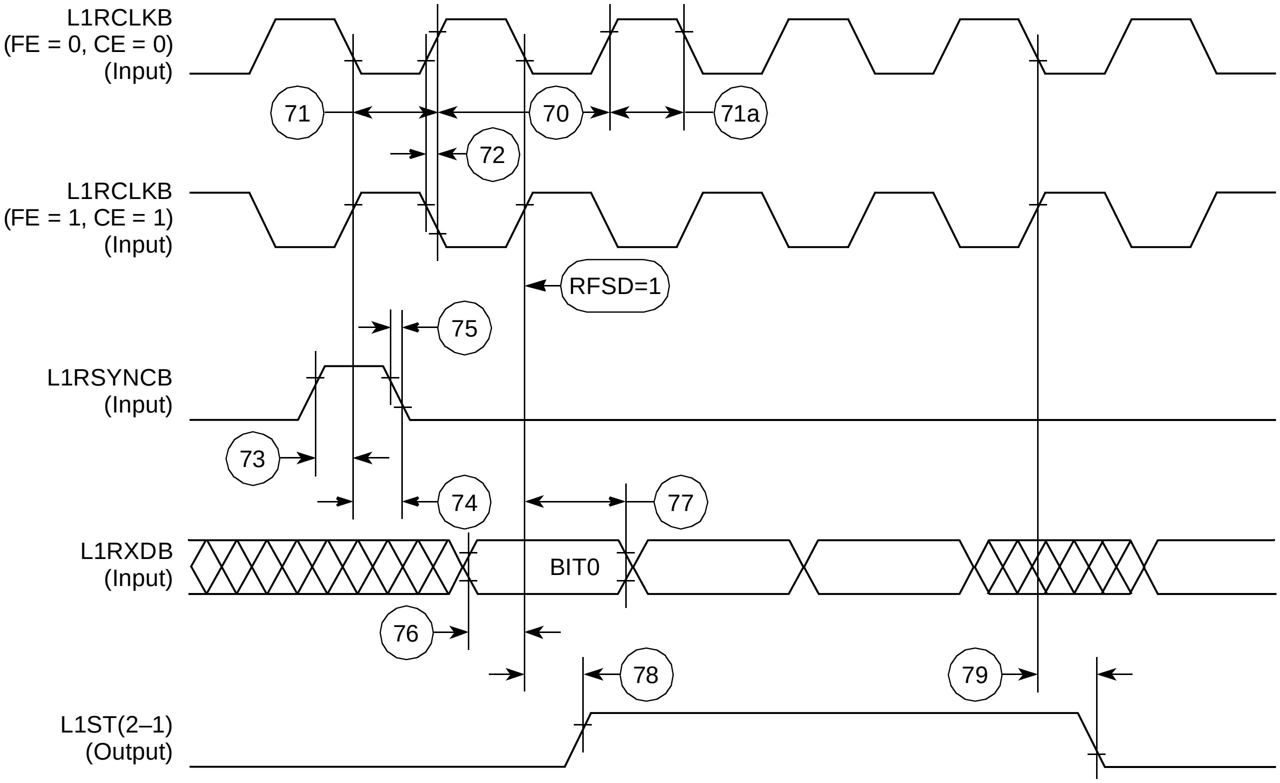


Figure 48. SI Receive Timing Diagram with Normal Clocking (DSC = 0)

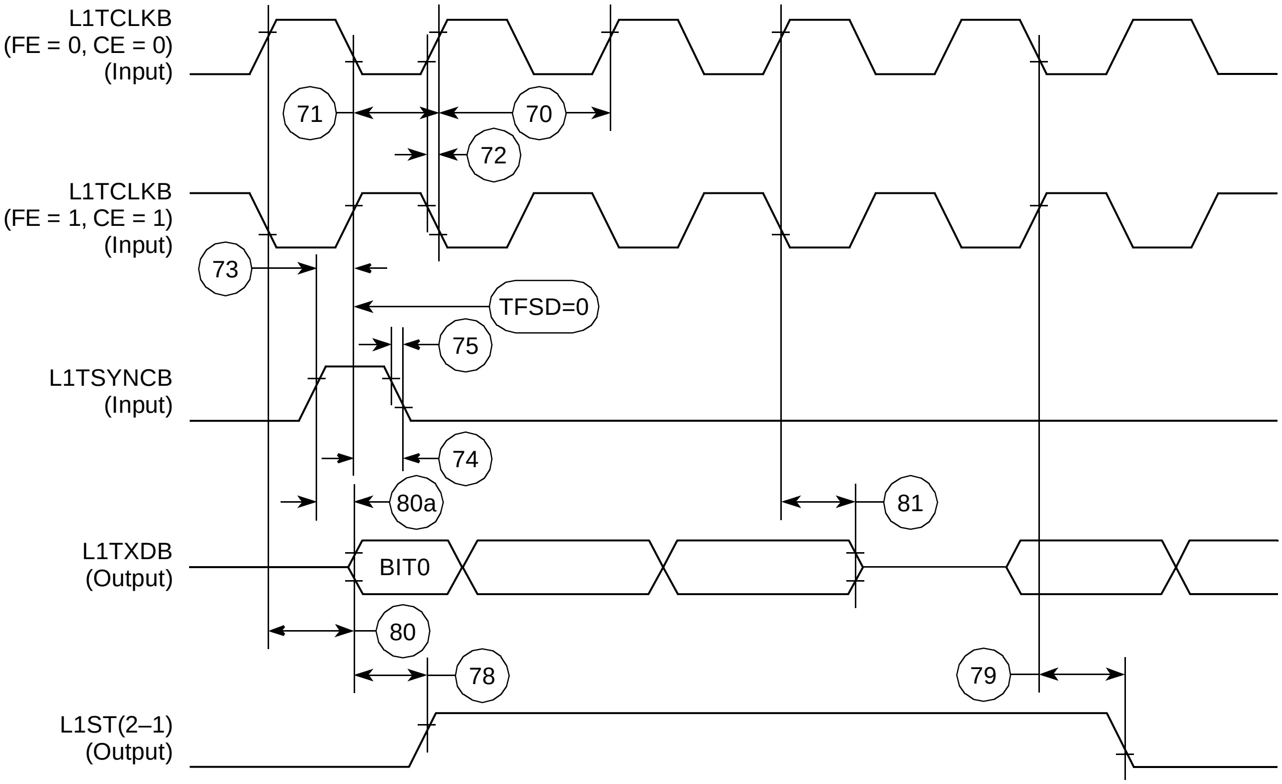


Figure 50. SI Transmit Timing Diagram (DSC = 0)

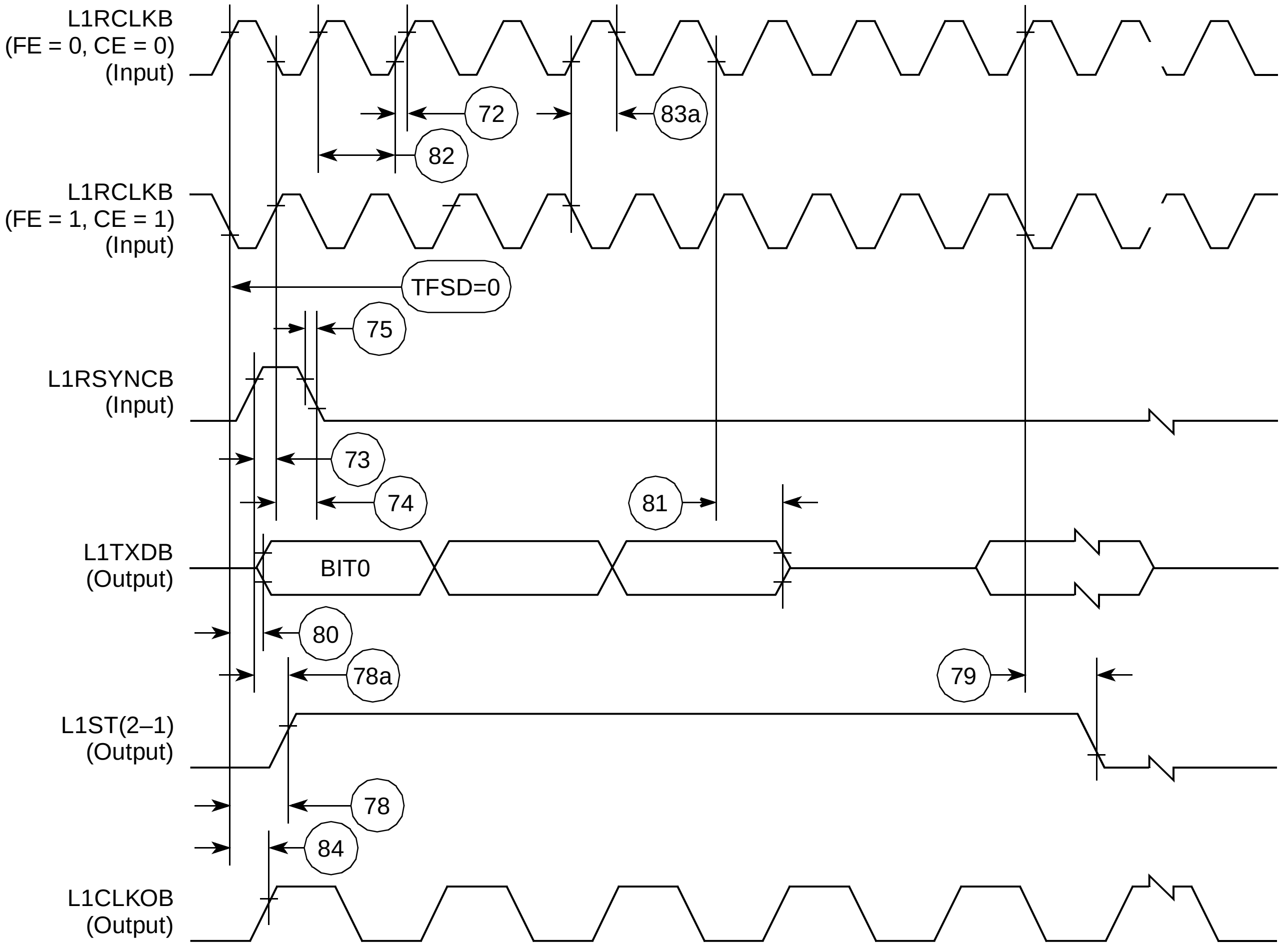


Figure 51. SI Transmit Timing with Double Speed Clocking (DSC = 1)

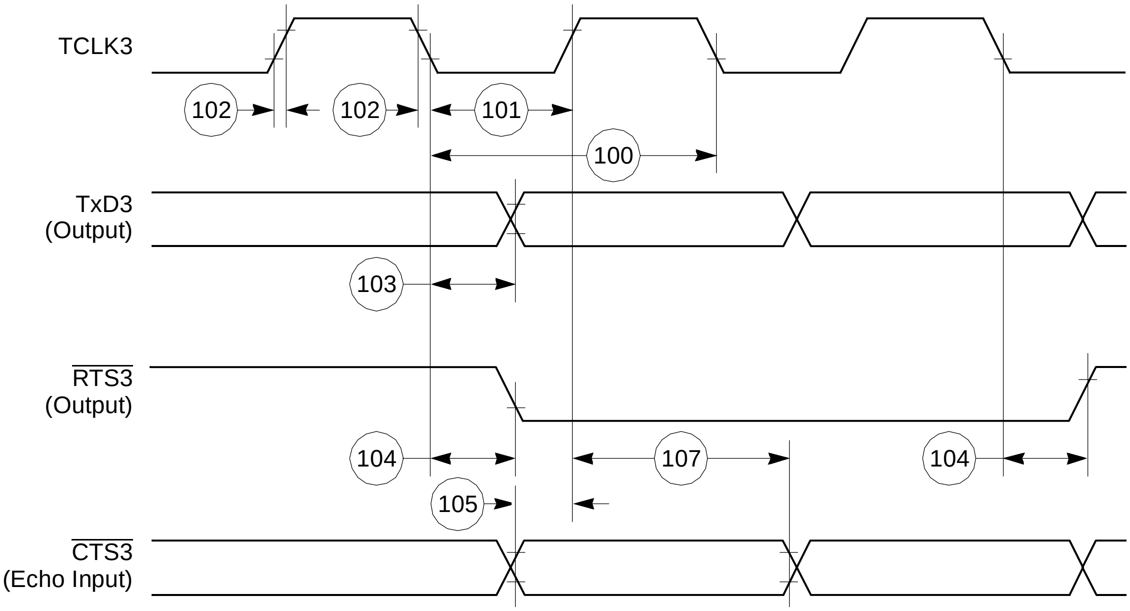


Figure 55. HDLC Bus Timing Diagram

13.7 Ethernet Electrical Specifications

Table 24 provides the Ethernet timings as shown in Figure 56 through Figure 58.

Table 24. Ethernet Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
120	CLSN width high	40	—	ns
121	RCLK3 rise/fall time	—	15	ns
122	RCLK3 width low	40	—	ns
123	RCLK3 clock period[1]	80	120	ns
124	RXD3 setup time	20	—	ns
125	RXD3 hold time	5	—	ns
126	RENA active delay (from RCLK3 rising edge of the last data bit)	10	—	ns
127	RENA width low	100	—	ns
128	TCLK3 rise/fall time	—	15	ns
129	TCLK3 width low	40	—	ns
130	TCLK3 clock period[1]	99	101	ns
131	TXD3 active delay (from TCLK3 rising edge)	—	50	ns
132	TXD3 inactive delay (from TCLK3 rising edge)	6.5	50	ns
133	TENA active delay (from TCLK3 rising edge)	10	50	ns
134	TENA inactive delay (from TCLK3 rising edge)	10	50	ns

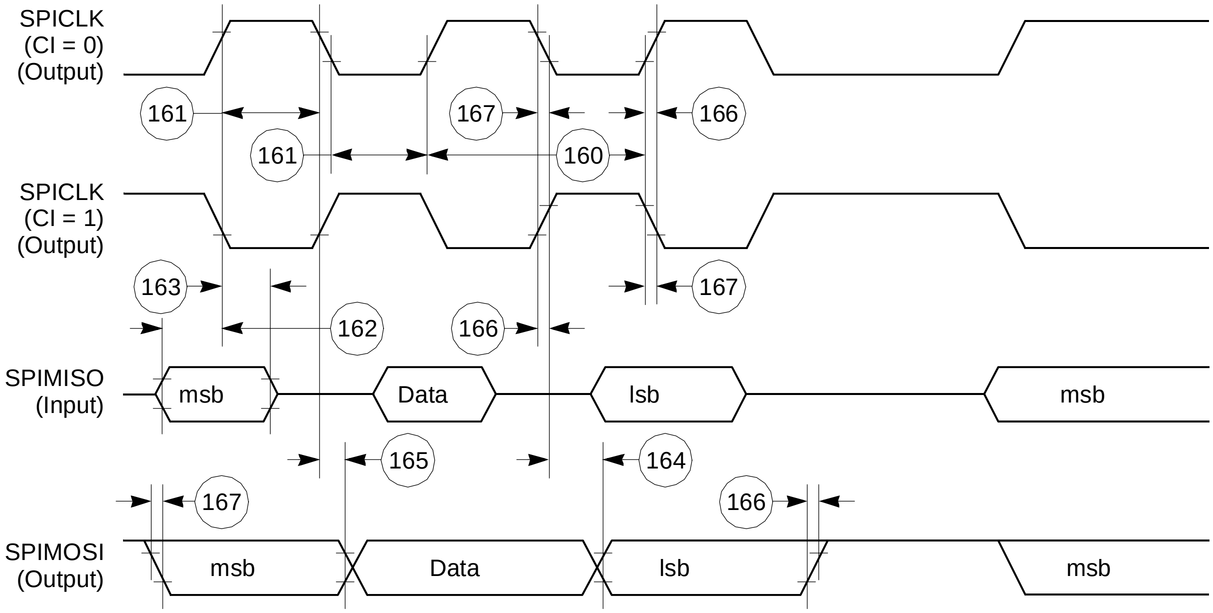


Figure 60. SPI Master (CP = 0) Timing Diagram

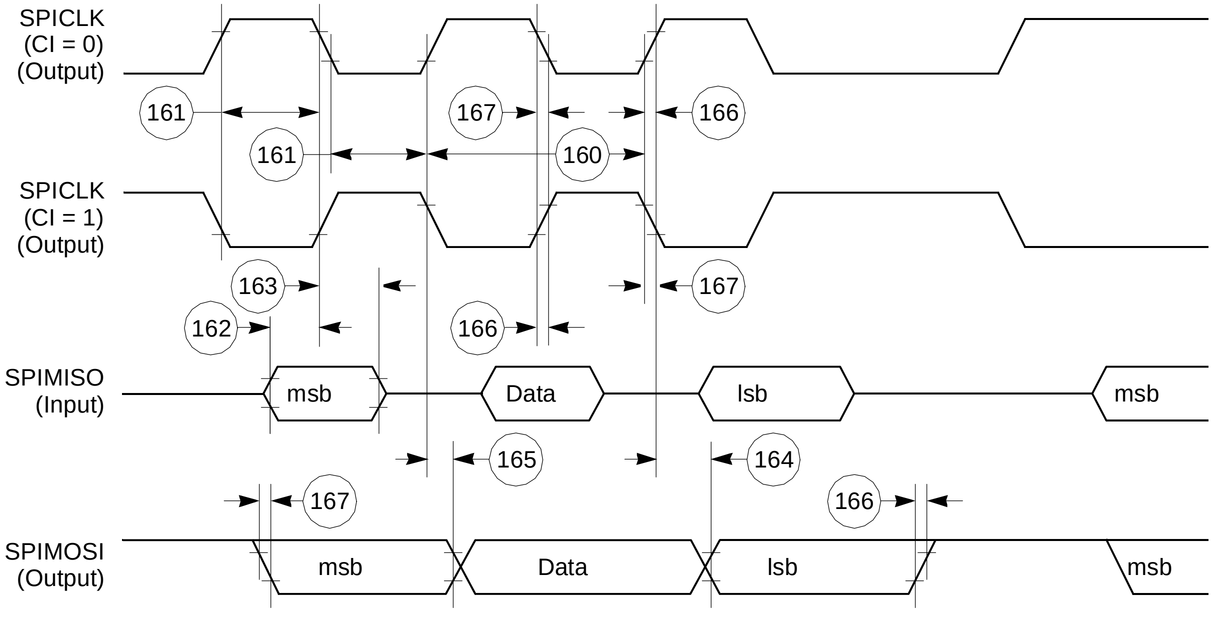


Figure 61. SPI Master (CP = 1) Timing Diagram

Figure 65 shows MII receive signal timing.

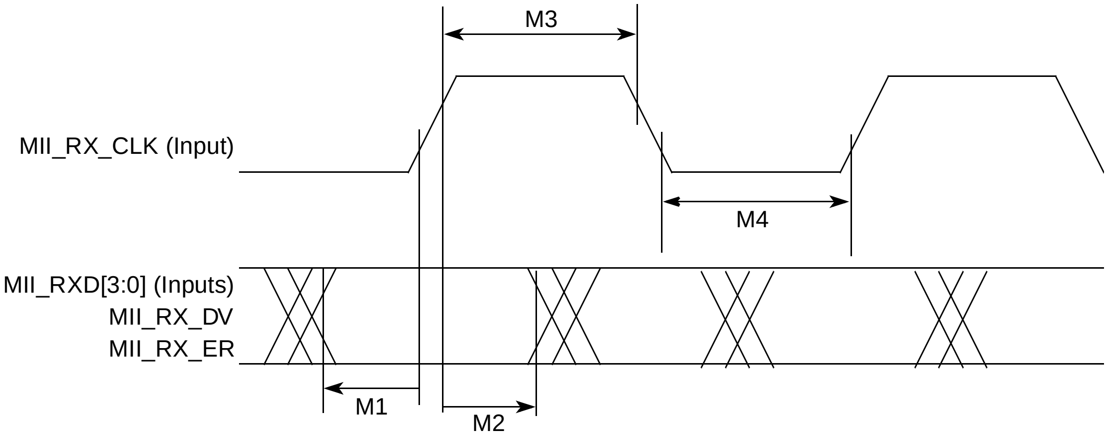


Figure 65. MII Receive Signal Timing Diagram

15.2 MII and Reduced MII Transmit Signal Timing

The transmitter functions correctly up to a MII_TX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_TX_CLK frequency – 1%.

Table 32 provides information on the MII transmit signal timing.

Table 32. MII Transmit Signal Timing

Num	Characteristic	Min	Max	Unit
M5	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER invalid	5	—	ns
M6	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER valid	—	25	ns
M7	MII_TX_CLK pulse width high	35%	65%	MII_TX_CLK period
M8	MII_TX_CLK pulse width low	35%	65%	MII_TX_CLK period
M20_RMII	RMII_TXD[1:0], RMII_TX_EN to RMII_REFCLK setup	4	—	ns
M21_RMII	RMII_TXD[1:0], RMII_TX_EN data hold from RMII_REFCLK rising edge	2	—	ns

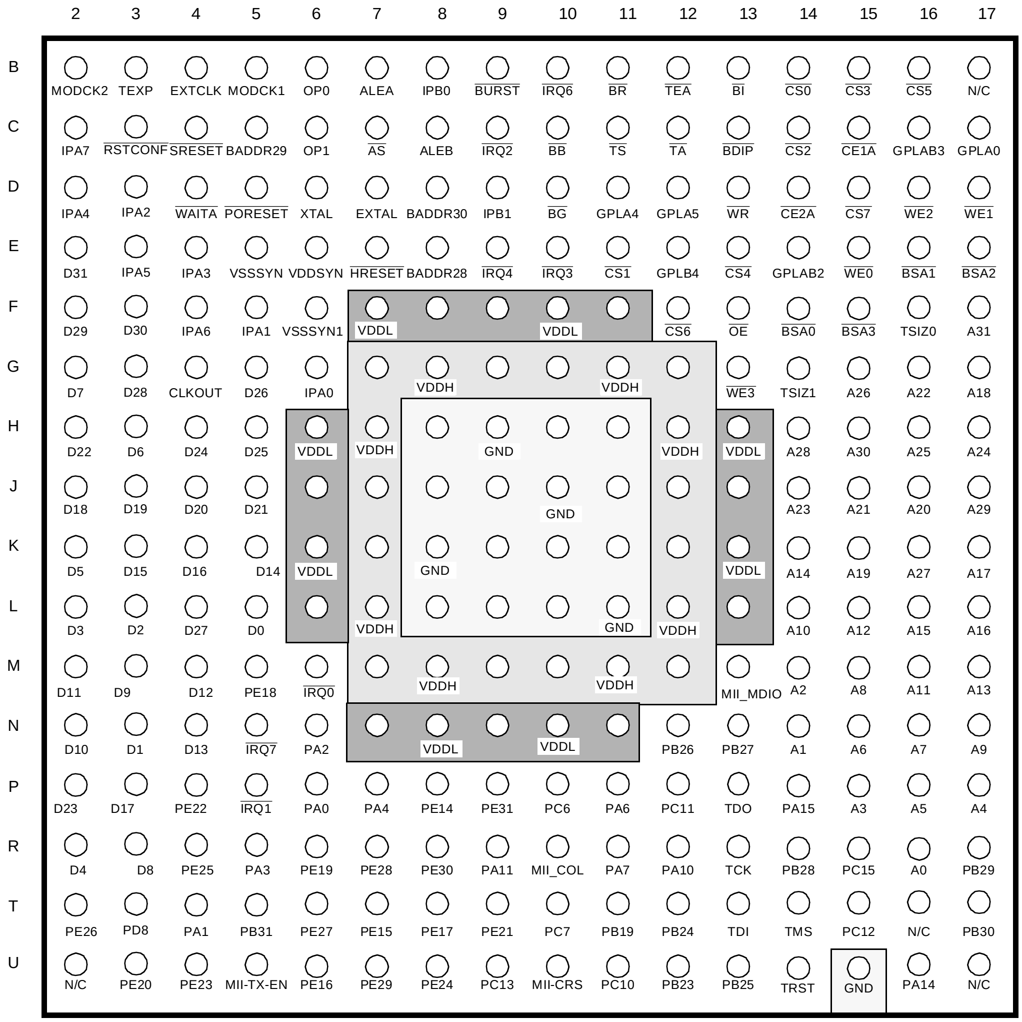
16.1 Pin Assignments

Figure 69 shows the JEDEC pinout of the PBGA package as viewed from the top surface. For additional information, see the *MPC885 PowerQUICC Family User's Manual*.

NOTE

The pin numbering starts with B2 in order to conform to the JEDEC standard for 23-mm body size using a 16 × 16 array.

NOTE: This is the top view of the device.



	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
B	MODCK2	TEXP	EXTCLK	MODCK1	OP0	ALEA	IPB0	BURST	IRQ6	BR	TEA	BI	CS0	CS3	CS5	N/C
C	IPA7	RSTCONF	SRESET	BADDR29	OP1	AS	ALEB	IRQ2	BB	TS	TA	BDIP	CS2	CE1A	GPLAB3	GPLA0
D	IPA4	IPA2	WAITA	PORESET	XTAL	EXTAL	BADDR30	IPB1	BG	GPLA4	GPLA5	WR	CE2A	CS7	WE2	WE1
E	D31	IPA5	IPA3	VSSSYN	VDDSYN	HRESET	BADDR28	IRQ4	IRQ3	CS1	GPLB4	CS4	GPLAB2	WE0	BSA1	BSA2
F	D29	D30	IPA6	IPA1	VSSSYN1	VDDL			VDDL		CS6	OE	BSA0	BSA3	TSIZ0	A31
G	D7	D28	CLKOUT	D26	IPA0		VDDH			VDDH		WE3	TSIZ1	A26	A22	A18
H	D22	D6	D24	D25	VDDL	VDDH		GND			VDDH	VDDL	A28	A30	A25	A24
J	D18	D19	D20	D21					GND				A23	A21	A20	A29
K	D5	D15	D16	D14	VDDL		GND					VDDL	A14	A19	A27	A17
L	D3	D2	D27	D0		VDDH				GND	VDDH		A10	A12	A15	A16
M	D11	D9	D12	PE18	IRQ0		VDDH			VDDH		MII_MDIO	A2	A8	A11	A13
N	D10	D1	D13	IRQ7	PA2		VDDL		VDDL		PB26	PB27	A1	A6	A7	A9
P	D23	D17	PE22	IRQ1	PA0	PA4	PE14	PE31	PC6	PA6	PC11	TDO	PA15	A3	A5	A4
R	D4	D8	PE25	PA3	PE19	PE28	PE30	PA11	MII_COL	PA7	PA10	TCK	PB28	PC15	A0	PB29
T	PE26	PD8	PA1	PB31	PE27	PE15	PE17	PE21	PC7	PB19	PB24	TDI	TMS	PC12	N/C	PB30
U	N/C	PE20	PE23	MII-TX-EN	PE16	PE29	PE24	PC13	MII-CRS	PC10	PB23	PB25	TRST	GND	PA14	N/C

Figure 69. Pinout of the PBGA Package—JEDEC Standard

Table 36. Pin Assignments—JEDEC Standard (continued)

Name	Pin Number	Type
IP_A6	F4	Input (3.3 V only)
IP_A7	C2	Input (3.3 V only)
ALE_B, DSCK	C8	Bidirectional Three-state (3.3 V only)
IP_B[0:1], IWP[0:1], VFLS[0:1]	B8, D9	Bidirectional (3.3 V only)
OP0	B6	Bidirectional (3.3 V only)
OP1	C6	Output
OP2, MODCK1, $\overline{\text{STS}}$	B5	Bidirectional (3.3 V only)
OP3, MODCK2, DSDO	B2	Bidirectional (3.3 V only)
BADDR[28:29]	E8, C5	Output
BADDR30, $\overline{\text{REG}}$	D8	Output
$\overline{\text{AS}}$	C7	Input (3.3 V only)
PA15, USBRXD	P14	Bidirectional
PA14, USBOE	U16	Bidirectional (Optional: open-drain)
PA11, RXD4, MII1-TXD0, RMII1-TXD0	R9	Bidirectional (Optional: open-drain) (5-V tolerant)
PA10, MII1-TXERR, TIN4, CLK7	R12	Bidirectional (Optional: open-drain) (5-V tolerant)
PA7, CLK1, BRGO1, TIN1	R11	Bidirectional
PA6, CLK2, $\overline{\text{TOUT1}}$	P11	Bidirectional
PA4, $\overline{\text{CTS4}}$, MII1-TXD1, RMII-TXD1	P7	Bidirectional
PA3, MII1-RXER, RMII1-RXER, BRGO3	R5	Bidirectional (5-V tolerant)
PA2, MII1-RXDV, RMII1-CRS_DV, TXD4	N6	Bidirectional (5-V tolerant)
PA1, MII1-RXD0, RMII1-RXD0, BRGO4	T4	Bidirectional (5-V tolerant)
PA0, MII1-RXD1, RMII1-RXD1, TOUT4	P6	Bidirectional (5-V tolerant)
PB31, $\overline{\text{SPISEL}}$, MII1-TXCLK, RMII1-REFCLK	T5	Bidirectional (Optional: open-drain) (5-V tolerant)

Table 36. Pin Assignments—JEDEC Standard (continued)

Name	Pin Number	Type
TDO, DSDO	P13	Output (5-V tolerant)
MII1_CRS	U10	Input
MII_MDIO	M13	Bidirectional (5-V tolerant)
MII1_TX_EN, RMII1_TX_EN	U5	Output (5-V tolerant)
MII1_COL	R10	Input
V_{SSSYN}	E5	PLL analog GND
V_{SSSYN1}	F6	PLL analog GND
V_{DDSYN}	E6	PLL analog V_{DD}
GND	H8, H9, H10, H11, J8, J9, J10, J11, K8, K9, K10, K11, L8, L9, L10, L11, U15	Power
V_{DDL}	F7, F8, F9, F10, F11, H6, H13, J6, J13, K6, K13, L6, L13, N7, N8, N9, N10, N11	Power
V_{DDH}	G7, G8, G9, G10, G11, G12, H7, H12, J7, J12, K7, K12, L7, L12, M7, M8, M9, M10, M11, M12	Power
N/C	B17, T16, U2, U17	No connect

17 Document Revision History

Table 37 lists significant changes between revisions of this hardware specification.

Table 37. Document Revision History

Revision Number	Date	Changes
0	2/2003	Initial release.
0.1	3/2003	Took out the time-slot assigner and changed the SCC for SCC3 to SCC4.
0.2	5/2003	Changed the package drawing, removed all references to Data Parity. Changed the SPI Master Timing Specs. 162 and 164. Added the RMII and USB timing. Added the 80-MHz timing.
0.3	5/2003	Made sure the pin types were correct. Changed the Features list to agree with the MPC885.
0.4	5/2003	Corrected the signals that had overlines on them. Made corrections on two pins that were typos.
0.5	5/2003	Changed the pin descriptions for PD8 and PD9.
0.6	5/2003	Changed a few typos. Put back the I^{2}C. Put in the new reset configuration, corrected the USB timing.
0.7	6/2003	Changed the pin descriptions per the June 22 spec, removed Utopia from the pin descriptions, changed PADIR, PBDIR, PCDIR and PDDIR to be 0 in the Mandatory Reset Config.
0.8	8/2003	Added the reference to USB 2.0 to the Features list and removed 1.1 from USB on the block diagrams.
0.9	8/2003	Changed the USB description to full-/low-speed compatible.
1.0	9/2003	Added the DSP information in the Features list. Put a new sentence under Mechanical Dimensions. Fixed table formatting. Nontechnical edits. Released to the external web.
1.1	10/2003	Added TDMb to the MPC875 Features list, the MPC875 Block Diagram, added 13.5 Serial Interface AC Electrical Specifications, and removed TDMa from the pin descriptions.
2.0	12/2003	Changed DBGC in the Mandatory Reset Configuration to X1. Changed the maximum operating frequency to 133 MHz. Put the timing in the 80 MHz column. Put in the orderable part numbers. Rounded the timings to hundredths in the 80 MHz column. Put the pin numbers in footnotes by the maximum currents in Table 6. Changed 22 and 41 in the Timing. Put TBD in the Thermal table.

Table 37. Document Revision History (continued)

Revision Number	Date	Changes
3.0	1/07/2004 7/19/2004	• Added sentence to Spec B1A about EXTCLK and CLKOUT being in alignment for integer values. • Added a footnote to Spec 41 specifying that EDM = 1. • Added the thermal numbers to Table 4. • Added RMII1_EN under M1II_EN in Table 36, Pin Assignments. • Added a table footnote to Table 6, DC Electrical Specifications, about meeting the V_{IL} Max of the I^2C Standard. • Put the new part numbers in the Ordering Information Section.
4	08/2007	• Updated template. • On page 1, updated first paragraph and added a second paragraph. • After Table 2, inserted a new figure showing the undershoot/overshoot voltage (Figure 3) and renumbered the rest of the figures. • In Table 10, for reset timings B29f and B29g added footnote indicating that the formula only applies to bus operation up to 50 MHz. • In Figure 5, changed all reference voltage measurement points from 0.2 and 0.8 V to 50% level. • In Table 18, changed num 46 description to read, “$\overline{\text{TA}}$ assertion to rising edge ...” • In Figure 43, changed $\overline{\text{TA}}$ to reflect the rising edge of the clock.

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