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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Active
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	133MHz
Co-Processors/DSP	Communications; CPM, Security; SEC
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (1), 10/100Mbps (2)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TA)
Security Features	Cryptography
Package / Case	256-BBGA
Supplier Device Package	256-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc875zt133

Features

- The MPC875 has a time-slot assigner (TSA) that supports one TDM bus (TDMb)
 - Allows SCC and SMC to run in multiplexed and/or non-multiplexed operation
 - Supports T1, CEPT, PCM highway, ISDN basic rate, ISDN primary rate, user-defined
 - 1- or 8-bit resolution
 - Allows independent transmit and receive routing, frame synchronization, and clocking
 - Allows dynamic changes
 - Can be internally connected to two serial channels (one SCC and one SMC)
- PCMCIA interface
 - Master (socket) interface, release 2.1-compliant
 - Supports one independent PCMCIA socket on the MPC875/MPC870
 - Eight memory or I/O windows supported
- Debug interface
 - Eight comparators: four operate on instruction address, two operate on data address, and two operate on data
 - Supports conditions: = ≠ < >
 - Each watchpoint can generate a break point internally
- Normal high and normal low power modes to conserve power
- 1.8-V core and 3.3-V I/O operation with 5-V TTL compatibility
- The MPC875/MPC870 comes in a 256-pin ball grid array (PBGA) package

The MPC875 block diagram is shown in Figure 1.

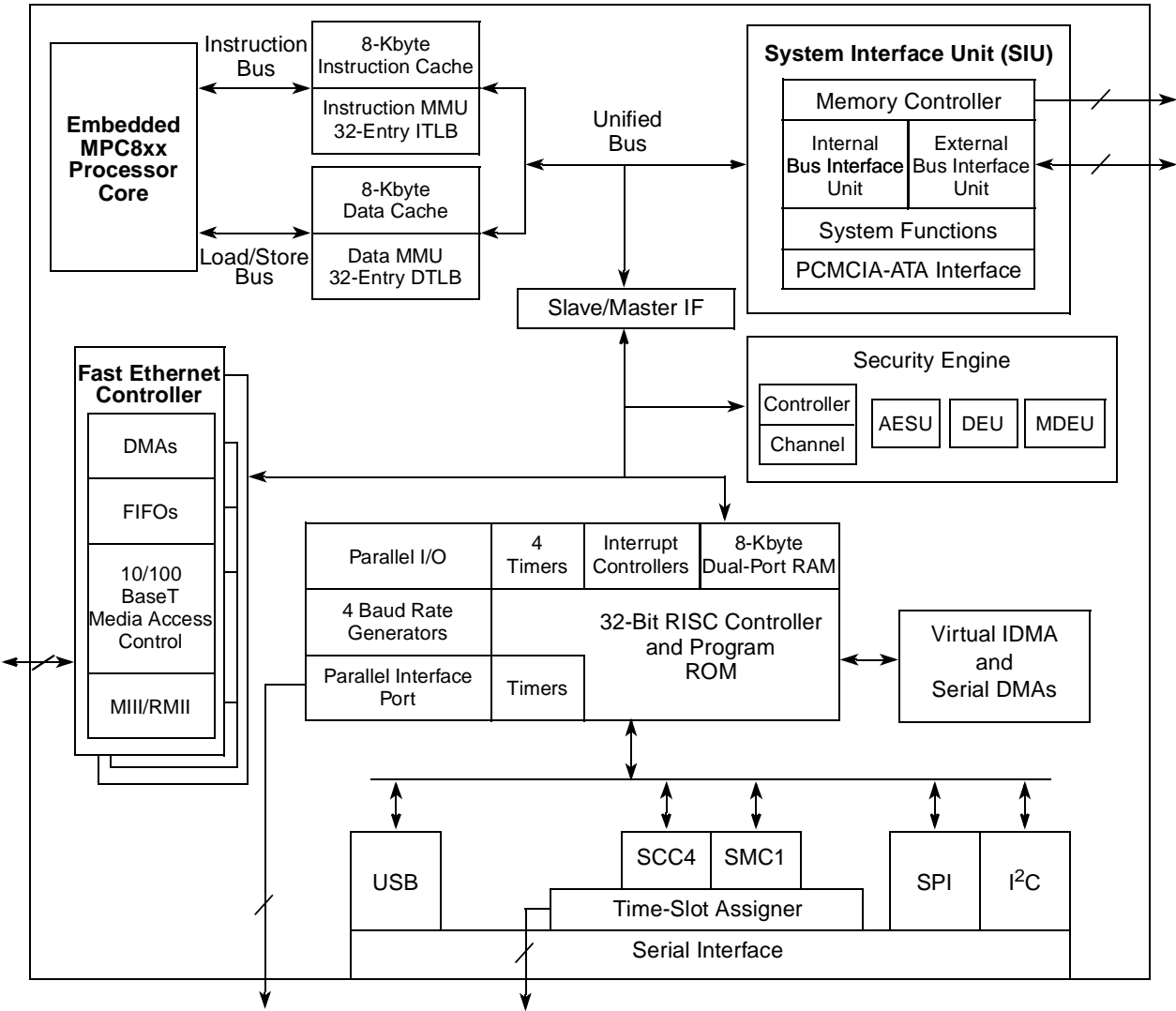


Figure 1. MPC875 Block Diagram

5 Power Dissipation

Table 5 provides information on power dissipation. The modes are 1:1, where CPU and bus speeds are equal, and 2:1, where CPU frequency is twice bus speed.

Table 5. Power Dissipation (P_D)

Die Revision	Bus Mode	Frequency	Typical ¹	Maximum ²	Unit
0	1:1	66 MHz	310	390	mW
		80 MHz	350	430	mW
	2:1	133 MHz	430	495	mW

¹ Typical power dissipation is measured at $V_{DDL} = V_{DDSYN} = 1.8$ V, and V_{DDH} is at 3.3 V.

² Maximum power dissipation at $V_{DDL} = V_{DDSYN} = 1.9$ V, and V_{DDH} is at 3.5 V.

NOTE

The values in Table 5 represent V_{DDL} -based power dissipation and do not include I/O power dissipation over V_{DDH} . I/O power dissipation varies widely by application due to buffer current, depending on external circuitry.

The V_{DDSYN} power dissipation is negligible.

6 DC Characteristics

Table 6 provides the DC electrical characteristics for the MPC875/MPC870.

Table 6. DC Electrical Specifications

Characteristic	Symbol	Min	Max	Unit
Operating voltage	V_{DDH} (I/O)	3.135	3.465	V
	V_{DDL} (core)	1.7	1.9	V
	V_{DDSYN} ¹	1.7	1.9	V
	Difference between V_{DDL} and V_{DDSYN}	—	100	mV
Input high voltage (all inputs except EXTAL and EXTCLK) ²	V_{IH}	2.0	3.465	V
Input low voltage ³	V_{IL}	GND	0.8	V
EXTAL, EXTCLK input high voltage	V_{IHC}	$0.7 \times V_{DDH}$	V_{DDH}	V
Input leakage current, $V_{in} = 5.5$ V (except TMS, \overline{TRST} , DSCK, and DSDI pins) for 5-V tolerant pins ¹	I_{in}	—	100	μ A
Input leakage current, $V_{in} = V_{DDH}$ (except TMS, \overline{TRST} , DSCK, and DSDI)	I_{In}	—	10	μ A
Input leakage current, $V_{in} = 0$ V (except TMS, \overline{TRST} , DSCK, and DSDI pins)	I_{In}	—	10	μ A
Input capacitance ⁴	C_{in}	—	20	pF

Table 10. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B15	CLKOUT to \overline{TEA} High-Z (MIN = $0.00 \times B1 + 2.50$)	2.50	15.00	2.50	15.00	2.50	15.00	2.50	15.00	ns
B16	\overline{TA} , \overline{BI} valid to CLKOUT (setup time) (MIN = $0.00 \times B1 + 6.00$)	6.00	—	6.00	—	6.00	—	6	—	ns
B16a	\overline{TEA} , \overline{KR} , \overline{RETRY} , \overline{CR} valid to CLKOUT (setup time) (MIN = $0.00 \times B1 + 4.5$)	4.50	—	4.50	—	4.50	—	4.50	—	ns
B16b	\overline{BB} , \overline{BG} , \overline{BR} , valid to CLKOUT (setup time) ² (4MIN = $0.00 \times B1 + 0.00$)	4.00	—	4.00	—	4.00	—	4.00	—	ns
B17	CLKOUT to \overline{TA} , \overline{TEA} , \overline{BI} , \overline{BB} , \overline{BG} , \overline{BR} valid (hold time) (MIN = $0.00 \times B1 + 1.00^3$)	1.00	—	1.00	—	2.00	—	2.00	—	ns
B17a	CLKOUT to \overline{KR} , \overline{RETRY} , \overline{CR} valid (hold time) (MIN = $0.00 \times B1 + 2.00$)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B18	D(0:31) valid to CLKOUT rising edge (setup time) ⁴ (MIN = $0.00 \times B1 + 6.00$)	6.00	—	6.00	—	6.00	—	6.00	—	ns
B19	CLKOUT rising edge to D(0:31) valid (hold time) ⁴ (MIN = $0.00 \times B1 + 1.00^5$)	1.00	—	1.00	—	2.00	—	2.00	—	ns
B20	D(0:31) valid to CLKOUT falling edge (setup time) ⁶ (MIN = $0.00 \times B1 + 4.00$)	4.00	—	4.00	—	4.00	—	4.00	—	ns
B21	CLKOUT falling edge to D(0:31) valid (hold time) ⁶ (MIN = $0.00 \times B1 + 2.00$)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B22	CLKOUT rising edge to \overline{CS} asserted GPCM ACS = 00 (MAX = $0.25 \times B1 + 6.3$)	7.60	13.80	6.30	12.50	3.80	10.00	3.13	9.43	ns
B22a	CLKOUT falling edge to \overline{CS} asserted GPCM ACS = 10, $TRLX = 0$ (MAX = $0.00 \times B1 + 8.00$)	—	8.00	—	8.00	—	8.00	—	8.00	ns
B22b	CLKOUT falling edge to \overline{CS} asserted GPCM ACS = 11, $TRLX = 0$, $EBDF = 0$ (MAX = $0.25 \times B1 + 6.3$)	7.60	13.80	6.30	12.50	3.80	10.00	3.13	9.43	ns
B22c	CLKOUT falling edge to \overline{CS} asserted GPCM ACS = 11, $TRLX = 0$, $EBDF = 1$ (MAX = $0.375 \times B1 + 6.6$)	10.90	18.00	10.90	16.00	5.20	12.30	4.69	10.93	ns
B23	CLKOUT rising edge to \overline{CS} negated GPCM read access, GPCM write access ACS = 00, $TRLX = 0$ and $CSNT = 0$ (MAX = $0.00 \times B1 + 8.00$)	2.00	8.00	2.00	8.00	2.00	8.00	2.00	8.00	ns
B24	A(0:31) and $BADDR(28:30)$ to \overline{CS} asserted GPCM ACS = 10, $TRLX = 0$ (MIN = $0.25 \times B1 - 2.00$)	5.60	—	4.30	—	1.80	—	1.13	—	ns
B24a	A(0:31) and $BADDR(28:30)$ to \overline{CS} asserted GPCM ACS = 11, $TRLX = 0$ (MIN = $0.50 \times B1 - 2.00$)	13.20	—	10.50	—	5.60	—	4.25	—	ns

Table 10. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B33a	CLKOUT rising edge to $\overline{\text{GPL}}$ valid as requested by control bit GxT3 in the corresponding word in the UPM (MAX = $0.25 \times B1 + 6.80$)	7.60	14.30	6.30	13.00	3.80	10.50	3.13	10.00	ns
B34	A(0:31), BADDR(28:30), and D(0:31) to $\overline{\text{CS}}$ valid, as requested by control bit CST4 in the corresponding word in the UPM (MIN = $0.25 \times B1 - 2.00$)	5.60	—	4.30	—	1.80	—	1.13	—	ns
B34a	A(0:31), BADDR(28:30), and D(0:31) to $\overline{\text{CS}}$ valid, as requested by control bit CST1 in the corresponding word in the UPM (MIN = $0.50 \times B1 - 2.00$)	13.20	—	10.50	—	5.60	—	4.25	—	ns
B34b	A(0:31), BADDR(28:30), and D(0:31) to $\overline{\text{CS}}$ valid, as requested by CST2 in the corresponding word in UPM (MIN = $0.75 \times B1 - 2.00$)	20.70	—	16.70	—	9.40	—	6.80	—	ns
B35	A(0:31), BADDR(28:30) to $\overline{\text{CS}}$ valid as requested by control bit BST4 in the corresponding word in the UPM (MIN = $0.25 \times B1 - 2.00$)	5.60	—	4.30	—	1.80	—	1.13	—	ns
B35a	A(0:31), BADDR(28:30), and D(0:31) to $\overline{\text{BS}}$ valid as requested by BST1 in the corresponding word in the UPM (MIN = $0.50 \times B1 - 2.00$)	13.20	—	10.50	—	5.60	—	4.25	—	ns
B35b	A(0:31), BADDR(28:30), and D(0:31) to $\overline{\text{BS}}$ valid as requested by control bit BST2 in the corresponding word in the UPM (MIN = $0.75 \times B1 - 2.00$)	20.70	—	16.70	—	9.40	—	7.40	—	ns
B36	A(0:31), BADDR(28:30), and D(0:31) to $\overline{\text{GPL}}$ valid as requested by control bit GxT4 in the corresponding word in the UPM (MIN = $0.25 \times B1 - 2.00$)	5.60	—	4.30	—	1.80	—	1.13	—	ns
B37	UPWAIT valid to CLKOUT falling edge ⁹ (MIN = $0.00 \times B1 + 6.00$)	6.00	—	6.00	—	6.00	—	6.00	—	ns
B38	CLKOUT falling edge to UPWAIT valid ⁹ (MIN = $0.00 \times B1 + 1.00$)	1.00	—	1.00	—	1.00	—	1.00	—	ns
B39	$\overline{\text{AS}}$ valid to CLKOUT rising edge ¹⁰ (MIN = $0.00 \times B1 + 7.00$)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B40	A(0:31), TSIZ(0:1), RD/ $\overline{\text{WR}}$, $\overline{\text{BURST}}$ valid to CLKOUT rising edge (MIN = $0.00 \times B1 + 7.00$)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B41	$\overline{\text{TS}}$ valid to CLKOUT rising edge (setup time) (MIN = $0.00 \times B1 + 7.00$)	7.00	—	7.00	—	7.00	—	7.00	—	ns

Table 10. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B42	CLKOUT rising edge to \overline{TS} valid (hold time) (MIN = $0.00 \times B1 + 2.00$)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B43	\overline{AS} negation to memory controller signals negation (MAX = TBD)	—	TBD	—	TBD	—	TBD	—	TBD	ns

¹ For part speeds above 50 MHz, use 9.80 ns for B11a.

² The timing required for \overline{BR} input is relevant when the MPC875/MPC870 is selected to work with the internal bus arbiter. The timing for \overline{BG} input is relevant when the MPC875/MPC870 is selected to work with the external bus arbiter.

³ For part speeds above 50 MHz, use 2 ns for B17.

⁴ The D(0:31) input timings B18 and B19 refer to the rising edge of the CLKOUT in which the \overline{TA} input signal is asserted.

⁵ For part speeds above 50 MHz, use 2 ns for B19.

⁶ The D(0:31) input timings B20 and B21 refer to the falling edge of the CLKOUT. This timing is valid only for read accesses controlled by chip-selects under control of the user-programmable machine (UPM) in the memory controller, for data beats where DLT3 = 1 in the RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

⁷ This formula applies to bus operation up to 50 MHz.

⁸ The timing B30 refers to \overline{CS} when ACS = 00 and to $\overline{WE}(0:3)$ when CSNT = 0.

⁹ The signal UPWAIT is considered asynchronous to the CLKOUT and synchronized internally. The timings specified in B37 and B38 are specified to enable the freeze of the UPM output signals as described in [Figure 20](#).

¹⁰ The \overline{AS} signal is considered asynchronous to the CLKOUT. The timing B39 is specified in order to allow the behavior specified in [Figure 23](#).

Figure 9 provides the timing for the synchronous input signals.

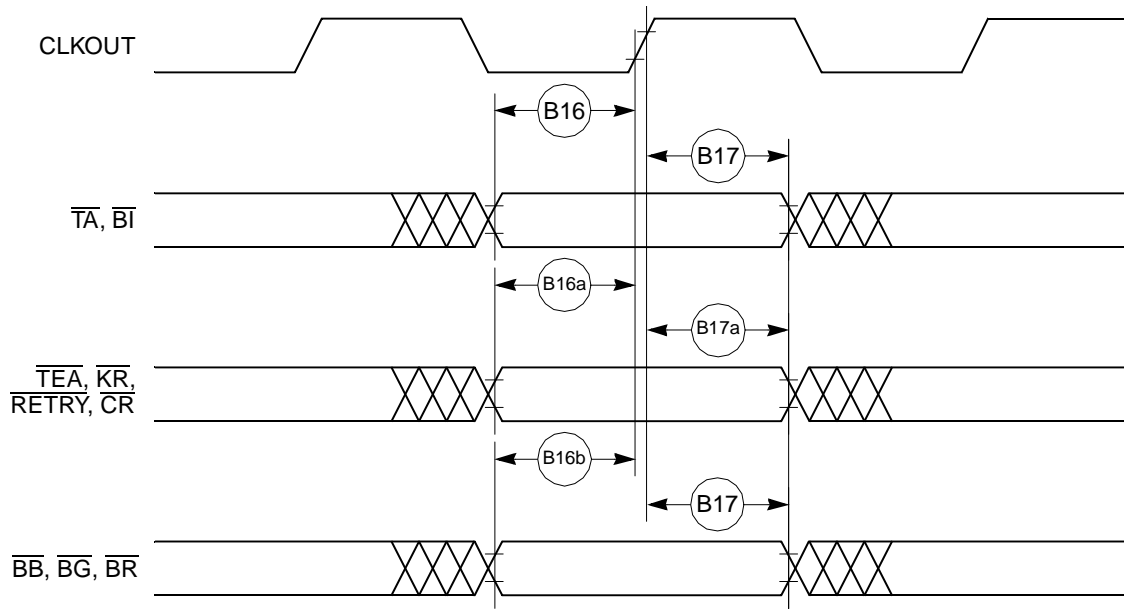


Figure 9. Synchronous Input Signals Timing

Figure 10 provides normal case timing for input data. It also applies to normal read accesses under the control of the user-programmable machine (UPM) in the memory controller.

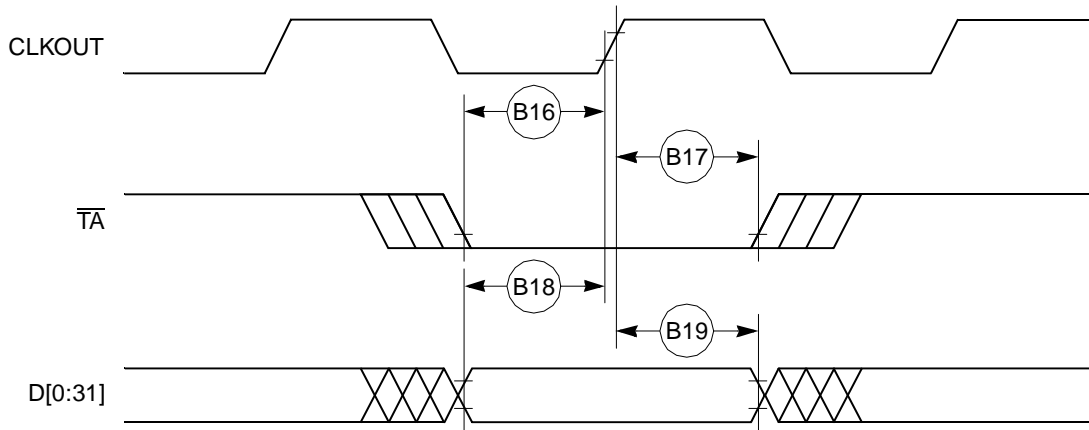


Figure 10. Input Data Timing in Normal Case

Figure 11 provides the timing for the input data controlled by the UPM for data beats where $DLT3 = 1$ in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

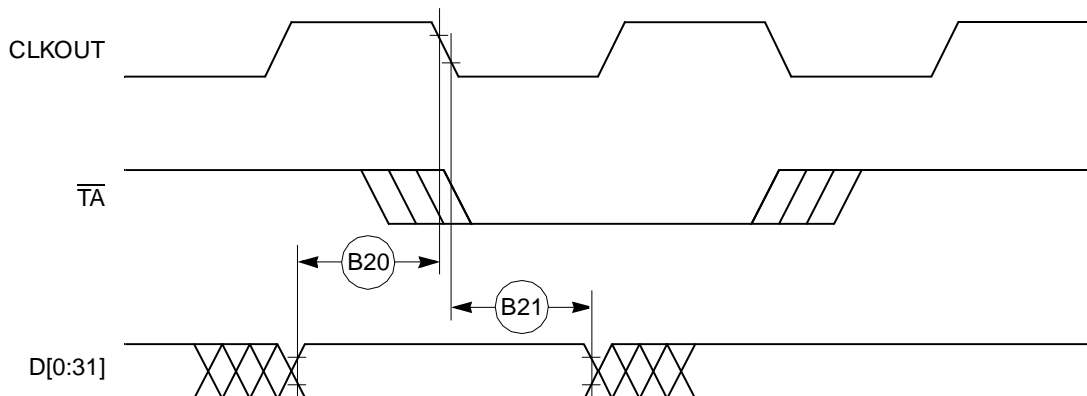


Figure 11. Input Data Timing when Controlled by UPM in the Memory Controller and $DLT3 = 1$

Figure 12 through Figure 15 provide the timing for the external bus read controlled by various GPCM factors.

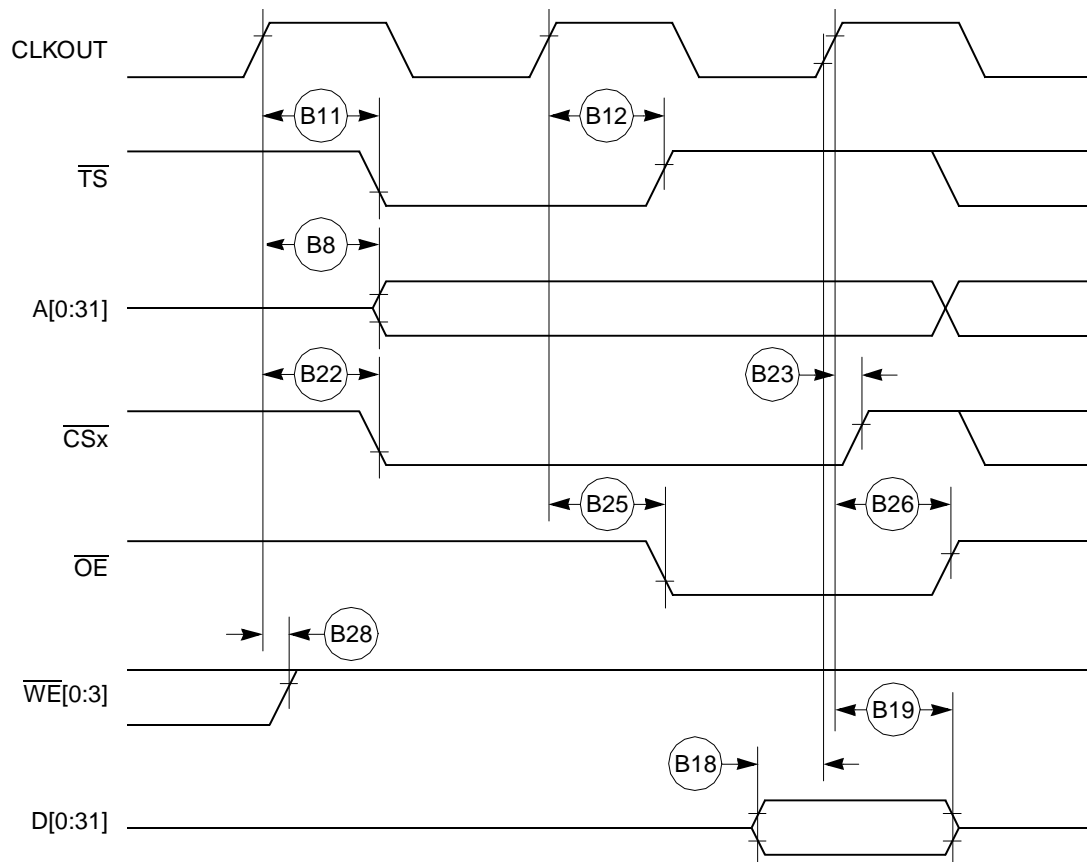


Figure 12. External Bus Read Timing (GPCM Controlled— $ACS = 00$)

Table 12 shows the PCMCIA timing for the MPC875/MPC870.

Table 12. PCMCIA Timing

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
P44	A(0:31), $\overline{\text{REG}}$ valid to PCMCIA strobe asserted ¹ (MIN = $0.75 \times B1 - 2.00$)	20.70	—	16.70	—	9.40	—	7.40	—	ns
P45	A(0:31), $\overline{\text{REG}}$ valid to ALE negation ¹ (MIN = $1.00 \times B1 - 2.00$)	28.30	—	23.00	—	13.20	—	10.50	—	ns
P46	CLKOUT to $\overline{\text{REG}}$ valid (MAX = $0.25 \times B1 + 8.00$)	7.60	15.60	6.30	14.30	3.80	11.80	3.13	11.13	ns
P47	CLKOUT to $\overline{\text{REG}}$ invalid (MIN = $0.25 \times B1 + 1.00$)	8.60	—	7.30	—	4.80	—	4.125	—	ns
P48	CLKOUT to $\overline{\text{CE1}}$, $\overline{\text{CE2}}$ asserted (MAX = $0.25 \times B1 + 8.00$)	7.60	15.60	6.30	14.30	3.80	11.80	3.13	11.13	ns
P49	CLKOUT to $\overline{\text{CE1}}$, $\overline{\text{CE2}}$ negated (MAX = $0.25 \times B1 + 8.00$)	7.60	15.60	6.30	14.30	3.80	11.80	3.13	11.13	ns
P50	CLKOUT to $\overline{\text{PCOE}}$, $\overline{\text{IORD}}$, $\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ assert time (MAX = $0.00 \times B1 + 11.00$)	—	11.00	—	11.00	—	11.00	—	11.00	ns
P51	CLKOUT to $\overline{\text{PCOE}}$, $\overline{\text{IORD}}$, $\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ negate time (MAX = $0.00 \times B1 + 11.00$)	2.00	11.00	2.00	11.00	2.00	11.00	2.00	11.00	ns
P52	CLKOUT to ALE assert time (MAX = $0.25 \times B1 + 6.30$)	7.60	13.80	6.30	12.50	3.80	10.00	3.13	9.40	ns
P53	CLKOUT to ALE negate time (MAX = $0.25 \times B1 + 8.00$)	—	15.60	—	14.30	—	11.80	—	11.13	ns
P54	$\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ negated to D(0:31) invalid ¹ (MIN = $0.25 \times B1 - 2.00$)	5.60	—	4.30	—	1.80	—	1.125	—	ns
P55	$\overline{\text{WAITA}}$ and $\overline{\text{WAITB}}$ valid to CLKOUT rising edge ¹ (MIN = $0.00 \times B1 + 8.00$)	8.00	—	8.00	—	8.00	—	8.00	—	ns
P56	CLKOUT rising edge to $\overline{\text{WAITA}}$ and $\overline{\text{WAITB}}$ invalid ¹ (MIN = $0.00 \times B1 + 2.00$)	2.00	—	2.00	—	2.00	—	2.00	—	ns

¹ PSST = 1. Otherwise add PSST times cycle time.

PSHT = 0. Otherwise add PSHT times cycle time.

These synchronous timings define when the $\overline{\text{WAITA}}$ signals are detected in order to freeze (or relieve) the PCMCIA current cycle. The $\overline{\text{WAITA}}$ assertion will be effective only if it is detected 2 cycles before the PSL timer expiration. See Chapter 16, "PCMCIA Interface," in the *MPC885 PowerQUICC™ Family Reference Manual*.

Table 13 shows the PCMCIA port timing for the MPC875/MPC870.

Table 13. PCMCIA Port Timing

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
P57	CLKOUT to OPx valid (MAX = $0.00 \times B1 + 19.00$)	—	19.00	—	19.00	—	19.00	—	19.00	ns
P58	$\overline{\text{HRESET}}$ negated to OPx drive ¹ (MIN = $0.75 \times B1 + 3.00$)	25.70	—	21.70	—	14.40	—	12.40	—	ns
P59	IP_Xx valid to CLKOUT rising edge (MIN = $0.00 \times B1 + 5.00$)	5.00	—	5.00	—	5.00	—	5.00	—	ns
P60	CLKOUT rising edge to IP_Xx invalid (MIN = $0.00 \times B1 + 1.00$)	1.00	—	1.00	—	1.00	—	1.00	—	ns

¹ OP2 and OP3 only.

Figure 30 provides the PCMCIA output port timing for the MPC875/MPC870.

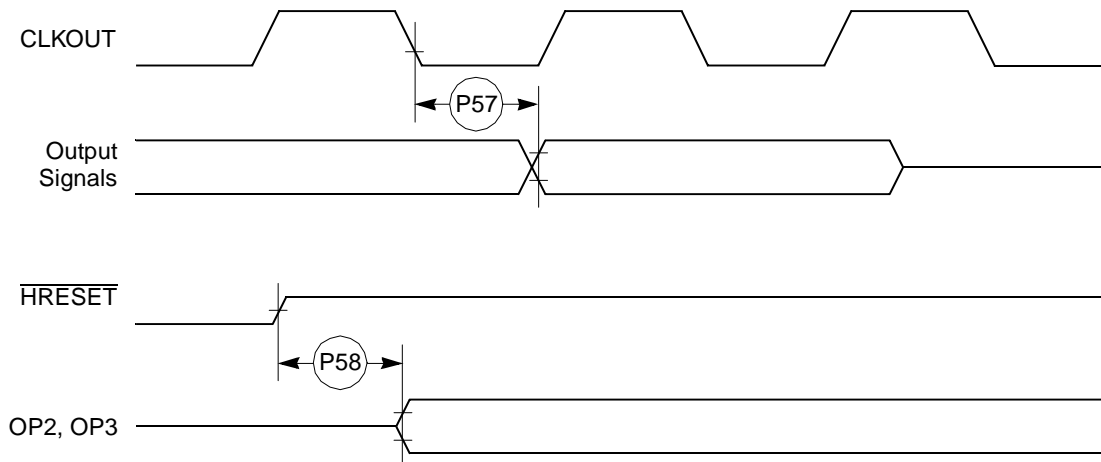


Figure 30. PCMCIA Output Port Timing

Figure 31 provides the PCMCIA input port timing for the MPC875/MPC870.

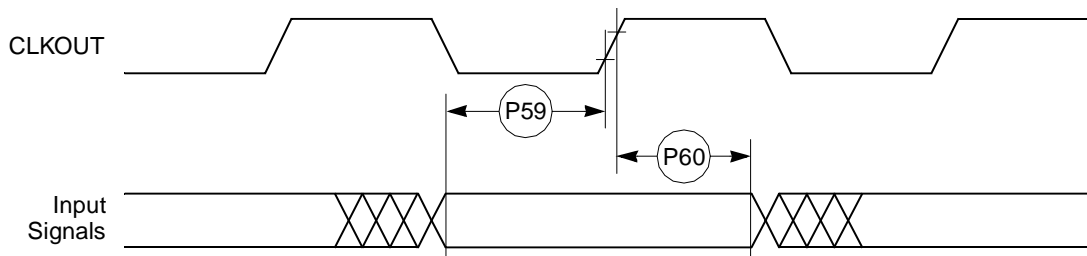


Figure 31. PCMCIA Input Port Timing

Table 14 shows the debug port timing for the MPC875/MPC870.

Table 14. Debug Port Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
D61	DSCK cycle time	$3 \times T_{\text{CLOCKOUT}}$		—
D62	DSCK clock pulse width	$1.25 \times T_{\text{CLOCKOUT}}$		—
D63	DSCK rise and fall times	0.00	3.00	ns
D64	DSDI input data setup time	8.00		ns
D65	DSDI data hold time	5.00		ns
D66	DSCK low to DSDO data valid	0.00	15.00	ns
D67	DSCK low to DSDO invalid	0.00	2.00	ns

Figure 32 provides the input timing for the debug port clock.

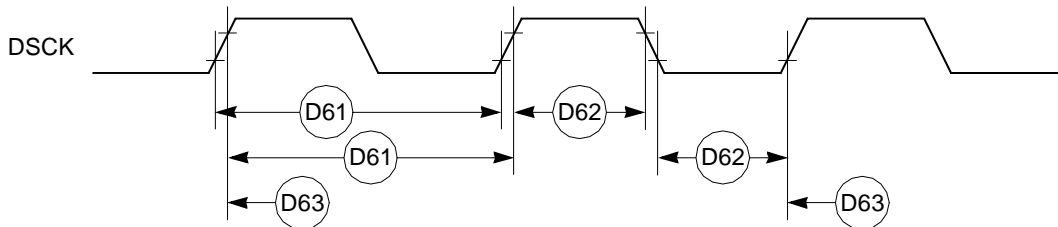


Figure 32. Debug Port Clock Input Timing

Figure 33 provides the timing for the debug port.

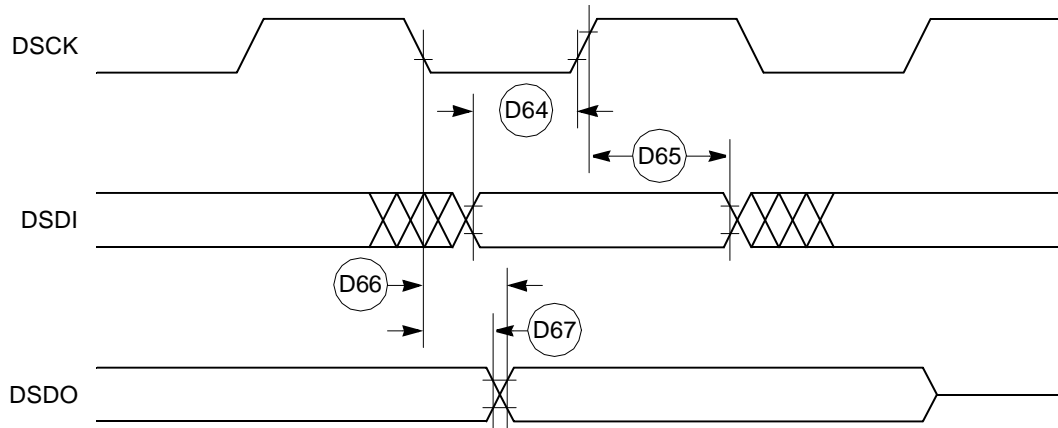


Figure 33. Debug Port Timings

13 CPM Electrical Characteristics

This section provides the AC and DC electrical specifications for the communications processor module (CPM) of the MPC875/MPC870.

13.1 Port C Interrupt AC Electrical Specifications

Table 17 provides the timings for Port C interrupts.

Table 17. Port C Interrupt Timing

Num	Characteristic	33.34 MHz		Unit
		Min	Max	
35	Port C interrupt pulse width low (edge-triggered mode)	55	—	ns
36	Port C interrupt minimum time between active edges	55	—	ns

Figure 41 shows the Port C interrupt detection timing.

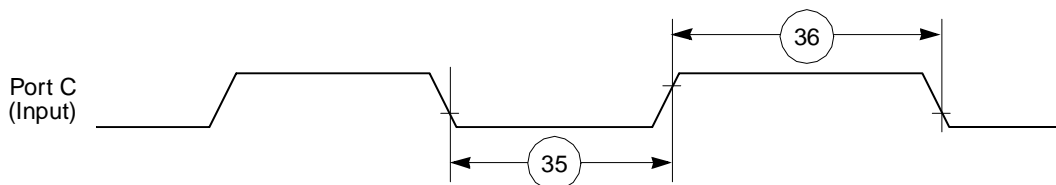


Figure 41. Port C Interrupt Detection Timing

13.2 IDMA Controller AC Electrical Specifications

Table 18 provides the IDMA controller timings as shown in Figure 42 through Figure 45.

Table 18. IDMA Controller Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
40	\overline{DREQ} setup time to clock high	7	—	ns
41	\overline{DREQ} hold time from clock high ¹	TBD	—	ns
42	\overline{SDACK} assertion delay from clock high	—	12	ns
43	\overline{SDACK} negation delay from clock low	—	12	ns
44	\overline{SDACK} negation delay from \overline{TA} low	—	20	ns
45	\overline{SDACK} negation delay from clock high	—	15	ns
46	\overline{TA} assertion to rising edge of the clock setup time (applies to external \overline{TA})	7	—	ns

¹ Applies to high-to-low mode (EDM = 1).

13.3 Baud Rate Generator AC Electrical Specifications

Table 19 provides the baud rate generator timings as shown in Figure 46.

Table 19. Baud Rate Generator Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
50	BRGO rise and fall time	—	10	ns
51	BRGO duty cycle	40	60	%
52	BRGO cycle	40	—	ns

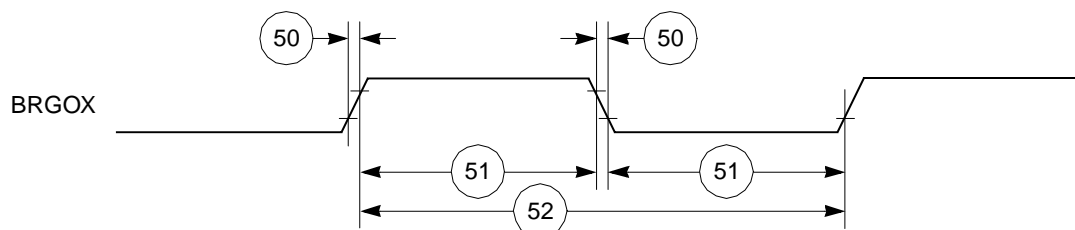


Figure 46. Baud Rate Generator Timing Diagram

13.4 Timer AC Electrical Specifications

Table 20 provides the general-purpose timer timings as shown in Figure 47.

Table 20. Timer Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
61	TIN/ $\overline{\text{TGATE}}$ rise and fall time	10	—	ns
62	TIN/ $\overline{\text{TGATE}}$ low time	1	—	clk
63	TIN/ $\overline{\text{TGATE}}$ high time	2	—	clk
64	TIN/ $\overline{\text{TGATE}}$ cycle time	3	—	clk
65	CLKO low to $\overline{\text{TOUT}}$ valid	3	25	ns

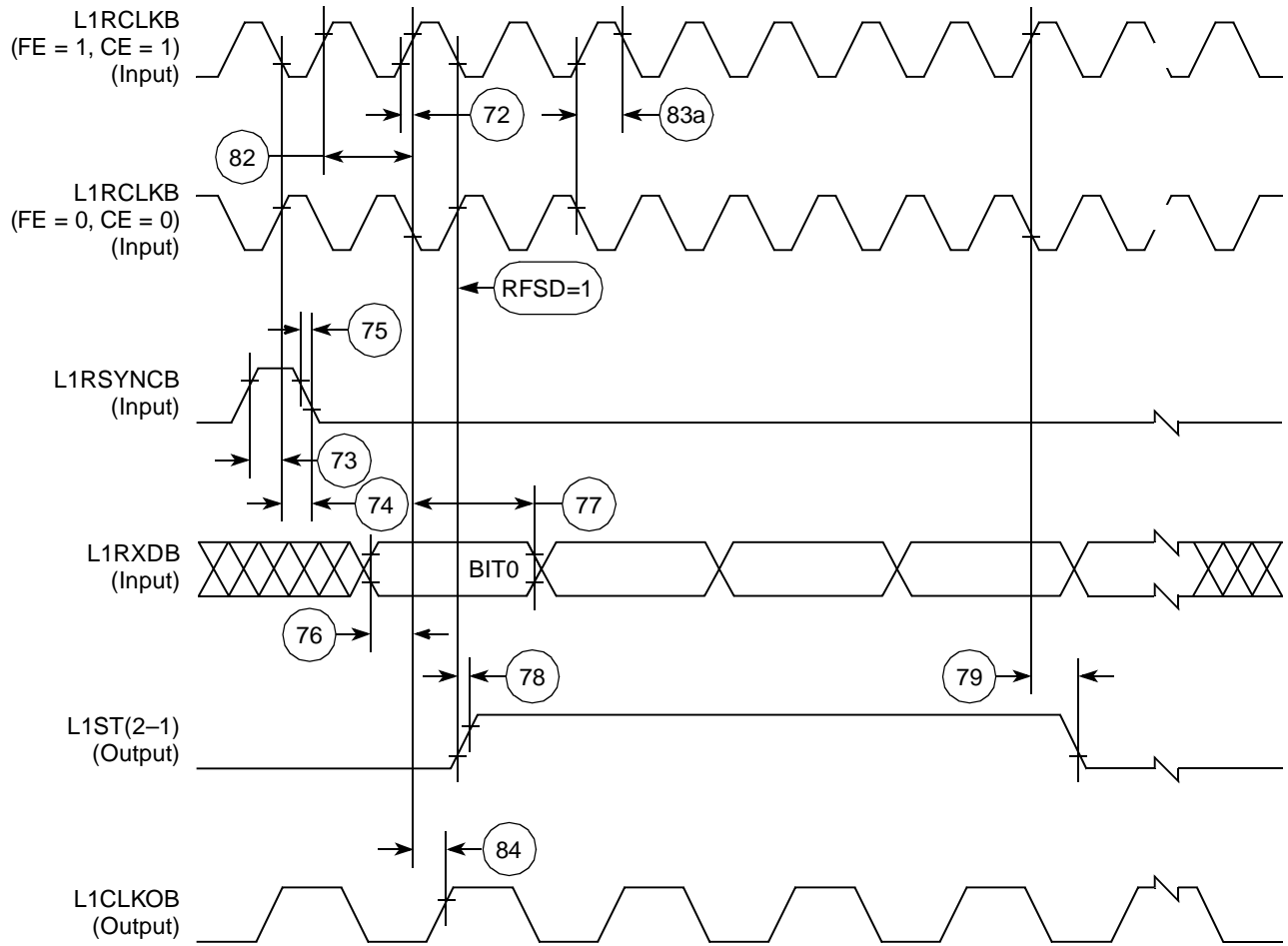


Figure 49. SI Receive Timing with Double-Speed Clocking (DSC = 1)

13.6 SCC in NMSI Mode Electrical Specifications

Table 22 provides the NMSI external clock timing.

Table 22. NMSI External Clock Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
100	RCLK3 and TCLK3 width high ¹	1/SYNCCLK	—	ns
101	RCLK3 and TCLK3 width low	1/SYNCCLK + 5	—	ns
102	RCLK3 and TCLK3 rise/fall time	—	15.00	ns
103	TXD3 active delay (from TCLK3 falling edge)	0.00	50.00	ns
104	$\overline{\text{RTS3}}$ active/inactive delay (from TCLK3 falling edge)	0.00	50.00	ns
105	$\overline{\text{CTS3}}$ setup time to TCLK3 rising edge	5.00	—	ns
106	RXD3 setup time to RCLK3 rising edge	5.00	—	ns
107	RXD3 hold time from RCLK3 rising edge ²	5.00	—	ns
108	$\overline{\text{CD3}}$ setup time to RCLK3 rising edge	5.00	—	ns

¹ The ratios SYNCCLK/RCLK3 and SYNCCLK/TCLK3 must be greater than or equal to 2.25/1.

² Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as external SYNC signals.

Table 23 provides the NMSI internal clock timing.

Table 23. NMSI Internal Clock Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
100	RCLK3 and TCLK3 frequency ¹	0.00	SYNCCLK/3	MHz
102	RCLK3 and TCLK3 rise/fall time	—	—	ns
103	TXD3 active delay (from TCLK3 falling edge)	0.00	30.00	ns
104	$\overline{\text{RTS3}}$ active/inactive delay (from TCLK3 falling edge)	0.00	30.00	ns
105	$\overline{\text{CTS3}}$ setup time to TCLK3 rising edge	40.00	—	ns
106	RXD3 setup time to RCLK3 rising edge	40.00	—	ns
107	RXD3 hold time from RCLK3 rising edge ²	0.00	—	ns
108	$\overline{\text{CD3}}$ setup time to RCLK3 rising edge	40.00	—	ns

¹ The ratios SYNCCLK/RCLK3 and SYNCCLK/TCLK3 must be greater or equal to 3/1.

² Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as external SYNC signals.

Table 24. Ethernet Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
138	CLKO1 low to $\overline{\text{SDACK}}$ asserted ²	—	20	ns
139	CLKO1 low to $\overline{\text{SDACK}}$ negated ²	—	20	ns

¹ The ratios SYNCCLK/RCLK3 and SYNCCLK/TCLK3 must be greater than or equal to 2/1.

² $\overline{\text{SDACK}}$ is asserted whenever the SDMA writes the incoming frame DA into memory.

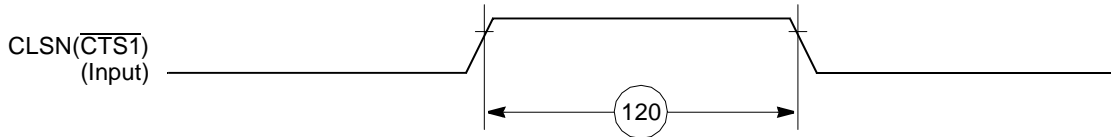


Figure 56. Ethernet Collision Timing Diagram

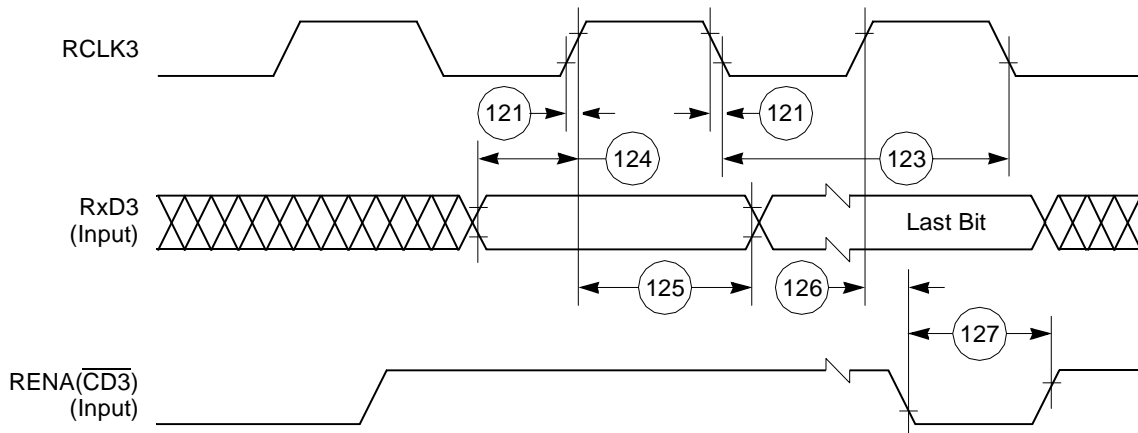
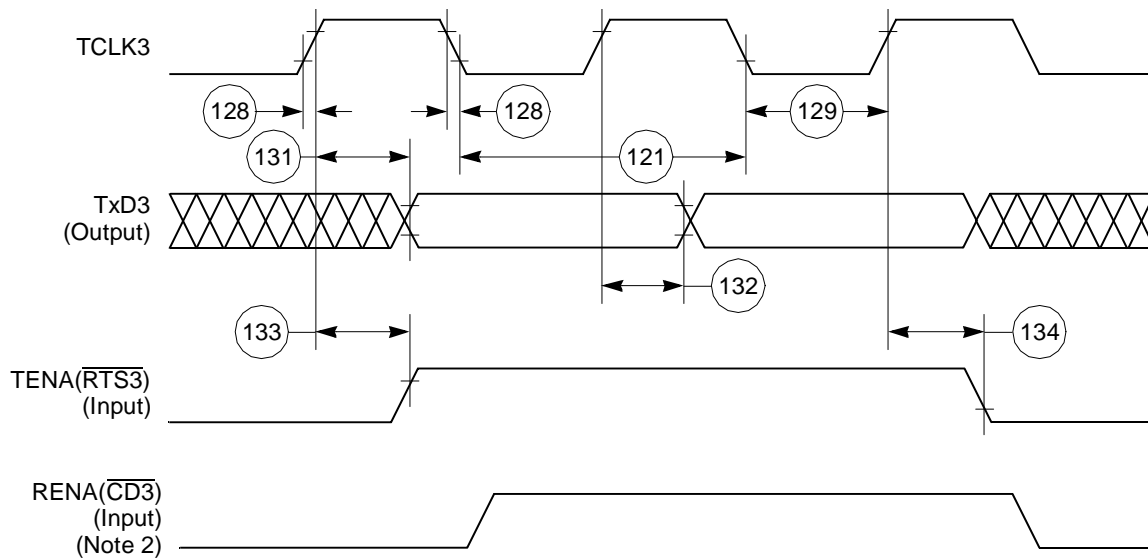


Figure 57. Ethernet Receive Timing Diagram



Notes:

1. Transmit clock invert (TCI) bit in GSMR is set.
2. If RENA is negated before TENA or RENA is not asserted at all during transmit, then the CSL bit is set in the buffer descriptor at the end of the frame transmission.

Figure 58. Ethernet Transmit Timing Diagram

13.8 SMC Transparent AC Electrical Specifications

Table 25 provides the SMC transparent timings as shown in Figure 59.

Table 25. SMC Transparent Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
150	SMCLK clock period ¹	100	—	ns
151	SMCLK width low	50	—	ns
151A	SMCLK width high	50	—	ns
152	SMCLK rise/fall time	—	15	ns
153	SMTXD active delay (from SMCLK falling edge)	10	50	ns
154	SMRXD/SMSYNC setup time	20	—	ns
155	RXD1/SMSYNC hold time	5	—	ns

¹ SYNCCLK must be at least twice as fast as SMCLK.

16 Mechanical Data and Ordering Information

Table 35 identifies the packages and operating frequencies available for the MPC875/MPC870.

Table 35. Available MPC875/MPC870 Packages/Frequencies

Package Type	Temperature (T _J)	Frequency (MHz)	Order Number
Plastic ball grid array ZT suffix—Leaded VR suffix—Lead-Free are available as needed	0°C to 95°C	66	KMPC875ZT66 KMPC870ZT66 MPC875ZT66 MPC870ZT66
		80	KMPC875ZT80 KMPC870ZT80 MPC875ZT80 MPC870ZT80
		133	KMPC875ZT133 KMPC870ZT133 MPC875ZT133 MPC870ZT133
Plastic ball grid array CZT suffix—Leaded CVR suffix—Lead-Free are available as needed	-40°C to 100°C	66	KMPC875CZT66 KMPC870CZT66 MPC875CZT66 MPC870CZT66
		133	KMPC875CZT133 KMPC870CZT133 MPC875CZT133 MPC870CZT133

Table 36. Pin Assignments—JEDEC Standard (continued)

Name	Pin Number	Type
PB30, SPICLK	T17	Bidirectional (Optional: open-drain) (5-V tolerant)
PB29, SPI MOSI	R17	Bidirectional (Optional: open-drain) (5-V tolerant)
PB28, SPIMISO, BRGO4	R14	Bidirectional (Optional: open-drain) (5-V tolerant)
PB27, I2CSDA, BRGO1	N13	Bidirectional (Optional: open-drain)
PB26, I2CSCL, BRGO2	N12	Bidirectional (Optional: open-drain)
PB25, SMTXD1	U13	Bidirectional (Optional: open-drain) (5-V tolerant)
PB24, SMRXD1	T12	Bidirectional (Optional: open-drain) (5-V tolerant)
PB23, $\overline{\text{SDACK1}}$, $\overline{\text{SMSYN1}}$	U12	Bidirectional (Optional: open-drain)
PB19, MII1-RXD3, RTS4	T11	Bidirectional (Optional: open-drain)
PC15, $\overline{\text{DREQ0}}$, L1ST1	R15	Bidirectional (5-V tolerant)
PC13, MII1-TXD3, $\overline{\text{SDACK1}}$	U9	Bidirectional (5-V tolerant)
PC12, MII1-TXD2, TOUT1	T15	Bidirectional (5-V tolerant)
PC11, USBRXP	P12	Bidirectional
PC10, USBRXN, $\overline{\text{TGATE1}}$	U11	Bidirectional
PC7, $\overline{\text{CTS4}}$, L1TSYN CB, USBTXP	T10	Bidirectional (5-V tolerant)
PC6, $\overline{\text{CD4}}$, L1RSYN CB, USBTXN	P10	Bidirectional (5-V tolerant)
PD8, RXD4, MII-MDC, RMII-MDC	T3	Bidirectional (5-V tolerant)
PE31, CLK8, L1TCLKB, MII1-RXCLK	P9	Bidirectional (Optional: open-drain)
PE30, L1RXDB, MII1-RXD2	R8	Bidirectional (Optional: open-drain)

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