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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

E·XF

Product Status	Active
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	66MHz
Co-Processors/DSP	Communications; CPM, Security; SEC
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (1), 10/100Mbps (2)
SATA	·
USB	USB 2.0 (1)
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TA)
Security Features	Cryptography
Package / Case	256-BBGA
Supplier Device Package	256-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc875zt66

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong





The MPC875 block diagram is shown in Figure 1.

Figure 1. MPC875 Block Diagram





3 Maximum Tolerated Ratings

This section provides the maximum tolerated voltage and temperature ranges for the MPC875/MPC870. Table 2 displays the maximum tolerated ratings and Table 3 displays the operating temperatures.

Rating	Symbol	Value	Unit
Supply voltage ¹	V _{DDL} (core voltage)	-0.3 to 3.4	V
	V _{DDH} (I/O voltage)	–0.3 to 4	V
	V _{DDSYN}	-0.3 to 3.4	V
	Difference between V_{DDL} and V_{DDSYN}	<100	mV
Input voltage ²	V _{in}	$GND-0.3$ to V_{DDH}	V
Storage temperature range	T _{stg}	-55 to +150	°C

Table 2. Maximum Tolerated Ratings

¹ The power supply of the device must start its ramp from 0.0 V.

² Functional operating conditions are provided with the DC electrical specifications in Table 6. Absolute maximum ratings are stress ratings only; functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.

Caution: All inputs that tolerate 5 V cannot be more than 2.5 V greater than V_{DDH}. This restriction applies to power up and normal operation (that is, if the MPC875/MPC870 is unpowered, a voltage greater than 2.5 V must not be applied to its inputs).

Figure 3 shows the undershoot and overshoot voltages at the interfaces of the MPC875/MPC870.



Figure 3. Undershoot/Overshoot Voltage for V_{DDH} and V_{DDL}

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Bus Signal Timing

Num	Characteristic	33	MHz	40 MHz		66 MHz		80 MHz		L Ins it
NUM	Characteristic	Min	Max	Min	Max	Min	Мах	Min	Max	Unit
B30d	$\overline{WE}(0:3)/BS_B[0:3]$ negated to A(0:31), BADDR(28:30) invalid GPCM write access TRLX = 1, CSNT =1, \overline{CS} negated to A(0:31) invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10 or 11, EBDF = 1	38.67	_	31.38		17.83		14.19	_	ns
B31	CLKOUT falling edge to \overline{CS} valid as requested by control bit CST4 in the corresponding word in the UPM (MAX = $0.00 \times B1 + 6.00$)	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B31a	CLKOUT falling edge to \overline{CS} valid as requested by control bit CST1 in the corresponding word in the UPM (MAX = $0.25 \times B1 + 6.80$)	7.60	14.30	6.30	13.00	3.80	10.50	3.13	10.00	ns
B31b	CLKOUT rising edge to \overline{CS} valid, as requested by control bit CST2 in the corresponding word in the UPM (MAX = $0.00 \times B1 + 8.00$)	1.50	8.00	1.50	8.00	1.50	8.00	1.50	8.00	ns
B31c	CLKOUT rising edge to \overline{CS} valid, as requested by control bit CST3 in the corresponding word in the UPM (MAX = $0.25 \times B1 + 6.30$)	7.60	13.80	6.30	12.50	3.80	10.00	3.13	9.40	ns
B31d	CLKOUT falling edge to \overline{CS} valid as requested by control bit CST1 in the corresponding word in the UPM EBDF = 1 (MAX = 0.375 × B1 + 6.6)	13.30	18.00	11.30	16.00	7.60	12.30	4.69	11.30	ns
B32	CLKOUT falling edge to $\overline{\text{BS}}$ valid as requested by control bit BST4 in the corresponding word in the UPM (MAX = $0.00 \times \text{B1} + 6.00$)	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B32a	CLKOUT falling edge to \overline{BS} valid as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 0 (MAX = 0.25 × B1 + 6.80)	7.60	14.30	6.30	13.00	3.80	10.50	3.13	10.00	ns
B32b	CLKOUT rising edge to $\overline{\text{BS}}$ valid, as requested by control bit BST2 in the corresponding word in the UPM (MAX = $0.00 \times \text{B1} + 8.00$)	1.50	8.00	1.50	8.00	1.50	8.00	1.50	8.00	ns
B32c	CLKOUT rising edge to $\overline{\text{BS}}$ valid, as requested by control bit BST3 in the corresponding word in the UPM (MAX = $0.25 \times B1 + 6.80$)	7.60	14.30	6.30	13.00	3.80	10.50	3.13	10.00	ns
B32d	CLKOUT falling edge to $\overline{\text{BS}}$ valid as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 1 (MAX = 0.375 × B1 + 6.60)	13.30	18.00	11.30	16.00	7.60	12.30	4.49	11.30	ns
B33	CLKOUT falling edge to $\overline{\text{GPL}}$ valid as requested by control bit GxT4 in the corresponding word in the UPM (MAX = $0.00 \times \text{B1} + 6.00$)	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns

Table 10. Bus Operation Timings (continued)



		33	MHz	40	MHz	66 I	MHz	80 1	٧Hz	
Num	Characteristic	Min	Max	Min	Max	Min	Max	Min	Max	Unit
B33a	CLKOUT rising edge to $\overline{\text{GPL}}$ valid as requested by control bit GxT3 in the corresponding word in the UPM (MAX = $0.25 \times B1 + 6.80$)	7.60	14.30	6.30	13.00	3.80	10.50	3.13	10.00	ns
B34	A(0:31), BADDR(28:30), and D(0:31) to \overline{CS} valid, as requested by control bit CST4 in the corresponding word in the UPM (MIN = 0.25 × B1 - 2.00)		_	4.30	_	1.80	_	1.13	_	ns
B34a	A(0:31), BADDR(28:30), and D(0:31) to \overline{CS} valid, as requested by control bit CST1 in the corresponding word in the UPM (MIN = 0.50 × B1 - 2.00)	13.20	_	10.50	_	5.60	_	4.25	_	ns
B34b	A(0:31), BADDR(28:30), and D(0:31) to \overline{CS} valid, as requested by CST2 in the corresponding word in UPM (MIN = 0.75 × B1 – 2.00)	20.70	_	16.70	_	9.40	_	6.80	_	ns
B35	A(0:31), BADDR(28:30) to \overline{CS} valid as requested by control bit BST4 in the corresponding word in the UPM (MIN = $0.25 \times B1 - 2.00$)	5.60	_	4.30	_	1.80	_	1.13	_	ns
B35a	A(0:31), BADDR(28:30), and D(0:31) to $\overline{\text{BS}}$ valid as requested by BST1 in the corresponding word in the UPM (MIN = 0.50 × B1 - 2.00)	13.20	_	10.50	_	5.60	_	4.25	_	ns
B35b	A(0:31), BADDR(28:30), and D(0:31) to $\overline{\text{BS}}$ valid as requested by control bit BST2 in the corresponding word in the UPM (MIN = 0.75 × B1 - 2.00)	20.70	_	16.70	_	9.40	_	7.40	_	ns
B36	A(0:31), BADDR(28:30), and D(0:31) to $\overline{\text{GPL}}$ valid as requested by control bit GxT4 in the corresponding word in the UPM (MIN = $0.25 \times B1 - 2.00$)	5.60	_	4.30	_	1.80	_	1.13	_	ns
B37	UPWAIT valid to CLKOUT falling edge ⁹ (MIN = $0.00 \times B1 + 6.00$)	6.00	—	6.00	—	6.00	_	6.00	_	ns
B38	CLKOUT falling edge to UPWAIT valid ⁹ (MIN = $0.00 \times B1 + 1.00$)	1.00	—	1.00	—	1.00	—	1.00	_	ns
B39	$\overline{\text{AS}}$ valid to CLKOUT rising edge ¹⁰ (MIN = 0.00 × B1 + 7.00)	7.00	—	7.00	—	7.00	—	7.00	_	ns
B40	A(0:31), TSIZ(0:1), RD/WR, BURST valid to CLKOUT rising edge (MIN = 0.00 × B1 + 7.00)	7.00	—	7.00		7.00	—	7.00	—	ns
B41	$\overline{\text{TS}}$ valid to CLKOUT rising edge (setup time) (MIN = 0.00 × B1 + 7.00)	7.00	—	7.00		7.00		7.00	—	ns

Table 10. Bus Operation Timings (continued)

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Figure 5 provides the control timing diagram.



Figure 6 provides the timing for the external clock.



Figure 6. External Clock Timing

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Figure 9 provides the timing for the synchronous input signals.



Figure 10 provides normal case timing for input data. It also applies to normal read accesses under the control of the user-programmable machine (UPM) in the memory controller.



Figure 10. Input Data Timing in Normal Case



Bus Signal Timing

Figure 11 provides the timing for the input data controlled by the UPM for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)



Figure 11. Input Data Timing when Controlled by UPM in the Memory Controller and DLT3 = 1

Figure 12 through Figure 15 provide the timing for the external bus read controlled by various GPCM factors.



Figure 12. External Bus Read Timing (GPCM Controlled—ACS = 00)

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Figure 14. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 11)

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Figure 18. External Bus Write Timing (GPCM Controlled—TRLX = 1, CSNT = 1)



Bus Signal Timing



Figure 22 provides the timing for the synchronous external master access controlled by the GPCM.

Figure 22. Synchronous External Master Access Timing (GPCM Handled ACS = 00)

Figure 23 provides the timing for the asynchronous external master memory access controlled by the GPCM.





Figure 24 provides the timing for the asynchronous external master control signals negation.



Figure 24. Asynchronous External Master—Control Signals Negation Timing



Table 15 shows the reset timing for the MPC875/MPC870.

Table 15. Reset Timing

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
Nulli			Max	Min	Max	Min	Max	Min	Max	Unit
R69	CLKOUT to $\overline{\text{HRESET}}$ high impedance (MAX = 0.00 × B1 + 20.00)	—	20.00	—	20.00	_	20.00	_	20.00	ns
R70	CLKOUT to $\overline{\text{SRESET}}$ high impedance (MAX = 0.00 × B1 + 20.00)		20.00	—	20.00		20.00		20.00	ns
R71	RSTCONF pulse width (MIN = 17.00 × B1)	515.20	—	425.00	_	257.60	_	212.50	_	ns
R72	_	—		—		—		—		—
R73	Configuration data to $\overline{\text{HRESET}}$ rising edge setup time (MIN = 15.00 × B1 + 50.00)	504.50	—	425.00	_	277.30	_	237.50	—	ns
R74	Configuration data to $\overrightarrow{\text{RSTCONF}}$ rising edge setup time (MIN = 0.00 × B1 + 350.00)	350.00	_	350.00		350.00	_	350.00	_	ns
R75	Configuration data hold time after $\overrightarrow{\text{RSTCONF}}$ negation (MIN = 0.00 × B1 + 0.00)	0.00	—	0.00	_	0.00	_	0.00	_	ns
R76	Configuration data hold time after HRESET negation (MIN = $0.00 \times B1 + 0.00$)	0.00	—	0.00	_	0.00	_	0.00	—	ns
R77	HRESET and RSTCONF asserted todata out drive(MAX = $0.00 \times B1 + 25.00$)	—	25.00	—	25.00	—	25.00	—	25.00	ns
R78	$\frac{RSTCONF}{Impedance} \text{ negated to data out high}$	—	25.00	_	25.00	_	25.00	_	25.00	ns
R79	CLKOUT of last rising edge before chip three-states $\overrightarrow{\text{HRESET}}$ to data out high impedance (MAX = 0.00 × B1 + 25.00)	—	25.00	—	25.00	—	25.00	—	25.00	ns
R80	DSDI, DSCK setup (MIN = $3.00 \times B1$)	90.90		75.00		45.50		37.50		ns
R81	DSDI, DSCK hold time (MIN = $0.00 \times B1 + 0.00$)	0.00	—	0.00	_	0.00	_	0.00	_	ns
R82	$\begin{tabular}{l} \hline $SRESET$ negated to CLKOUT rising edge for DSDI and DSCK sample (MIN = 8.00 imes B1)$	242.40		200.00	_	121.20	_	100.00	_	ns



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Table 16 provides the JTAG timings for the MPC875/MPC870 shown in Figure 37 through Figure 40.

Table 16. JTAG Timing

Num	Characteristic	All Freq	uencies	Unit	
Num	Characteristic	Min	Мах	Unit	
J82	TCK cycle time	100.00	—	ns	
J83	TCK clock pulse width measured at 1.5 V	40.00	—	ns	
J84	TCK rise and fall times	0.00	10.00	ns	
J85	TMS, TDI data setup time	5.00	—	ns	
J86	TMS, TDI data hold time	25.00	—	ns	
J87	TCK low to TDO data valid	—	27.00	ns	
J88	TCK low to TDO data invalid	0.00	_	ns	
J89	TCK low to TDO high impedance	—	20.00	ns	
J90	TRST assert time	100.00	—	ns	
J91	TRST setup time to TCK low	40.00	_	ns	
J92	TCK falling edge to output valid	—	50.00	ns	
J93	TCK falling edge to output valid out of high impedance	—	50.00	ns	
J94	TCK falling edge to output high impedance	—	50.00	ns	
J95	Boundary scan input valid to TCK rising edge	50.00	—	ns	
J96	TCK rising edge to boundary scan input invalid	50.00	_	ns	



Figure 37. JTAG Test Clock Input Timing



CPM Electrical Characteristics





CPM Electrical Characteristics

Num	Characteristic	All Freq	Unit	
Num	Undracteristic			Max
138	CLKO1 low to SDACK asserted ²	_	20	ns
139	CLKO1 low to SDACK negated ²		20	ns

Table 24. Ethernet Timing (continued)

¹ The ratios SYNCCLK/RCLK3 and SYNCCLK/TCLK3 must be greater than or equal to 2/1.

² SDACK is asserted whenever the SDMA writes the incoming frame DA into memory.



Figure 56. Ethernet Collision Timing Diagram



Figure 57. Ethernet Receive Timing Diagram



CPM Electrical Characteristics

Num	Characteristic	All Freq	Unit	
	Unaracteristic			Мах
210	SDL/SCL fall time	—	300	ns
211	Stop condition setup time	4.7	—	μs

Table 28. I²C Timing (SCL < 100 kHz) (continued)

SCL frequency is given by SCL = BRGCLK_frequency/((BRG register + 3) × pre_scalar × 2). The ratio SYNCCLK/(BRGCLK/pre_scalar) must be greater than or equal to 4/1.

Table 29 provides the I^2C (SCL > 100 kHz) timings.

lable 29.	. I ² C	Timing	(SCL	>	100	kHz))
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Num	Characteristic	Everencien	All Freq	Unit	
Num	Characteristic	Expression	Min	Мах	Unit
200	SCL clock frequency (slave)	fSCL	0	BRGCLK/48	Hz
200	SCL clock frequency (master) ¹	fSCL	BRGCLK/16512	BRGCLK/48	Hz
202	Bus free time between transmissions	—	1/(2.2 × fSCL)	_	S
203	Low period of SCL	—	1/(2.2 × fSCL)	_	S
204	High period of SCL	—	1/(2.2 × fSCL)	_	S
205	Start condition setup time	—	1/(2.2 × fSCL)	_	S
206	Start condition hold time	_	1/(2.2 × fSCL)	_	S
207	Data hold time	—	0	_	S
208	Data setup time	—	1/(40 × fSCL)	_	S
209	SDL/SCL rise time	—	—	1/(10 × fSCL)	S
210	SDL/SCL fall time	—	—	$1/(33 \times \text{fSCL})$	S
211	Stop condition setup time	—	$1/2(2.2 \times \text{fSCL})$	_	S

SCL frequency is given by SCL = BRGCLK_frequency/((BRG register + 3) × pre_scalar × 2). The ratio SYNCCLK/(BRGCLK/pre_scalar) must be greater than or equal to 4/1.

Figure 64 shows the I^2C bus timing.





Figure 66 shows the MII transmit signal timing diagram.



Figure 66. MII Transmit Signal Timing Diagram

15.3 MII Async Inputs Signal Timing (MII_CRS, MII_COL)

Table 33 provides information on the MII async inputs signal timing.

Table 33. MII Async Inputs Signal Timing

Num	Characteristic	Min	Max	Unit
M9	MII_CRS, MII_COL minimum pulse width	1.5		MII_TX_CLK period

Figure 67 shows the MII asynchronous inputs signal timing diagram.



Figure 67. MII Async Inputs Timing Diagram

15.4 MII Serial Management Channel Timing (MII_MDIO, MII_MDC)

Table 34 provides information on the MII serial management channel signal timing. The FEC functions correctly with a maximum MDC frequency in excess of 2.5 MHz.

Table 34.	MII	Serial	Management	Channel	Timing
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Num	Characteristic	Min	Мах	Unit
M10	MII_MDC falling edge to MII_MDIO output invalid (minimum propagation delay)	0	_	ns
M11	MII_MDC falling edge to MII_MDIO output valid (max prop delay)		25	ns
M12	MII_MDIO (input) to MII_MDC rising edge setup	10	—	ns
M13	MII_MDIO (input) to MII_MDC rising edge hold	0	—	ns
M14	MII_MDC pulse width high	40%	60%	MII_MDC period
M15	MII_MDC pulse width low	40%	60%	MII_MDC period

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Table 36 contains a list of the MPC875/MPC870 input and output signals and shows multiplexing and pin assignments.

Name	Pin Number	Туре
A[0:31]	R16, N14, M14, P15, P17, P16, N15, N16, M15, N17, L14, M16, L15, M17, K14, L16, L17, K17, G17, K15, J16, J15, G16, J14, H17, H16, G15, K16, H14, J17, H15, F17	Bidirectional Three-state (3.3 V only)
TSIZ0, REG	F16	Bidirectional Three-state (3.3 V only)
TSIZ1	G14	Bidirectional Three-state (3.3 V only)
RD/WR	D13	Bidirectional Three-state (3.3 V only)
BURST	B9	Bidirectional Three-state (3.3 V only)
BDIP, GPL_B5	C13	Output
TS	C11	Bidirectional Active pull-up (3.3 V only)
TA	C12	Bidirectional Active pull-up (3.3 V only)
TEA	B12	Open-drain
BI	B13	Bidirectional Active pull-up (3.3 V only)
IRQ2, RSV	C9	Bidirectional Three-state (3.3 V only)
ĪRQ4, KR, RETRY, SPKROUT	E9	Bidirectional Three-state (3.3 V only)
D[0:31]	L5, N3, L3, L2, R2, K2, H3, G2, R3, M3, N2, M2, M4, N4, K5, K3, K4, P3, J2, J3, J4, J5, H2, P2, H4, H5, G5, L4, G3, F2, F3, E2	Bidirectional Three-state (3.3 V only)
CR, IRQ3	E10	Input
FRZ, IRQ6	B10	Bidirectional Three-state (3.3 V only)
BR	B11	Bidirectional (3.3 V only)
BG	D10	Bidirectional (3.3 V only)
BB	C10	Bidirectional Active pull-up (3.3 V only)
IRQ0	M6	Input (3.3 V only)
IRQ1	P5	Input (3.3 V only)
IRQ7	N5	Input (3.3 V only)
CS[0:5]	B14, E11, C14, B15, E13, B16	Output

Table 36. Pin Assignments—JEDEC Standard



Name	Pin Number	Туре
TDO, DSDO	P13	Output (5-V tolerant)
MII1_CRS	U10	Input
MII_MDIO	M13	Bidirectional (5-V tolerant)
MII1_TX_EN, RMII1_TX_EN	U5	Output (5-V tolerant)
MII1_COL	R10	Input
V _{SSSYN}	E5	PLL analog GND
V _{SSSYN1}	F6	PLL analog GND
V _{DDSYN}	E6	PLL analog V _{DD}
GND	H8, H9, H10, H11, J8, J9, J10, J11, K8, K9, K10, K11, L8, L9, L10, L11, U15	Power
V _{DDL}	F7, F8, F9, F10, F11, H6, H13, J6, J13, K6, K13, L6, L13, N7, N8, N9, N10, N11	Power
V _{DDH}	G7, G8, G9, G10, G11, G12, H7, H12, J7, J12, K7, K12, L7, L12, M7, M8, M9, M10, M11, M12	Power
N/C	B17, T16, U2, U17	No connect

Table 36. Pin Assignments—JEDEC Standard (continued)



Document Revision History

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