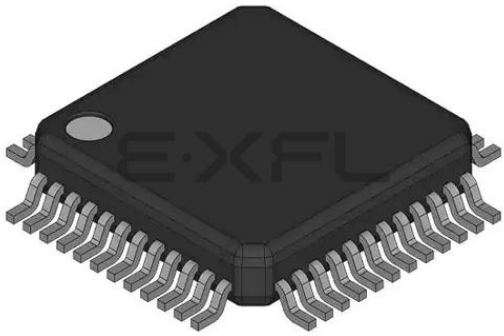
Cypress Semiconductor Corp - MB9AF132KBPMC-G-SNE2 Datasheet



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What is "Embedded - Microcontrollers"?

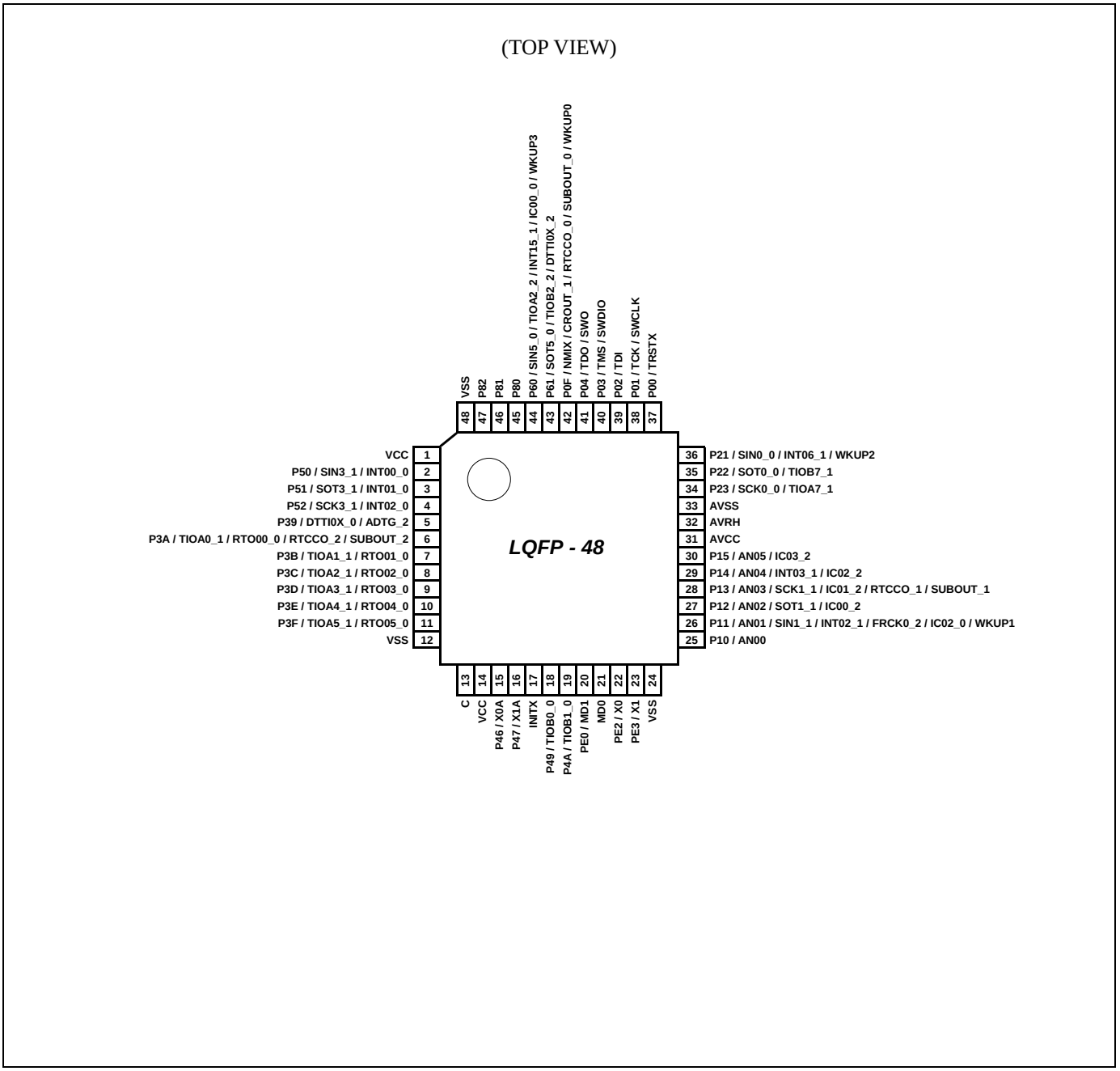
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	20MHz
Connectivity	CSIO, I²C, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	37
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 6x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/rochester-electronics/mb9af132kbpmc-g-sne2

3. Pin Assignment

FPT-48P-M49



Note:

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin No		Pin name	I/O circuit type	Pin state type
LQFP-64 QFN-64	LQFP-48 QFN-48			
25	-	P4C	E	H
		TIOB3_0		
		SCK7_1 (SCL7_1)		
26	-	P4D	E	H
		TIOB4_0		
		SOT7_1 (SDA7_1)		
27	-	P4E	E	F
		TIOB5_0		
		INT06_2		
		SIN7_1		
28	20	PE0	C	P
		MD1		
29	21	MD0	H	D
30	22	PE2	A	A
		X0		
31	23	PE3	A	B
		X1		
32	24	VSS	-	
33	-	VCC	-	
34	25	P10	F	J
		AN00		
35	26	P11	F	L
		AN01		
		SIN1_1		
		INT02_1		
		FRCK0_2		
		IC02_0		
		WKUP1		
36	27	P12	F	J
		AN02		
		SOT1_1 (SDA1_1)		
		IC00_2		
37	28	P13	F	J
		AN03		
		SCK1_1 (SCL1_1)		
		IC01_2		
		RTCCO_1		
		SUBOUT_1		

Pin function	Pin name	Function description	Pin No	
			LQFP-64 QFN-64	LQFP-48 QFN-48
GPIO	P30	General-purpose I/O port 3	5	-
	P31		6	-
	P32		7	-
	P33		8	-
	P39		9	5
	P3A		10	6
	P3B		11	7
	P3C		12	8
	P3D		13	9
	P3E		14	10
	P3F		15	11
	P46	General-purpose I/O port 4	19	15
	P47		20	16
	P49		22	18
	P4A		23	19
	P4B		24	-
	P4C		25	-
	P4D		26	-
	P4E		27	-
	P50	General-purpose I/O port 5	2	2
	P51		3	3
	P52		4	4
	P60	General-purpose I/O port 6	60	44
	P61		59	43
	P62		58	-
	P80	General-purpose I/O port 8	61	45
	P81		62	46
	P82		63	47
	PE0	General-purpose I/O port E	28	20
	PE2		30	22
	PE3		31	23

7. Handling Devices

Power supply pins

In products with multiple VCC and VSS pins, respective pins at the same potential are interconnected within the device in order to prevent malfunctions such as latch-up. However, all of these pins should be connected externally to the power supply or ground lines in order to reduce electromagnetic emission levels, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with each Power supply pins and GND pins of this device at low impedance. It is also advisable that a ceramic capacitor of approximately 0.1 µF be connected as a bypass capacitor between each Power supply pins and GND pins, between AVCC pin and AVSS pin near this device.

Stabilizing power supply voltage

A malfunction may occur when the power supply voltage fluctuates rapidly even though the fluctuation is within the recommended operating conditions of the VCC power supply voltage. As a rule, with voltage stabilization, suppress the voltage fluctuation so that the fluctuation in VCC ripple (peak-to-peak value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the VCC value in the recommended operating conditions, and the transient fluctuation rate does not exceed 0.1 V/µs when there is a momentary fluctuation on switching the power supply.

Crystal oscillator circuit

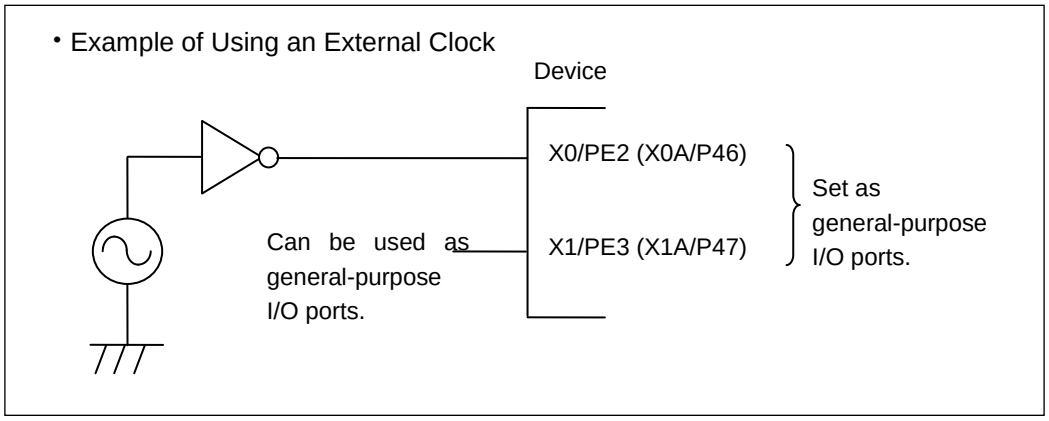
Noise near the X0/X1 and X0A/X1A pins may cause the device to malfunction. Design the printed circuit board so that X0/X1, X0A/X1A pins, the crystal oscillator, and the bypass capacitor to ground are located as close to the device as possible.

It is strongly recommended that the PC board artwork be designed such that the X0/X1 and X0A/X1A pins are surrounded by ground plane as this is expected to produce stable operation.

Evaluate oscillation of your using crystal oscillator by your mount board.

Using an external clock

To use the external clock, set general-purpose I/O ports to input the clock to X0/PE2 and X0A/P46 pins.



Handling when using Multi-function serial pin as I^2C pin

If it is using the Multi-function serial pin as I^2C pins, P-ch transistor of digital output is always disable. However, I^2C pins need to keep the electrical characteristic like other pins and not to connect to external I^2C bus system with power OFF.

11. Pin Status in Each CPU State

The terms used for pin status have the following meanings.

- INITX = 0

  This is the period when the INITX pin is the L level.

- INITX = 1

  This is the period when the INITX pin is the H level.

- SPL = 0

  This is the status that standby pin level setting bit (SPL) in standby mode control register (STB_CTL) is set to 0.

- SPL = 1

  This is the status that standby pin level setting bit (SPL) in standby mode control register (STB_CTL) is set to 1.

- Input enabled

  Indicates that the input function can be used.

- Internal input fixed at 0

  This is the status that the input function cannot be used. Internal input is fixed at L.

- Hi-Z

  Indicates that the pin drive transistor is disabled and the pin is put in the Hi-Z state.

- Setting disabled

  Indicates that the setting is disabled.

- Maintain previous state

  Maintains the state that was immediately prior to entering the current mode.
  If a built-in peripheral function is operating, the output follows the peripheral function.
  If the pin is being used as a port, that output is maintained.

- Analog input is enabled

  Indicates that the analog input is enabled.

- Trace output

  Indicates that the trace function can be used.

- GPIO selected

  In Deep Standby mode, pins switch to the general-purpose I/O port.

Pin status type	Function group	Power-on reset or low voltage detection state	INITX input state	Device internal reset state	Run mode or Sleep mode state	Timer mode, RTC mode, or Stop mode state		Deep Standby RTC mode or Deep Standby Stop mode state		Return from Deep Standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
L	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled
	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected
	External interrupt enabled selected						Maintain previous state	GPIO selected	Hi-Z / Internal input fixed at 0	
	Resource other than above selected						Hi-Z / Internal input fixed at 0			
	GPIO selected							Maintain previous state		Maintain previous state
M	Sub crystal oscillator input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
	External sub clock input selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state / When oscillation stop*2, output maintain previous state / Internal input fixed at 0	Hi-Z / Input enabled / When oscillation stop*2, Hi-Z / Internal input fixed at 0	Maintain previous state / When oscillation stop*2, output maintain previous state / Internal input fixed at 0	Hi-Z / Input enabled / When oscillation stop*2, Hi-Z / Internal input fixed at 0	Maintain previous state / When Return from Deep Stand-by STOP mode, GPIO selected
	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Output maintain previous state / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	Output maintain previous state / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	Maintain previous state

12. Electrical Characteristics

12.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1,*2	V_{CC}	V_{SS} - 0.5	V_{SS} + 6.5	V	
Analog power supply voltage*1,*3	AV_{CC}	V_{SS} - 0.5	V_{SS} + 6.5	V	
Analog reference voltage*1,*3	AVRH	V_{SS} - 0.5	V_{SS} + 6.5	V	
Input voltage*1	V_I	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 6.5 V)	V	
		V_{SS} - 0.5	V_{SS} + 6.5	V	5V tolerant
Analog pin input voltage*1	V_{IA}	V_{SS} - 0.5	AV_{CC} + 0.5 (≤ 6.5 V)	V	
Output voltage*1	V_O	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 6.5 V)	V	
L level maximum output current*4	I_{OL}	-	10	mA	
L level average output current*5	I_{OLAV}	-	4	mA	
L level total maximum output current	$\sum I_{OL}$	-	60	mA	
L level total average output current*6	$\sum I_{OLAV}$	-	30	mA	
H level maximum output current*4	I_{OH}	-	-10	mA	
H level average output current*5	I_{OHAV}	-	- 4	mA	
H level total maximum output current	$\sum I_{OH}$	-	-60	mA	
H level total average output current*6	$\sum I_{OHAV}$	-	-30	mA	
Power consumption	P_D	-	400	mW	
Storage temperature	T_{STG}	- 55	+ 150	°C	

*1: These parameters are based on the condition that $V_{SS} = AV_{SS} = 0.0$ V.

*2: V_{CC} must not drop below V_{SS} - 0.5 V.

*3: Be careful not to exceed V_{CC} + 0.5 V, for example, when the power is turned on.

*4: The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

*5: The average output current is defined as the average current value flowing through any one of the corresponding pins for a 100 ms period.

*6: The total average output current is defined as the average current value flowing through all of corresponding pins for a 100 ms.

WARNING

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

12.4 AC Characteristics

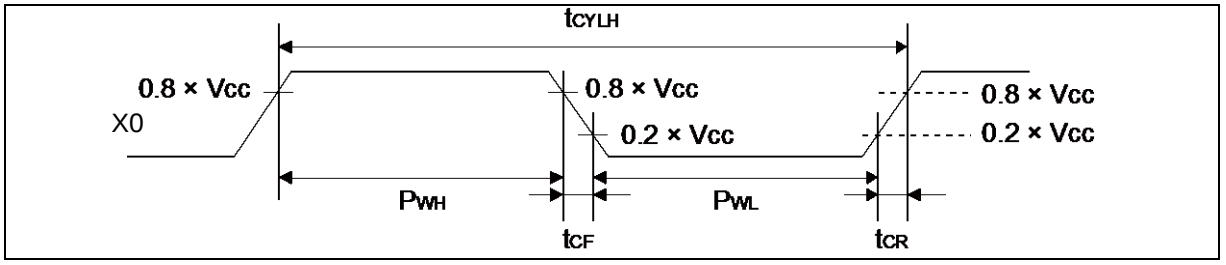
12.4.1 Main Clock Input Characteristics

(V_{CC} = 1.8V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	f_{CH}	X0, X1	V_{CC} ≥ 2.0 V	4	20	MHz	When crystal oscillator is connected
			V_{CC} < 2.0 V	4	4	MHz	
			V_{CC} ≥ 4.5 V	4	20	MHz	When using external clock
			V_{CC} < 4.5 V	4	16	MHz	
Input clock cycle	t_{CYLH}		V_{CC} ≥ 4.5 V	50	250	ns	When using external clock
			V_{CC} < 4.5 V	62.5	250	ns	
Input clock pulse width	-		P_{WH}/t_{CYLH}, P_{WL}/t_{CYLH}	45	55	%	When using external clock
Input clock rise time and fall time	t_{CF}, t_{CR}		-	-	5	ns	When using external clock
Internal operating clock*1 frequency	f_{CM}	-	-	-	20	MHz	Master clock
	f_{CC}	-	-	-	20	MHz	Base clock (HCLK/FCLK)
	f_{CP0}	-	-	-	20	MHz	APB0 bus clock*2
	f_{CP1}	-	-	-	20	MHz	APB1 bus clock*2
	f_{CP2}	-	-	-	20	MHz	APB2 bus clock*2
Internal operating clock*1 cycle time	t_{CYCC}	-	-	50	-	ns	Base clock (HCLK/FCLK)
	t_{CYCP0}	-	-	50	-	ns	APB0 bus clock*2
	t_{CYCP1}	-	-	50	-	ns	APB1 bus clock*2
	t_{CYCP2}	-	-	50	-	ns	APB2 bus clock*2

*1: For more information about each internal operating clock, see Chapter 2-1: Clock in FM3 Family Peripheral Manual.

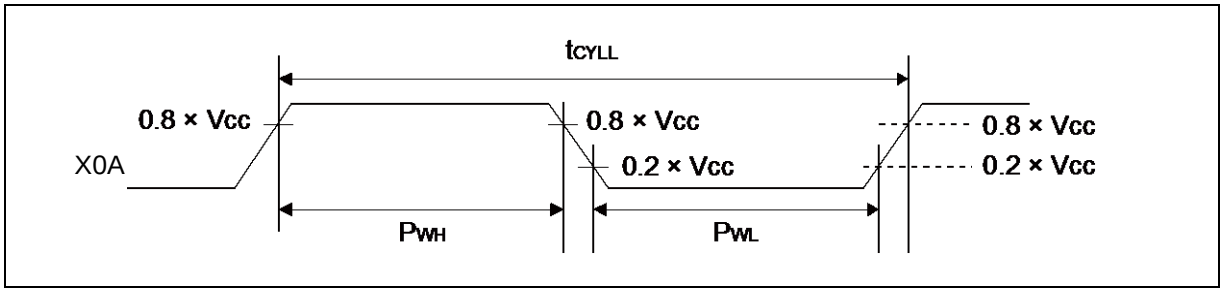
*2: For about each APB bus which each peripheral is connected to, see Block Diagram in this data sheet.



12.4.2 Sub Clock Input Characteristics

(V_{CC} = 1.8V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	f_{CL}	X0A, X1A	-	-	32.768	-	kHz	When crystal oscillator is connected
			-	32	-	100	kHz	When using external clock
Input clock cycle	t_{CYLL}		-	10	-	31.25	µs	When using external clock
Input clock pulse width	-		P_{WH}/t_{CYLL}, P_{WL}/t_{CYLL}	45	-	55	%	When using external clock



12.4.3 Built-in CR Oscillation Characteristics

Built-in High-speed CR

(V_{CC} = 1.8V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Conditions		Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	f_{CRH}	$V_{CC} \geq$ 2.2 V	T_A = + 25°C	3.92	4	4.08	MHz	When trimming*1
			T_A = - 40°C to + 85°C	3.8	4	4.2		
			T_A = - 40°C to + 85°C	2.3	-	7.03		When not trimming
		V_{CC} < 2.2 V	T_A = + 25°C	3.4	4	4.6	MHz	When trimming*1
			T_A = - 40°C to + 85°C	3.16	4	4.84		
			T_A = - 40°C to + 85°C	2.3	-	7.03		When not trimming
Frequency stabilization time	t_{CRWT}	-		-	-	10	µs	*2

*1: In the case of using the values in CR trimming area of Flash memory at shipment for frequency trimming.

*2: This is the time to stabilize the frequency of High-speed CR clock after setting trimming value. This period is able to use High-speed CR clock as source clock.

Built-in Low-speed CR

(V_{CC} = 1.8V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_{CRL}	-	50	100	150	kHz	

12.4.6 Reset Input Characteristics

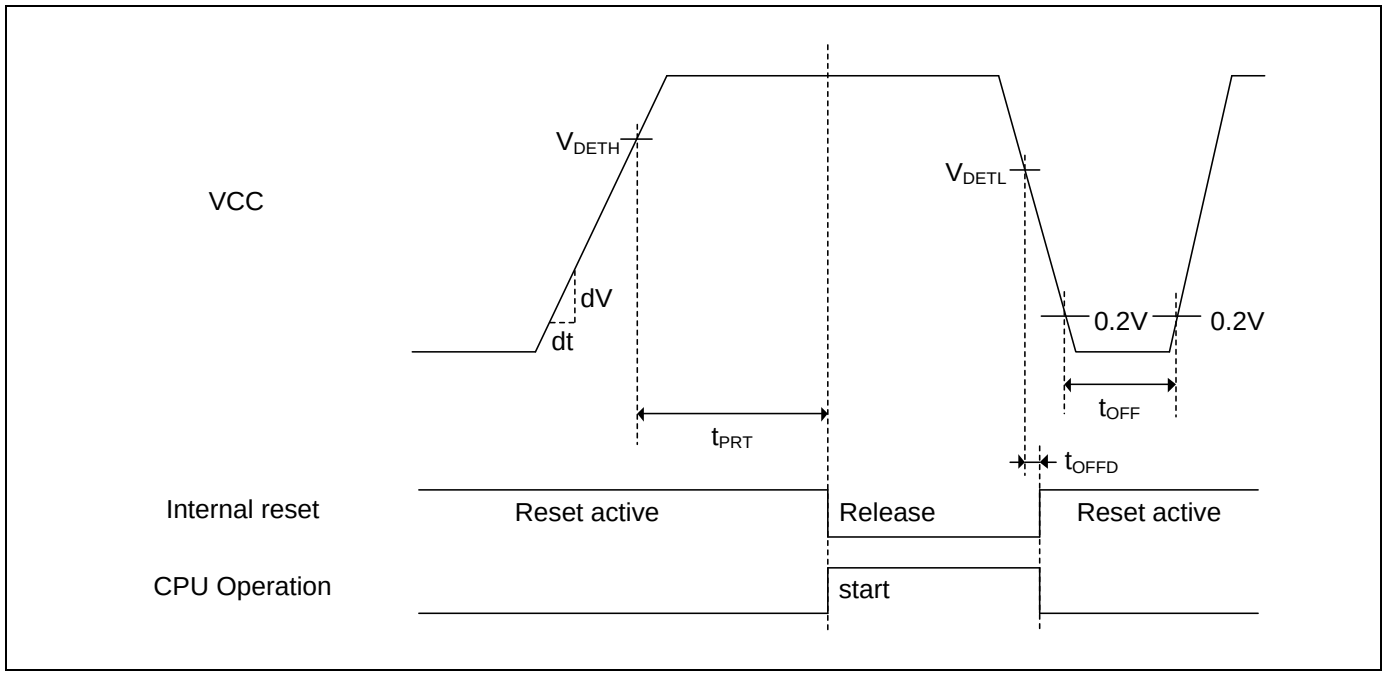
(V_{CC} = 1.8V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{INITX}	INITX	-	500	-	ns	
				1.5	-	ms	When RTC mode or Stop mode
				1.5	-	ms	When Deep Standby mode

12.4.7 Power-on Reset Timing

(V_{CC} = 1.8V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Power supply rising time	dV/dt	VCC	0.1	-	-	V/ms	
Power supply shut down time	t_{OFF}		1	-	-	ms	
Reset release voltage	V_{DETH}		1.44	1.60	1.76	V	When voltage rises
Reset detection voltage	V_{DETL}		1.39	1.55	1.71	V	When voltage drops
Time until releasing Power-on reset	t_{PRT}		0.46	-	11.4	ms	dV/dt ≥ 0.1mV/µs
Reset detection delay time	t_{OFFD}		-	-	0.4	ms	dV/dt ≥ -0.04mV/µs



12.4.9 CSIO/UART Timing

CSIO (SPI = 0, SCINV = 0)

(V_{CC} = 1.8V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

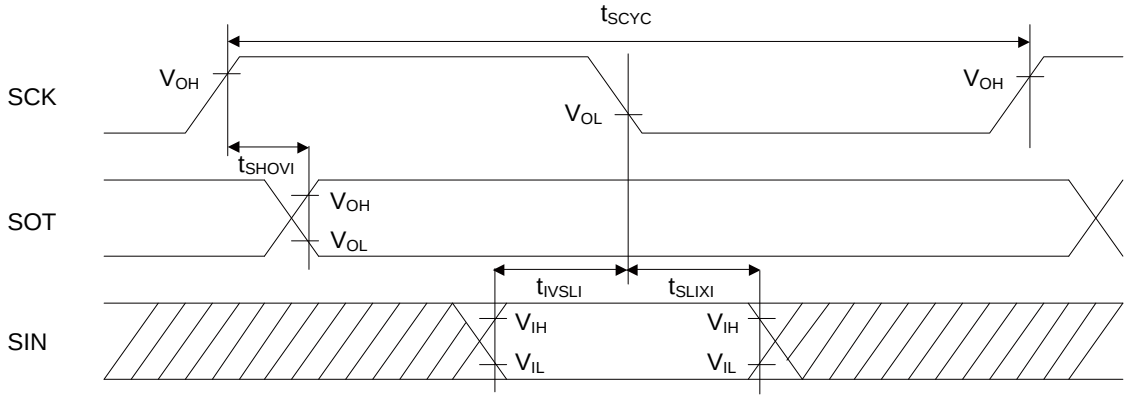
Parameter	Symbol	Pin name	Conditions	V_{CC} < 2.7 V		2.7 V ≤ V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	$4t_{CYCP}$	-	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKx, SOTx		-40	+40	-30	+30	-20	+20	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKx, SINx		75	-	50	-	30	-	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	0	-	0	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	Slave mode	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKx, SOTx		-	75	-	50	-	30*1 40*2	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	10	-	10	-	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	20	-	20	-	ns
SCK falling time	t_F	SCKx		-	5	-	5	-	5	ns
SCK rising time	t_R	SCKx		-	5	-	5	-	5	ns

*1 When PZR = 0.

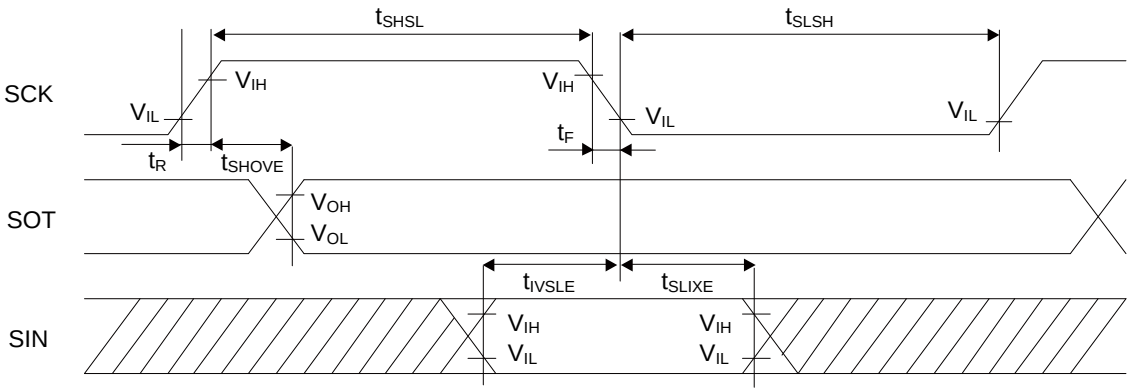
*2 When PZR = 1.

Notes:

- The above characteristics apply to clock synchronous mode.
- t_{CYCP} indicates the APB bus clock cycle time.
  About the APB bus number which Multi-function serial is connected to, see Block Diagram in this data sheet.
- These characteristics only guarantee the same relocate port number.
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- When the external load capacitance C_L = 50 pF.



Master mode



Slave mode

CSIO (SPI = 0, SCINV = 1)

(V_{CC} = 1.8V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	V_{CC} < 2.7 V		2.7 V ≤ V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	$4t_{CYCP}$	-	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCKx, SOTx		-40	+40	-30	+30	-20	+20	ns
SIN → SCK ↓ setup time	t_{IVSLI}	SCKx, SINx		75	-	50	-	30	-	ns
SCK ↓ → SIN hold time	t_{SLIXI}	SCKx, SINx		0	-	0	-	0	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	Slave mode	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCKx, SOTx		-	75	-	50	-	30*1 40*2	ns
SIN → SCK ↓ setup time	t_{IVSLE}	SCKx, SINx		10	-	10	-	10	-	ns
SCK ↓ → SIN hold time	t_{SLIXE}	SCKx, SINx		20	-	20	-	20	-	ns
SCK falling time	t_F	SCKx		-	5	-	5	-	5	ns
SCK rising time	t_R	SCKx		-	5	-	5	-	5	ns

*1 When PZR = 0.

*2 When PZR = 1.

Notes:

- The above characteristics apply to clock synchronous mode.
- t_{CYCP} indicates the APB bus clock cycle time.
  About the APB bus number which Multi-function serial is connected to, see Block Diagram in this data sheet
- These characteristics only guarantee the same relocate port number.
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- When the external load capacitance C_L = 50 pF.

12.4.11 I^2C Timing

(V_{CC} = 1.8V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

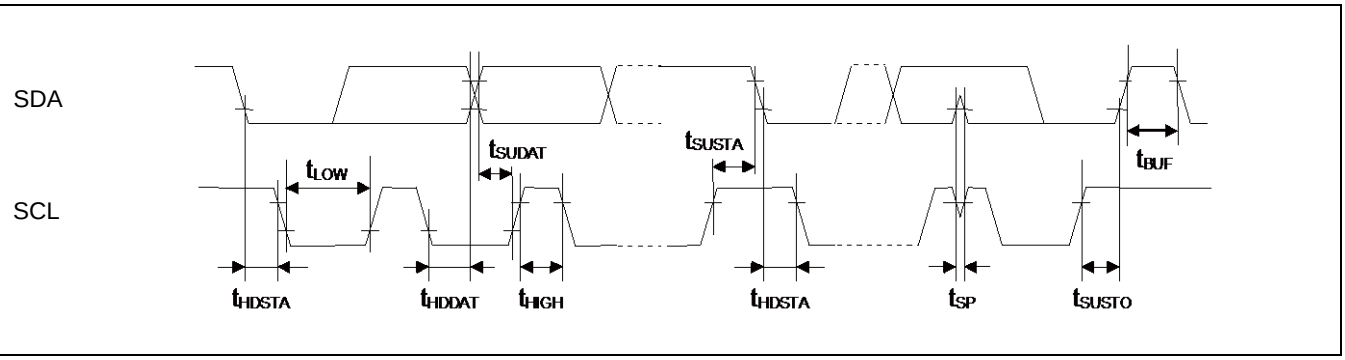
Parameter	Symbol	Conditions	Standard-mode		Fast-mode		Unit	Remarks
			Min	Max	Min	Max		
SCL clock frequency	f_{SCL}	C_L = 50 pF, R = (V_P/I_{OL})*1	0	100	0	400	kHz	
(Repeated) START condition hold time SDA ↓ → SCL ↓	t_{HDSTA}		4.0	-	0.6	-	µs	
SCL clock L width	t_{LOW}		4.7	-	1.3	-	µs	
SCL clock H width	t_{HIGH}		4.0	-	0.6	-	µs	
(Repeated) START condition setup time SCL ↑ → SDA ↓	t_{SUSTA}		4.7	-	0.6	-	µs	
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}		0	3.45*2	0	0.9*3	µs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}		250	-	100	-	ns	
STOP condition setup time SCL ↑ → SDA ↑	t_{SUSTO}		4.0	-	0.6	-	µs	
Bus free time between STOP condition and START condition	t_{BUF}		4.7	-	1.3	-	µs	
Noise filter	t_{SP}	-	2 t_{CYCP}*4	-	2 t_{CYCP}*4	-	ns	

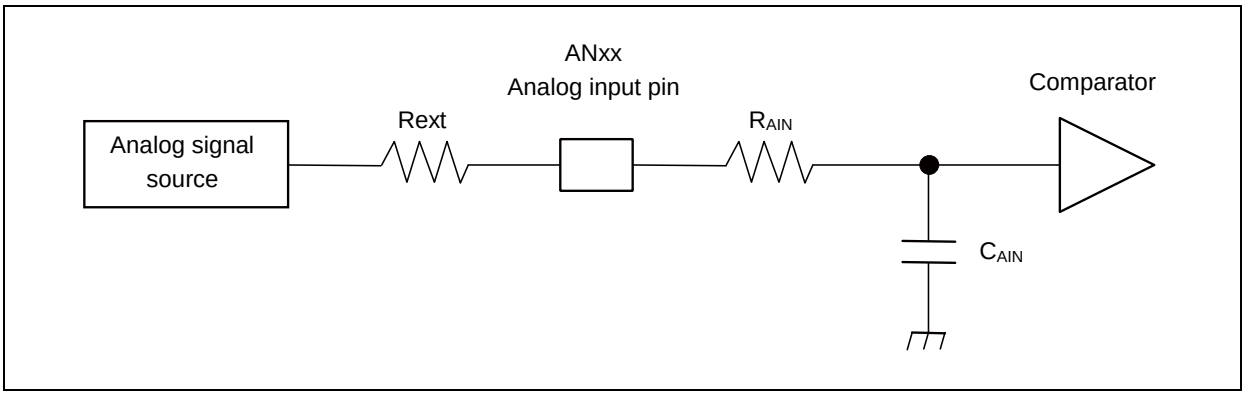
*1: R and C_L represent the pull-up resistor and load capacitance of the SCL and SDA lines, respectively.
V_P indicates the power supply voltage of the pull-up resistor and I_{OL} indicates V_{OL} guaranteed current.

*2: The maximum t_{HDDAT} must satisfy that it does not extend at least L period (t_{LOW}) of device's SCL signal.

*3: A Fast-mode I^2C bus device can be used on a Standard-mode I^2C bus system as long as the device satisfies the requirement of $t_{SUDAT} \geq 250$ ns.

*4: t_{CYCP} is the APB bus clock cycle time.
About the APB bus number which I^2C is connected to, see Block Diagram in this data sheet.
To use Standard-mode, set the APB bus clock at 2 MHz or more.
To use Fast-mode, set the APB bus clock at 8 MHz or more.





(Equation 1) $t_S \geq (R_{AIN} + R_{EXT}) \times C_{AIN} \times 9$

t_S : Sampling time

R_{AIN} : Input resistor of A/D = 0.9 kΩ at 4.5 V ≤ AV_{CC} ≤ 5.5 V
Input resistor of A/D = 1.6 kΩ at 2.7 V ≤ AV_{CC} < 4.5 V
Input resistor of A/D = 4.0 kΩ at 1.8 V ≤ AV_{CC} < 2.7 V

C_{AIN} : Input capacity of A/D = 15 pF at 1.8 V ≤ AV_{CC} ≤ 5.5 V

R_{EXT} : Output impedance of external circuit

(Equation 2) $t_C = t_{CCK} \times 14$

t_C : Compare time

t_{CCK} : Compare clock cycle

12.7 Flash Memory Write/Erase Characteristics

12.7.1 Write / Erase time

(V_{CC} = 2.0V to 5.5V, T_A = - 40°C to + 85°C)

Parameter		Value		Unit	Remarks
		Typ*	Max*		
Sector erase time	Large Sector	1.6	7.5	s	Includes write time prior to internal erase
	Small Sector	0.4	2.1		
Half word (16-bit) write time		25	400	µs	Not including system-level overhead time.
Chip erase time		4	19.2	s	Includes write time prior to internal erase

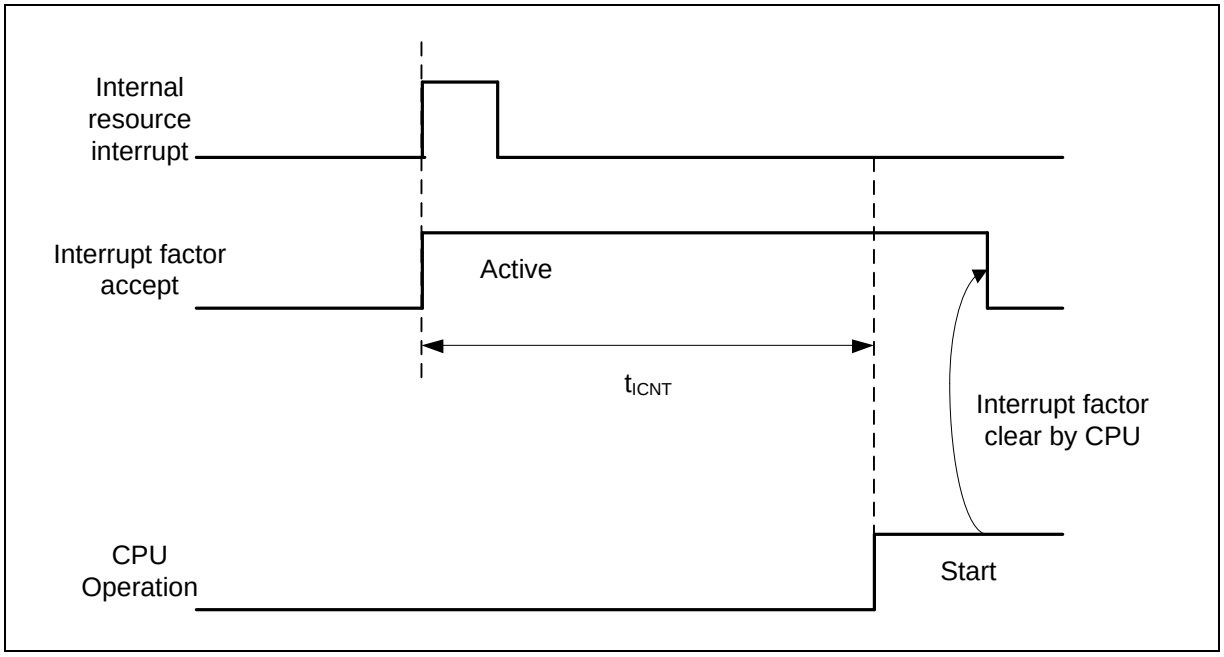
*: The typical value is immediately after shipment, the maximam value is guarantee value under 100,000 cycle of erase/write.

12.7.2 Write cycles and data hold time

Erase/write cycles (cycle)	Data hold time (year)	Remarks
1,000	20*	
10,000	10*	
100,000	5*	

*: At average + 85°C

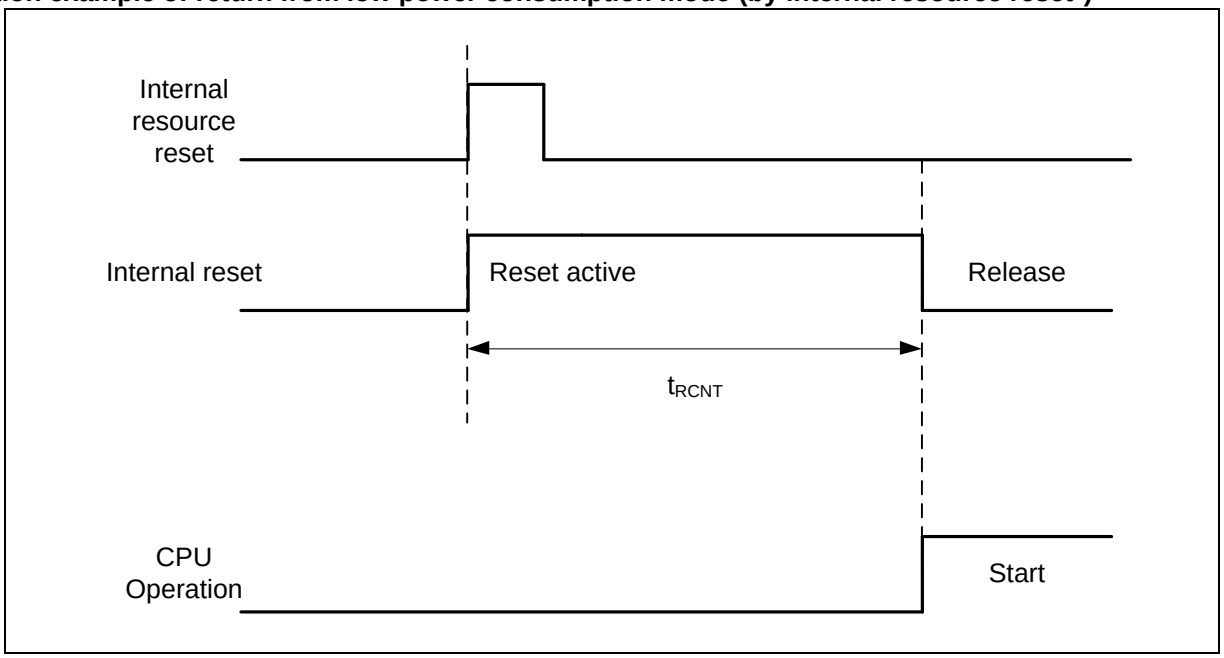
Operation example of return from Low-Power consumption mode (by internal resource interrupt*)



*: Internal resource interrupt is not included in return factor by the kind of Low-Power consumption mode.

Notes:
- The return factor is different in each Low-Power consumption modes. See Chapter 6: Low Power Consumption Mode and Operations of Standby Modes in FM3 Family Peripheral Manual.
- When interrupt recoveries, the operation mode that CPU recoveries depend on the state before the Low-Power consumption mode transition. See Chapter 6: Low Power Consumption Mode in FM3 Family Peripheral Manual.

Operation example of return from low power consumption mode (by internal resource reset*)

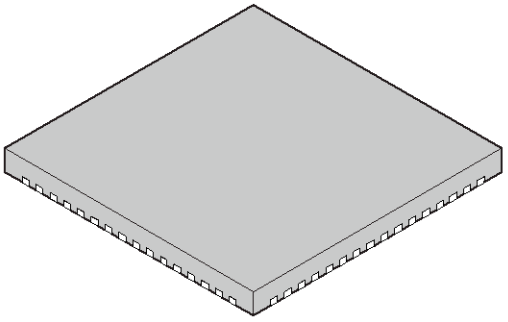


*: Internal resource reset is not included in return factor by the kind of Low-Power consumption mode.

Notes:
- The return factor is different in each Low-Power consumption modes.
  See Chapter 6: Low Power Consumption Mode and Operations of Standby Modes in FM3 Family Peripheral Manual.
- When interrupt recoveries, the operation mode that CPU recoveries depend on the state before the Low-Power consumption mode transition. See Chapter 6: Low Power Consumption Mode in FM3 Family Peripheral Manual.
- The time during the power-on reset/low-voltage detection reset is excluded. See (6) Power-on Reset Timing in 12.4 AC Characteristics in Electrical Characteristics for the detail on the time during the power-on reset/low-voltage detection reset.
- When in recovery from reset, CPU changes to the High-speed CR Run mode. When using the main clock or the PLL clock, it is necessary to add the main clock oscillation stabilization wait time or the Main PLL clock stabilization wait time.
- The internal resource reset means the watchdog reset and the CSV reset.

13. Ordering Information

Part number	On-chip Flash memory	On-chip SRAM	Package	Packing
MB9AF131KBPMC-G-SNE2	64 Kbyte	8 Kbyte	Plastic・LQFP (0.5mm pitch), 48-pin (FPT-48P-M49)	Tray
MB9AF132KBPMC-G-SNE2	128 Kbyte	8 Kbyte		
MB9AF131KBQN-G-AVE2	64 Kbyte	8 Kbyte	Plastic・QFN (0.5mm pitch), 48-pin (LCC-48P-M73)	
MB9AF132KBQN-G-AVE2	128 Kbyte	8 Kbyte		
MB9AF131LBPMC1-G-SNE2	64 Kbyte	8 Kbyte	Plastic・LQFP (0.5mm pitch), 64-pin (FPT-64P-M38)	
MB9AF132LBPMC1-G-SNE2	128 Kbyte	8 Kbyte		
MB9AF131LBPMC-G-SNE2	64 Kbyte	8 Kbyte	Plastic・LQFP (0.65mm pitch), 64-pin (FPT-64P-M39)	
MB9AF132LBPMC-G-SNE2	128 Kbyte	8 Kbyte		
MB9AF131LBQN-G-AVE2	64 Kbyte	8 Kbyte	Plastic・QFN (0.5mm pitch), 64-pin (LCC-64P-M24)	
MB9AF132LBQN-G-AVE2	128 Kbyte	8 Kbyte		

64-pin plastic QFN		
	Lead pitch	0.50 mm
	Package width × package length	9.00 mm × 9.00 mm
	Sealing method	Plastic mold
	Mounting height	0.90 mm MAX
	Weight	-
(LCC-64P-M24)