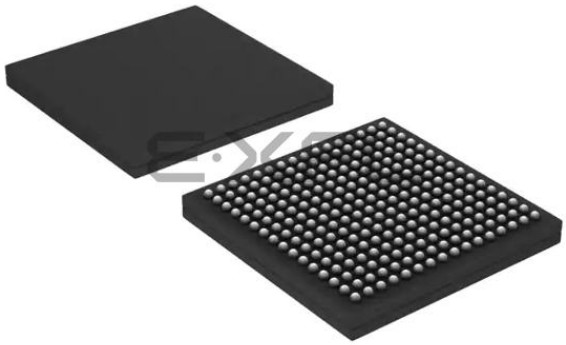

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, SD, SPI, UART/USART, USB, USB OTG
Peripherals	DMA, I²S, LCD, LVD, POR, PWM, WDT
Number of I/O	128
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 71x16b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	256-LBGA
Supplier Device Package	256-MAPPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk70fn1m0vmj12

3.2 Examples

Operating rating:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

Operating requirement:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

Operating behavior that includes a *typical value*:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	µA

3.3 Typical-value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DD}	3.3 V supply voltage	3.3	V

Table 4. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{OHT_DDR}	Output high current total for DDR pins	—	—	100	mA	
	• DDR1	—	—	56	mA	
	• DDR2	—	—	39	mA	
	• LPDDR1					
V_{OH_Tamper}	Output high voltage — high drive strength	V_{BAT} – 0.5	—	—	V	
	• 2.7 V ≤ V_{BAT} ≤ 3.6 V, I_{OH} = -10mA	V_{BAT} – 0.5	—	—	V	
	• 1.71 V ≤ V_{BAT} ≤ 2.7 V, I_{OH} = -3mA					
	Output high voltage — low drive strength	V_{BAT} – 0.5	—	—	V	
	• 2.7 V ≤ V_{BAT} ≤ 3.6 V, I_{OH} = -2mA	V_{BAT} – 0.5	—	—	V	
	• 1.71 V ≤ V_{BAT} ≤ 2.7 V, I_{OH} = -0.6mA					
I_{OH_Tamper}	Output high current total for Tamper pins	—	—	100	mA	
V_{OL}	Output low voltage — high drive strength		—			
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 10 mA	—	—	0.5	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 5 mA	—		0.5	V	
	Output low voltage — low drive strength		—			
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 2 mA	—	—	0.5	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 1 mA	—		0.5	V	
I_{OLT}	Output low current total for all ports	—	—	100	mA	
I_{OLT_io60}	Output low current total for fast digital ports	—	—	100	mA	
V_{OL_DDR}	Output low voltage for DDR pins	—	—	0.37	V	
	• DDR1 (I_{OL} = 16.2 mA)	—	—	0.28	V	
	• DDR2 half strength (I_{OL} = 5.36 mA)	—	—	0.28	V	
	• DDR2 full strength (I_{OL} = 13.4 mA)	—	—	0.1 x V_{DD_DDR}	V	
	• LPDDR1 half strength (I_{OL} = 0.1 mA)	—	—	0.1 x V_{DD_DDR}	V	
	• LPDDR1 full strength (I_{OL} = 0.1 mA)					
I_{OLT_DDR}	Output low current total for DDR pins	—	—	100	mA	
	• DDR1			56	mA	
	• DDR2			39	mA	
	• LPDDR1					
V_{OL_Tamper}	Output low voltage — high drive strength	—	—	0.5	V	
	• 2.7 V ≤ V_{BAT} ≤ 3.6 V, I_{OL} = 10mA	—	—	0.5	V	
	• 1.71 V ≤ V_{BAT} ≤ 2.7 V, I_{OL} = 3mA					
	Output low voltage — low drive strength	—	—	0.5	V	
	• 2.7 V ≤ V_{BAT} ≤ 3.6 V, I_{OL} = 2mA	—	—	0.5	V	
	• 1.71 V ≤ V_{BAT} ≤ 2.7 V, I_{OL} = 0.6mA					

Table continues on the next page...

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.
2. Digital pins have an associated GPIO port function and have 5V tolerant inputs, except EXTAL and XTAL.
3. Internal pull-up/pull-down resistors disabled.
4. Characterized, not tested in production.
5. Examples calculated using V_{IL} relation, V_{DD}, and max I_{IND}: $Z_{IND}=V_{IL}/I_{IND}$. This is the impedance needed to pull a high signal to a level below V_{IL} due to leakage when $V_{IL} < V_{IN} < V_{DD}$. These examples assume signal source low = 0 V. See Figure 2.
6. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{SS}
7. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{DD}

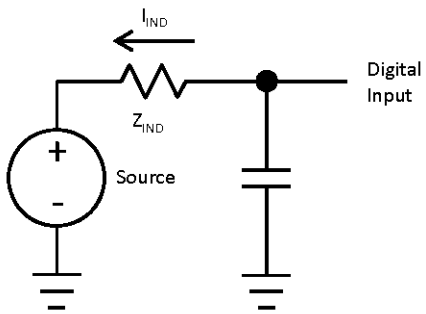

Figure 2. 5 V Tolerant Input IIND Parameter

5.2.4 Power mode transition operating behaviors

All specifications except t_{POR}, and VLLSx→RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 100 MHz
- Bus clock = 50 MHz
- FlexBus clock = 50 MHz
- Flash clock = 25 MHz
- MCG mode: FEI

Table 5. Power mode transition operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip. • V_{DD} slew rate ≥ 5.7 kV/s • V_{DD} slew rate < 5.7 kV/s	 — —	 300 1.7 V / (V_{DD} slew rate)	µs	1
	• VLLS1 → RUN	—	160	µs	
	• VLLS2 → RUN	—	114	µs	

Table continues on the next page...

6.1.2 JTAG electricals

Table 13. JTAG limited voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
J1	TCLK frequency of operation			MHz
	• Boundary Scan	0	10	
	• JTAG and CJTAG	0	25	
	• Serial Wire Debug	0	50	
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width			
	• Boundary Scan	50	—	ns
	• JTAG and CJTAG	20	—	ns
	• Serial Wire Debug	10	—	ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	2.4	—	ns
J7	TCLK low to boundary scan output data valid	—	25	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1	—	ns
J11	TCLK low to TDO data valid	—	17	ns
J12	TCLK low to TDO high-Z	—	17	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns

Table 14. JTAG full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	TCLK frequency of operation			MHz
	• Boundary Scan	0	10	
	• JTAG and CJTAG	0	20	
	• Serial Wire Debug	0	40	
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width			
	• Boundary Scan	50	—	ns
	• JTAG and CJTAG	25	—	ns
	• Serial Wire Debug	12.5	—	ns
J4	TCLK rise and fall times	—	3	ns

Table continues on the next page...

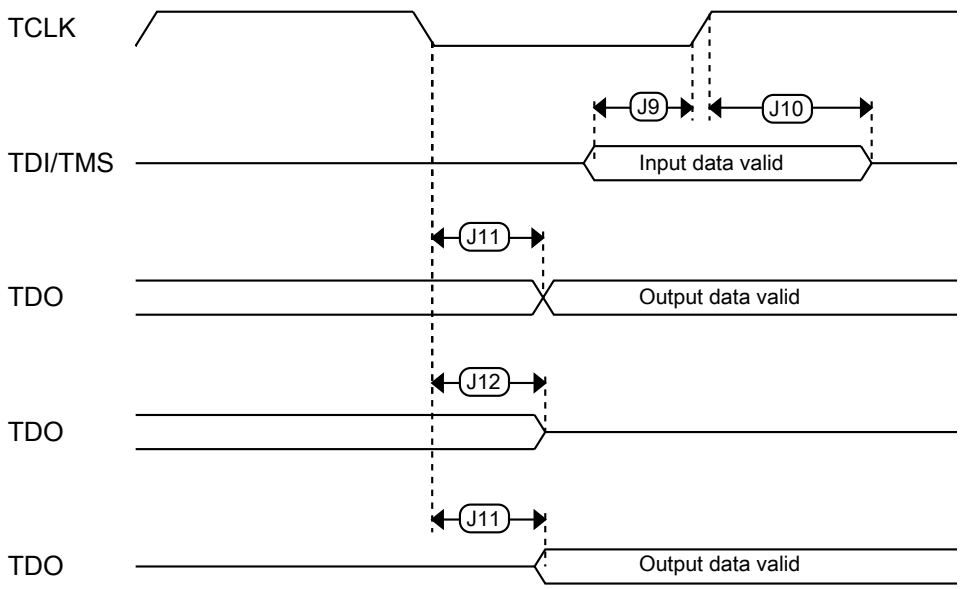

Figure 9. Test Access Port timing

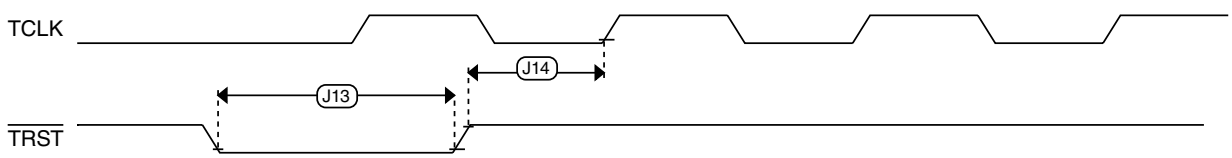

Figure 10. $\overline{\text{TRST}}$ timing

6.2 System modules

There are no specifications necessary for the device's system modules.

6.3 Clock modules

6.3.1 MCG specifications

Table 15. MCG specifications

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
f_{ints_ft}	Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C		—	32.768	—	kHz	
f_{ints_t}	Internal reference frequency (slow clock) — user trimmed		31.25	—	39.0625	kHz	
$\Delta_{fdco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM		—	± 0.3	± 0.6	$\%f_{dco}$	1
$\Delta f_{dco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM only		—	± 0.2	± 0.5	$\%f_{dco}$	1
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C		—	± 4.5	—	$\%f_{dco}$	1
f_{intf_ft}	Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C		—	4	—	MHz	
f_{intf_t}	Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C		3	—	5	MHz	
f_{loc_low}	Loss of external clock minimum frequency — RANGE = 00		(3/5) x f_{ints_t}	—	—	kHz	
f_{loc_high}	Loss of external clock minimum frequency — RANGE = 01, 10, or 11		(16/5) x f_{ints_t}	—	—	kHz	
FLL							
f_{fll_ref}	FLL reference frequency range		31.25	—	39.0625	kHz	
f_{dco}	DCO output frequency range	Low range (DRS=00) 640 × f_{fll_ref}	20	20.97	25	MHz	2, 3
		Mid range (DRS=01) 1280 × f_{fll_ref}	40	41.94	50	MHz	
		Mid-high range (DRS=10) 1920 × f_{fll_ref}	60	62.91	75	MHz	
		High range (DRS=11) 2560 × f_{fll_ref}	80	83.89	100	MHz	
$f_{dco\_t\_DMX32}$	DCO output frequency	Low range (DRS=00) 732 × f_{fll_ref}	—	23.99	—	MHz	4, 5
		Mid range (DRS=01) 1464 × f_{fll_ref}	—	47.97	—	MHz	
		Mid-high range (DRS=10) 2197 × f_{fll_ref}	—	71.99	—	MHz	
		High range (DRS=11) 2929 × f_{fll_ref}	—	95.98	—	MHz	
J_{cyc_fll}	FLL period jitter		—	180	—	ps	

Table continues on the next page...

6.3.2 Oscillator electrical specifications

6.3.2.1 Oscillator DC electrical specifications

Table 16. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	
I_{DDOSC}	Supply current — low-power mode (HGO=0)					1
	• 32 kHz	—	500	—	nA	
	• 4 MHz	—	200	—	µA	
	• 8 MHz (RANGE=01)	—	300	—	µA	
	• 16 MHz	—	950	—	µA	
	• 24 MHz	—	1.2	—	mA	
	• 32 MHz	—	1.5	—	mA	
I_{DDOSC}	Supply current — high-gain mode (HGO=1)					1
	• 32 kHz	—	25	—	µA	
	• 4 MHz	—	400	—	µA	
	• 8 MHz (RANGE=01)	—	500	—	µA	
	• 16 MHz	—	2.5	—	mA	
	• 24 MHz	—	3	—	mA	
	• 32 MHz	—	4	—	mA	
C_x	EXTAL load capacitance	—	—	—		2, 3
C_y	XTAL load capacitance	—	—	—		2, 3
R_F	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	—	MΩ	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	—	MΩ	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	—	—	MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	—	1	—	MΩ	
R_S	Series resistor — low-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200	—	kΩ	
	Series resistor — high-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — high-frequency, high-gain mode (HGO=1)	—	0	—	kΩ	

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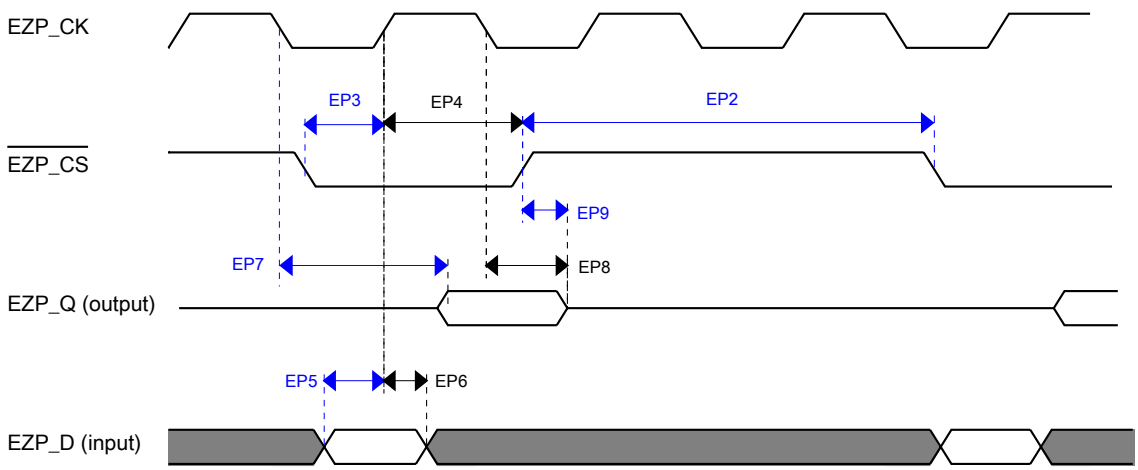

Figure 12. EzPort Timing Diagram

6.4.3 NFC specifications

The NAND flash controller (NFC) implements the interface to standard NAND flash memory devices. This section describes the timing parameters of the NFC.

In the following table:

- T_H is the flash clock high time and
- T_L is flash clock low time,

which are defined as:

$$T_{NFC} = T_L + T_H = \frac{T_{input\ clock}}{SCALER}$$

The SCALER value is derived from the fractional divider specified in the SIM's CLKDIV4 register:

$$SCALER = \frac{SIM\_CLKDIV4[NFCFRAC] + 1}{SIM\_CLKDIV4[NFCDIV] + 1}$$

In case the reciprocal of SCALER is an integer, the duty cycle of NFC clock is 50%, means $T_H = T_L$. In case the reciprocal of SCALER is not an integer:

$$T_L = (1 + SCALER / 2) \times \frac{T_{NFC}}{2}$$

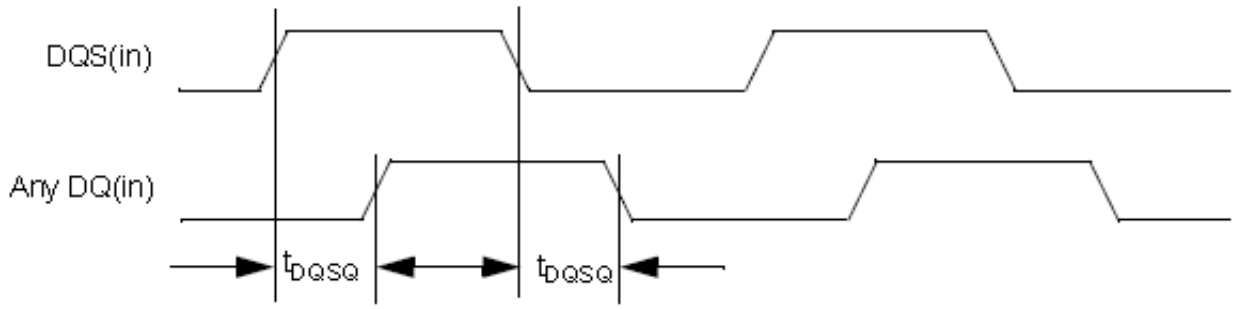

Figure 20. DDR read timing, DQ vs. DQS

6.4.5 Flexbus switching specifications

All processor bus timings are synchronous; input setup/hold and output delay are given in respect to the rising edge of a reference clock, FB_CLK. The FB_CLK frequency may be the same as the internal system bus frequency or an integer divider of that frequency.

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the Flexbus output clock (FB_CLK). All other timing relationships can be derived from these values.

Table 27. Flexbus limited voltage range switching specifications

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	FB_CLK	MHz	
FB1	Clock period	20	—	ns	
FB2	Address, data, and control output valid	—	11.5	ns	1
FB3	Address, data, and control output hold	0.5	—	ns	1
FB4	Data and $\overline{\text{FB\_TA}}$ input setup	8.5	—	ns	2
FB5	Data and $\overline{\text{FB\_TA}}$ input hold	0.5	—	ns	2

1. Specification is valid for all FB_AD[31:0], $\overline{\text{FB\_BE/BWE}n}$, $\overline{\text{FB\_CS}n}$, $\overline{\text{FB\_OE}}$, FB_R/$\overline{\text{W}}$,$\overline{\text{FB\_TBST}}$, FB_TSIZ[1:0], FB_ALE, and $\overline{\text{FB\_TS}}$.
2. Specification is valid for all FB_AD[31:0] and $\overline{\text{FB\_TA}}$.

Table 28. Flexbus full voltage range switching specifications

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	
	Frequency of operation	—	FB_CLK	MHz	
FB1	Clock period	1/FB_CLK	—	ns	
FB2	Address, data, and control output valid	—	13.5	ns	1
FB3	Address, data, and control output hold	0	—	ns	1

Table continues on the next page...

6.6.3.2 12-bit DAC operating behaviors

Table 35. 12-bit DAC operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA_DACLP}	Supply current — low-power mode	—	—	150	μA	
I_{DDA_DACHP}	Supply current — high-speed mode	—	—	700	μA	
t_{DACLP}	Full-scale settling time (0x080 to 0xF7F) — low-power mode	—	100	200	μs	1
t_{DACHP}	Full-scale settling time (0x080 to 0xF7F) — high-power mode	—	15	30	μs	1
$t_{CCDACLP}$	Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode	—	0.7	1	μs	1
$V_{dacoutl}$	DAC output voltage range low — high-speed mode, no load, DAC set to 0x000	—	—	100	mV	
$V_{dacouth}$	DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFF	V_{DACR} −100	—	V_{DACR}	mV	
INL	Integral non-linearity error — high speed mode	—	—	±8	LSB	2
DNL	Differential non-linearity error — V_{DACR} > 2 V	—	—	±1	LSB	3
DNL	Differential non-linearity error — V_{DACR} = VREF_OUT	—	—	±1	LSB	4
V_{OFFSET}	Offset error	—	±0.4	±0.8	%FSR	5
E_G	Gain error	—	±0.1	±0.6	%FSR	5
PSRR	Power supply rejection ratio, V_{DDA} ≥ 2.4 V	60	—	90	dB	
T_{CO}	Temperature coefficient offset voltage	—	3.7	—	μV/C	6
T_{GE}	Temperature coefficient gain error	—	0.000421	—	%FSR/C	
Rop	Output resistance (load = 3 kΩ)	—	—	250	Ω	
SR	Slew rate -80h→ F7Fh→ 80h				V/μs	
	• High power (SP_{HP})	1.2	1.7	—		
	• Low power (SP_{LP})	0.05	0.12	—		
CT	Channel to channel cross talk	—	—	-80	dB	
BW	3dB bandwidth				kHz	
	• High power (SP_{HP})	550	—	—		
	• Low power (SP_{LP})	40	—	—		

1. Settling within ±1 LSB
2. The INL is measured for 0 + 100 mV to V_{DACR} −100 mV
3. The DNL is measured for 0 + 100 mV to V_{DACR} −100 mV
4. The DNL is measured for 0 + 100 mV to V_{DACR} −100 mV with V_{DDA} > 2.4 V
5. Calculated by a best fit curve from V_{SS} + 100 mV to V_{DACR} − 100 mV
6. V_{DDA} = 3.0 V, reference select set for V_{DDA} (DACx_CO:DACRFS = 1), high power mode (DACx_C0:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device

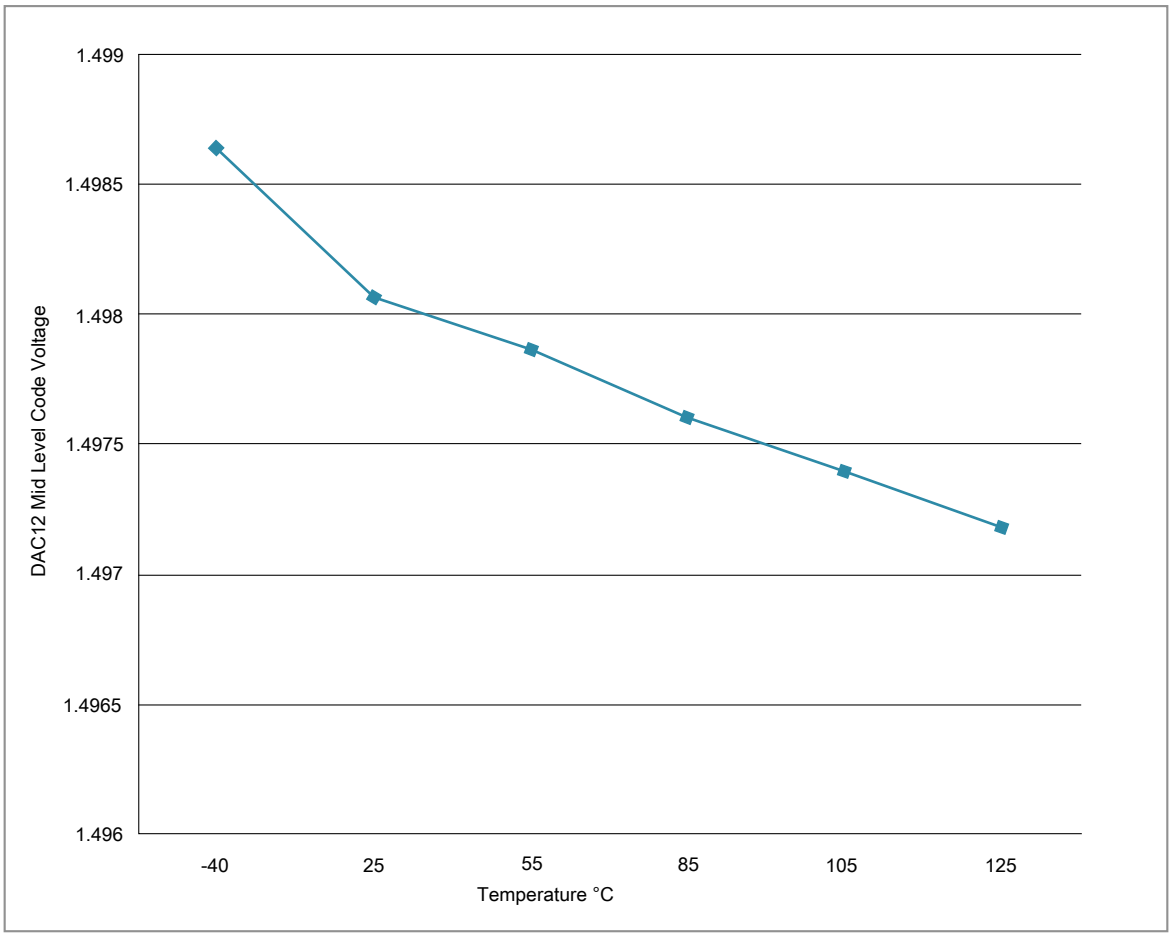

Figure 29. Offset at half scale vs. temperature

6.6.4 Voltage reference electrical specifications

Table 36. VREF full-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage	1.71	3.6	V	
T_A	Temperature	Operating temperature range of the device		°C	
C_L	Output load capacitance	100		nF	1, 2

1. C_L must be connected to VREF_OUT if the VREF_OUT functionality is being used for either an internal or external reference.
2. The load capacitance should not exceed +/-25% of the nominal specified C_L value over the operating temperature range of the device.

Table 46. Slave mode DSPI timing (limited voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
	Frequency of operation		15	MHz
DS9	DSPI_SCK input cycle time	4 x t_{BUS}	—	ns
DS10	DSPI_SCK input high/low time	(t_{SCK}/2) – 2	(t_{SCK}/2) + 2	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	10	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	14	ns
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	14	ns

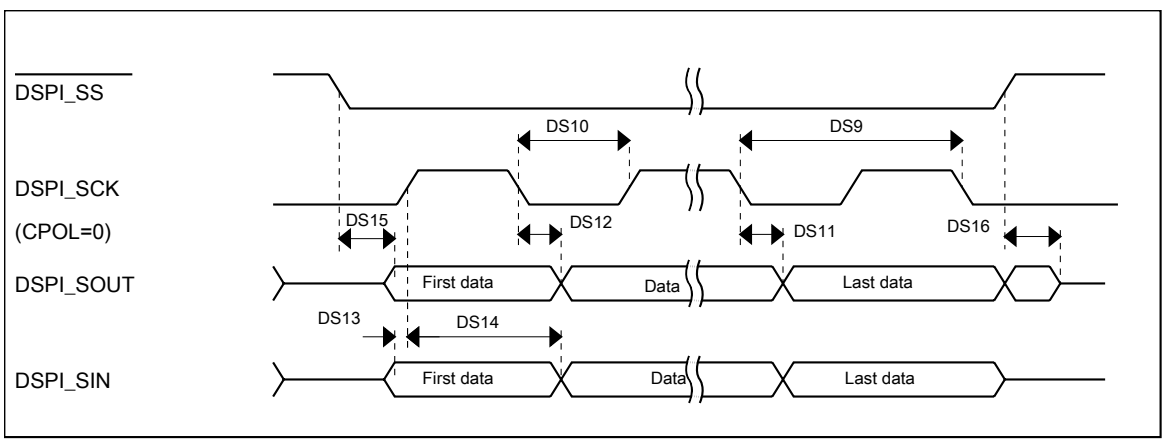

Figure 34. DSPI classic SPI timing — slave mode

6.8.8 DSPI switching specifications (full voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provides DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 47. Master mode DSPI timing (full voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	1
	Frequency of operation	—	15	MHz	
DS1	DSPI_SCK output cycle time	4 x t_{BUS}	—	ns	

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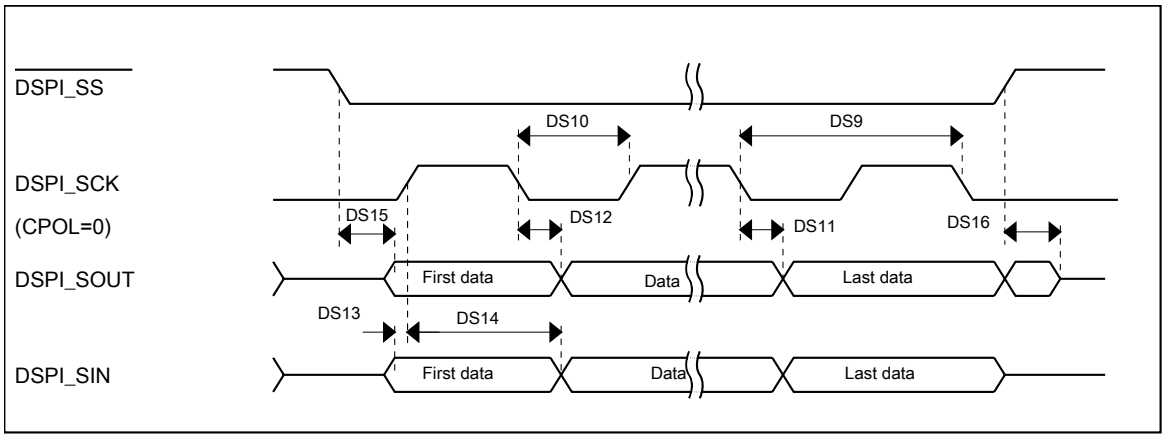

Figure 36. DSPI classic SPI timing — slave mode

6.8.9 Inter-Integrated Circuit Interface (I^2C) timing

Table 49. I^2C timing

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
SCL Clock Frequency	f_{SCL}	0	100	0	400 [1]	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t_{HD}; STA	4	—	0.6	—	µs
LOW period of the SCL clock	t_{LOW}	4.7	—	1.25	—	µs
HIGH period of the SCL clock	t_{HIGH}	4	—	0.6	—	µs
Set-up time for a repeated START condition	t_{SU}; STA	4.7	—	0.6	—	µs
Data hold time for I^2C bus devices	t_{HD}; DAT	0[2]	3.45[3]	0[4]	0.9[2]	µs
Data set-up time	t_{SU}; DAT	250[5]	—	100[3,6]	—	ns
Rise time of SDA and SCL signals	t_r	—	1000	20 +0.1C_b[7]	300	ns
Fall time of SDA and SCL signals	t_f	—	300	20 +0.1C_b[6]	300	ns
Set-up time for STOP condition	t_{SU}; STO	4	—	0.6	—	µs
Bus free time between STOP and START condition	t_{BUF}	4.7	—	1.3	—	µs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	N/A	N/A	0	50	ns

1. The maximum SCL Clock Frequency in Fast mode with maximum bus loading can only be achieved when using a pin configured for high drive across the full voltage range and when using the a pin configured for low drive with VDD ≥ 2.7 V.
2. The master mode I^2C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
3. The maximum tHD; DAT must be met only if the device does not stretch the LOW period (tLOW) of the SCL signal.
4. Input signal Slew = 10 ns and Output Load = 50 pF
5. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
6. A Fast mode I^2C bus device can be used in a Standard mode I2C bus system, but the requirement $t_{SU;\ DAT} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a

Table 51. SDHC switching specifications over the full operating voltage range

Num	Symbol	Description	Min.	Max.	Unit
		Operating voltage	1.71	3.6	V
		Card input clock			
SD1	fpp	Clock frequency (low speed)	0	400	kHz
	fpp	Clock frequency (SD\SDIO full speed\high speed)	0	25\50	MHz
	fpp	Clock frequency (MMC full speed\high speed)	0	20\50	MHz
	f_{OD}	Clock frequency (identification mode)	0	400	kHz
SD2	t_{WL}	Clock low time	7	—	ns
SD3	t_{WH}	Clock high time	7	—	ns
SD4	t_{TLH}	Clock rise time	—	3	ns
SD5	t_{THL}	Clock fall time	—	3	ns
		SDHC output / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)			
SD6	t_{OD}	SDHC output delay (output valid)	-5	6.5	ns
		SDHC input / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)			
SD7	t_{ISU}	SDHC input setup time	5	—	ns
SD8	t_{IH}	SDHC input hold time	1.3	—	ns

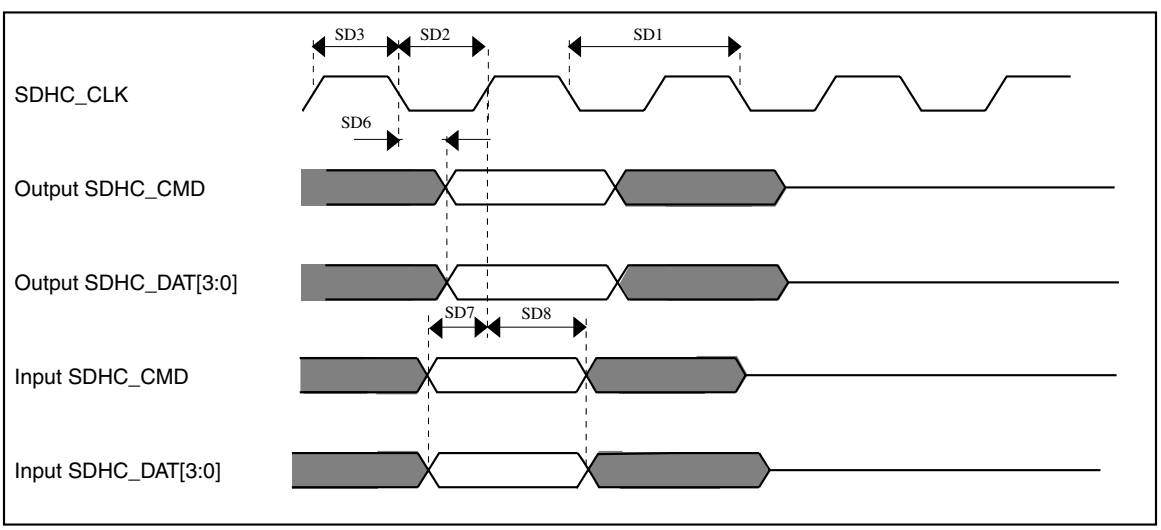

Figure 38. SDHC timing

6.8.12 I2S/SAI switching specifications

This section provides the AC timing for the I2S/SAI module in master mode (clocks are driven) and slave mode (clocks are input). All timing is given for noninverted serial clock polarity (TCR2[BCP] is 0, RCR2[BCP] is 0) and a noninverted frame sync (TCR4[FSP]

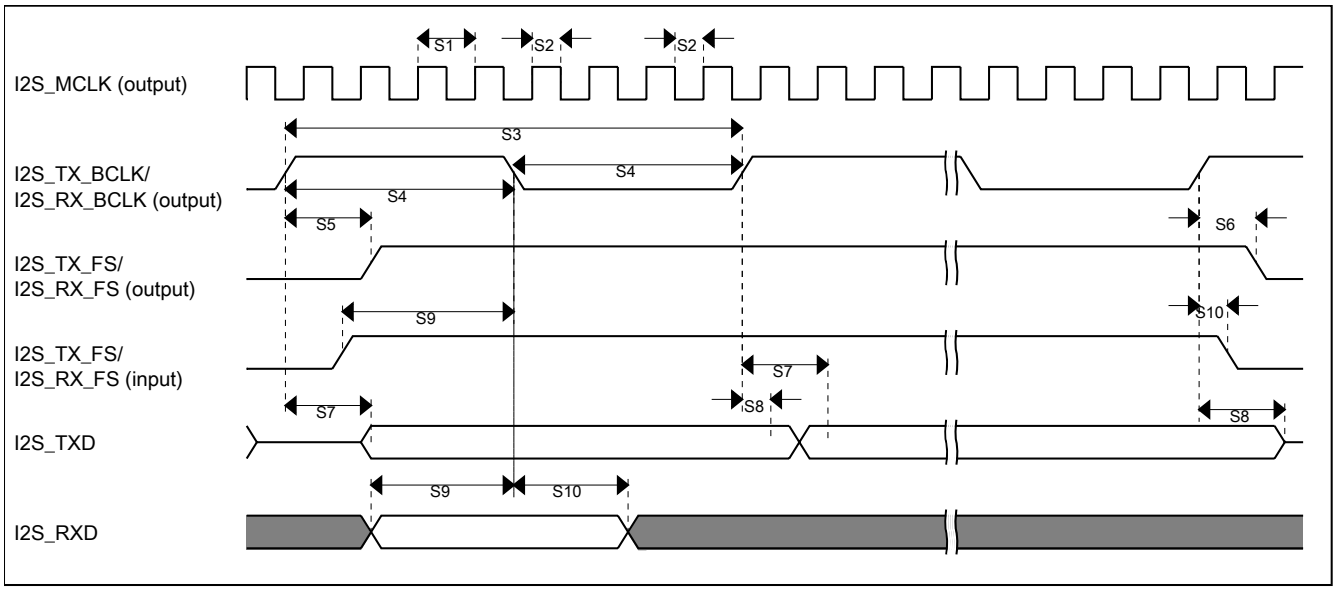

Figure 39. I2S/SAI timing — master modes

Table 53. I2S/SAI slave mode timing in Normal Run, Wait and Stop modes (limited voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	80	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	4.5	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid • Multiple SAI Synchronous mode • All other modes	 — —	 21 15	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	4.5	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid[1]	—	25	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

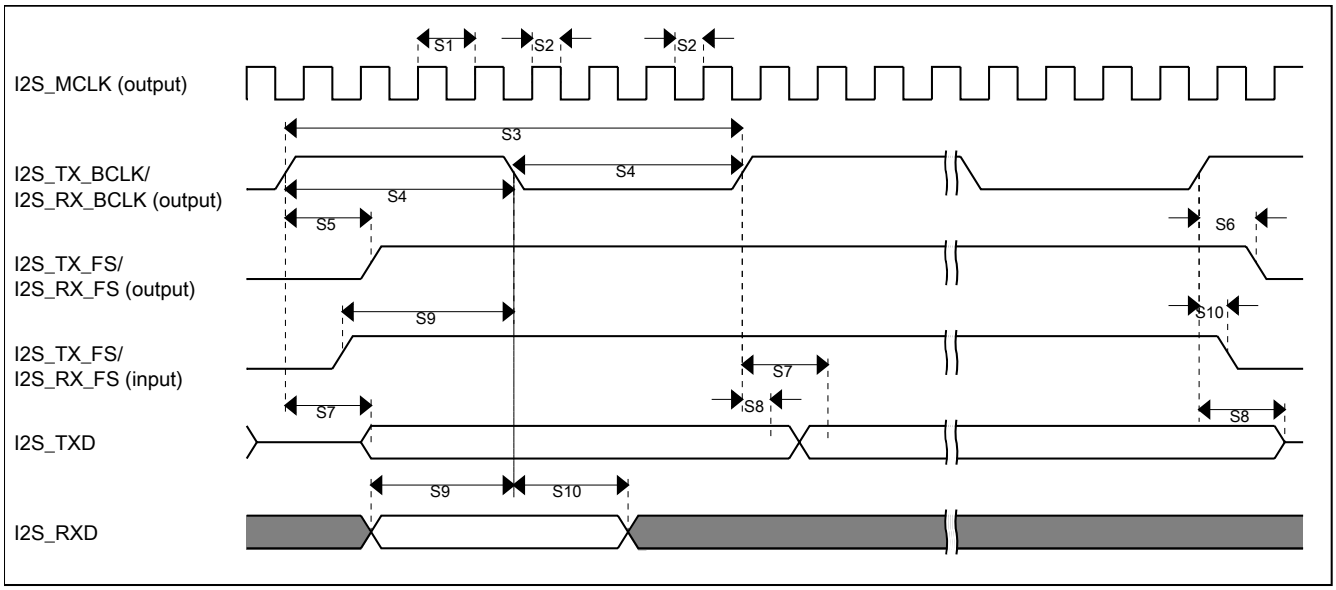

Figure 43. I2S/SAI timing — master modes

Table 57. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	250	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	30	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	3	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	63	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	30	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid[1]	—	72	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

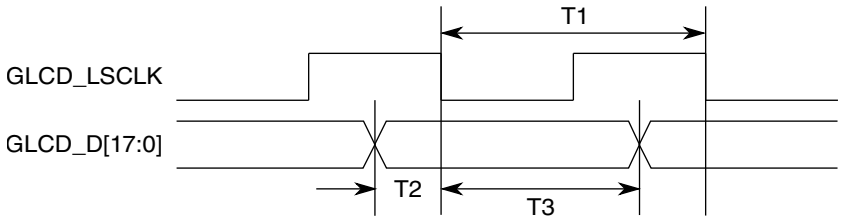

Figure 45. GLCD_LSCLK to GLCD_D[17:0] Timing

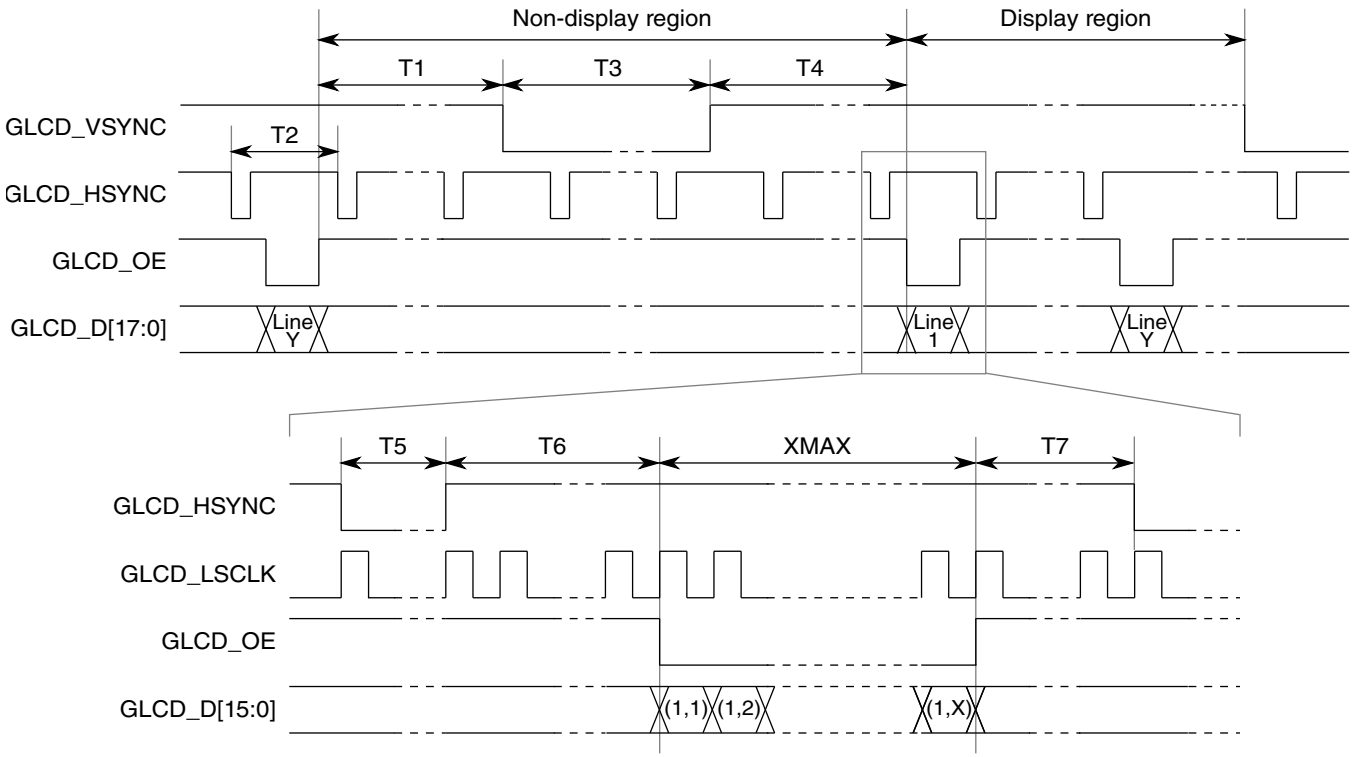

Figure 46. 4/8/12/16/18 Bit/Pixel TFT Color Mode Panel Timing

Table 60. 4/8/12/16/18 Bit/Pixel TFT Color Mode Panel Timing

Num	Description	Min.	Max.	Unit
T1	End of GLCD_OE to beginning of GLCD_VSYNC	T5 + T6 + T7 – 1	(VWAIT1 × T2) + T5 + T6 + T7 – 1	Ts
T2	GLCD_HSYNC period	—	XMAX + T5 + T6 + T7	Ts
T3	GLCD_VSYNC pulse width	T2	VWIDTH × T2	Ts
T4	End of GLCD_VSYNC to beginning of GLCD_OE	1	(VWAIT2 × T2) + 1	Ts
T5	GLCD_HSYNC pulse width	1	HWIDTH + 1	Ts
T6	End of GLCD_HSYNC to beginning to GLCD_OE	3	HWAIT2 + 3	Ts
T7	End of GLCD_OE to beginning of GLCD_HSYNC	1	HWAIT1 + 1	Ts

NOTE

- Ts is the GLCD_LSCLK period. GLCD_VSYNC, GLCD_HSYNC, and GLCD_OE can be programmed as active high or active low. In the preceding figure, all 3 signals are active low. GLCD_LSCLK can be programmed to be deactivated during the GLCD_VSYNC pulse or the GLCD_OE deasserted period. In the preceding figure, GLCD_LSCLK is always active.
- XMAX is defined in number of pixels in one line.

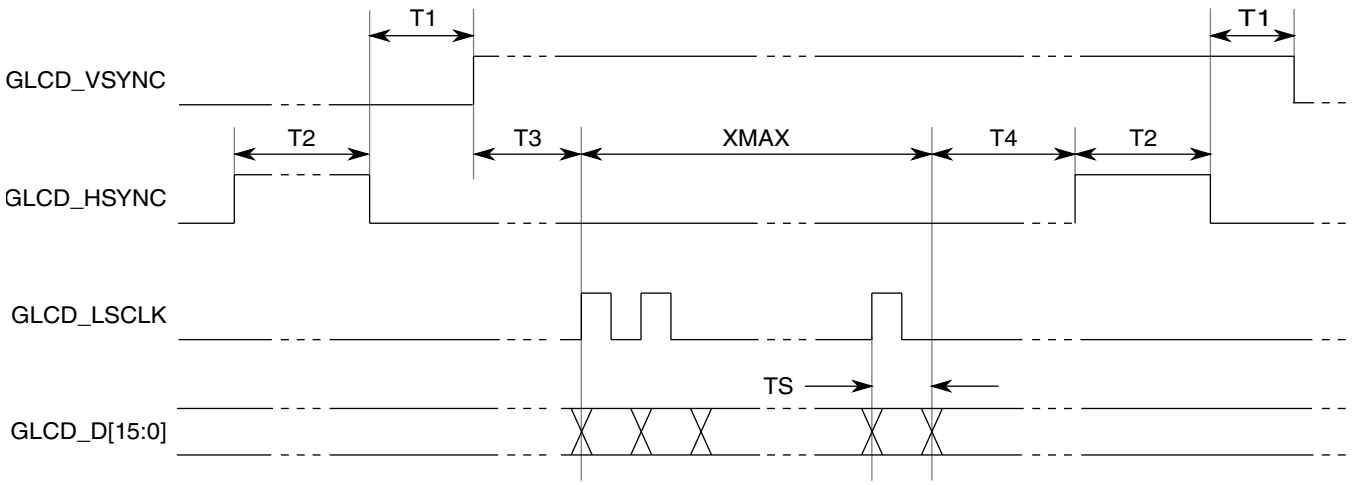

Figure 47. Non-TFT Mode Panel Timing

Table 61. Non-TFT Mode Panel Timing

Num	Description	Min.	Max.	Unit
T1	GLCD_HSYNC to GLCD_VSYNC delay	2	HWAIT2 + 2	Tpix
T2	GLCD_HSYNC pulse width	1	HWIDTH + 1	Tpix
T3	GLCD_VSYNC to GLCD_LSCLK	—	0 ≤ T3 ≤ Ts	—
T4	GLCD_LSCLK to GLCD_HSYNC	1	HWAIT1 + 1	Tpix

NOTE

Ts is the GLCD_LSCLK period while Tpix is the pixel clock period. GLCD_VSYNC, GLCD_HSYNC, and GLCD_LSCLK can be programmed as active high or active low. In the preceding figure, all these 3 signals are active high. When it is in CSTN mode or monochrome mode with bus width = 1, T3 = Tpix = Ts. When it is in monochrome mode with bus width = 2, 4 and 8, T3 = 1, 2 and 4 Tpix respectively.

256 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
N9	PTF22	ADC3_SE7b	ADC3_SE7b	PTF22	I2C0_SCL	FTM1_CH0	UART5_CTS_b			GLCD_D18	
R12	PTA6	ADC3_SE6a	ADC3_SE6a	PTA6	ULPI_CLK	FTM0_CH3	I2S1_RXD0	CLKOUT		TRACE_CLKOUT	
P12	PTA7	ADC0_SE10	ADC0_SE10	PTA7	ULPI_DIR	FTM0_CH4	I2S1_RX_BCLK			TRACE_D3	
N12	PTA8	ADC0_SE11	ADC0_SE11	PTA8	ULPI_NXT	FTM1_CH0	I2S1_RX_FS		FTM1_QD_PHA	TRACE_D2	
T13	PTA9	ADC3_SE5a	ADC3_SE5a	PTA9	ULPI_STP	FTM1_CH1	MII0_RXD3		FTM1_QD_PHB	TRACE_D1	
P13	PTA10	ADC3_SE4a	ADC3_SE4a	PTA10	ULPI_DATA0	FTM2_CH0	MII0_RXD2		FTM2_QD_PHA	TRACE_D0	
R13	PTA11	ADC3_SE15	ADC3_SE15	PTA11	ULPI_DATA1	FTM2_CH1	MII0_RXCLK		FTM2_QD_PHB		
M10	PTA12	CMP2_IN0	CMP2_IN0	PTA12	CAN0_TX	FTM1_CH0	RMII0_RXD1/MII0_RXD1		I2S0_TXD0	FTM1_QD_PHA	
N10	PTA13/LLWU_P4	CMP2_IN1	CMP2_IN1	PTA13/LLWU_P4	CAN0_RX	FTM1_CH1	RMII0_RXD0/MII0_RXD0		I2S0_TX_FS	FTM1_QD_PHB	
R11	PTA14	CMP3_IN0	CMP3_IN0	PTA14	SPI0_PCS0	UART0_TX	RMII0_CRS_DV/MII0_RXDV		I2S0_RX_BCLK	I2S0_TXD1	
P11	PTA15	CMP3_IN1	CMP3_IN1	PTA15	SPI0_SCK	UART0_RX	RMII0_TXEN/MII0_TXEN		I2S0_RXD0		
T14	VSS	VSS	VSS								
N11	PTA16	CMP3_IN2	CMP3_IN2	PTA16	SPI0_SOUT	UART0_CTS_b/UART0_COL_b	RMII0_TXD0/MII0_TXD0		I2S0_RX_FS	I2S0_RXD1	
T11	PTA17	ADC1_SE17	ADC1_SE17	PTA17	SPI0_SIN	UART0_RTS_b	RMII0_TXD1/MII0_TXD1		I2S0_MCLK		
P10	PTF23	ADC3_SE10	ADC3_SE10	PTF23	I2C0_SDA	FTM1_CH1			TRACE_CLKOUT	GLCD_D19	
R10	PTF24	ADC3_SE11	ADC3_SE11	PTF24	CAN1_RX	FTM1_QD_PHA			TRACE_D3	GLCD_D20	
R9	PTF25	ADC3_SE12	ADC3_SE12	PTF25	CAN1_TX	FTM1_QD_PHB			TRACE_D2	GLCD_D21	
T9	PTF26	ADC3_SE13	ADC3_SE13	PTF26		FTM2_QD_PHA			TRACE_D1	GLCD_D22	
T10	PTF27	ADC3_SE14	ADC3_SE14	PTF27		FTM2_QD_PHB			TRACE_D0	GLCD_D23	
J7	VDD	VDD	VDD								
K8	VSS	VSS	VSS								
T15	PTA18	EXTAL0	EXTAL0	PTA18		FTM0_FLT2	FTM_CLKIN0				
T16	PTA19	XTAL0	XTAL0	PTA19		FTM1_FLT0	FTM_CLKIN1		LPTMR0_ALT1		
R16	RESET_b	RESET_b	RESET_b								
N13	PTA24	CMP3_IN4	CMP3_IN4	PTA24	ULPI_DATA2		MII0_TXD2		FB_A29		