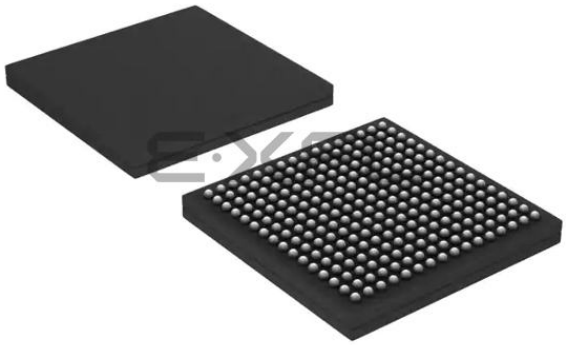

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, SD, SPI, UART/USART, USB, USB OTG
Peripherals	DMA, I²S, LCD, LVD, POR, PWM, WDT
Number of I/O	128
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 71x16b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	256-LBGA
Supplier Device Package	256-MAPPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk70fx512vmj12

4.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I_{LAT}	Latch-up current at ambient temperature of 105°C	-100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

4.4 Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage[1]	–0.3	3.8	V
V_{DD_INT}	Core supply voltage	–0.3	3.8	V
V_{DD_DDR}	DDR I/O supply voltage	–0.3	3.8	V
I_{DD}	Digital supply current	—	300	mA
I_{DD_INT}	Core supply current	—	185	mA
I_{DD_DDR}	DDR supply current	—	220	mA
V_{DIO}	Digital input voltage (except $\overline{\text{RESET}}$, EXTAL0/XTAL0, and EXTAL1/XTAL1) [2]	–0.3	5.5	V
V_{DDDR}	DDR input voltage	–0.3	V_{DD_DDR} + 0.3	V
V_{AIO}	Analog[3], $\overline{\text{RESET}}$, EXTAL0/XTAL0, and EXTAL1/XTAL1 input voltage	–0.3	V_{DD} + 0.3	V
I_D	Maximum current single pin limit (applies to all digital pins)	–25	25	mA
V_{DDA}	Analog supply voltage	V_{DD} – 0.3	V_{DD} + 0.3	V
V_{USB0_DP}	USB0_DP input voltage	–0.3	3.63	V
V_{USB1_DP}	USB1_DP input voltage	–0.3	3.63	V

Table continues on the next page...

5.2.1 Voltage and current operating requirements

Table 1. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	max [V_{DD_DDR}, 1.71 V]	3.6	V	
V_{DD_INT}	Core supply voltage	1.71	V_{DD}	V	
V_{DD_DDR}	DDR voltage — memory I/O buffers • DDR1 • DDR2/LPDDR1	 2.3 1.71	 2.7 1.9	 V V	
V_{REF_DDR}	Input reference voltage (DDR1/DDR2/ LPDDR1)	0.49 × V_{DD_DDR}	V_{DD_DDR}	V	1
V_{DDA}	Analog supply voltage	1.71	3.6	V	
$V_{DD} – V_{DDA}$	V_{DD}-to-V_{DDA} differential voltage	–0.1	0.1	V	
$V_{SS} – V_{SSA}$	V_{SS}-to-V_{SSA} differential voltage	–0.1	0.1	V	
V_{BAT}	RTC battery supply voltage	1.71	3.6	V	
V_{IH}	Input high voltage (digital pins except Tamper pins and DDR pins) • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V	 0.7 × V_{DD} 0.75 × V_{DD}	 — —	 V V	
V_{IL}	Input low voltage (digital pins except Tamper pins and DDR pins) • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V	 — —	 0.35 × V_{DD} 0.3 × V_{DD}	 V V	
V_{IH_DDR}	Input high voltage (DDR pins) • DDR1 • DDR2 • LPDDR1	 V_{REF_DDR} + 0.15 V_{REF_DDR} + 0.125 0.7 × V_{DD_DDR}	 — — —	 V V V	
V_{IL_DDR}	Input low voltage (DDR pins) • DDR1 • DDR2 • LPDDR1	 — — —	 V_{REF_DDR} – 0.15 V_{REF_DDR} – 0.125 0.3 × V_{DD_DDR}	 V V V	
V_{HYS}	Input hysteresis (digital pins except Tamper pins and DDR pins)	0.06 × V_{DD}	—	V	
I_{ICDIO}	Digital pin (except Tamper pins) negative DC injection current — single pin • V_{IN} < V_{SS}-0.3V	-5	—	mA	2
I_{ICAIO}	Analog[3], EXTAL0/XTAL0, and EXTAL1/ XTAL1 pin DC injection current — single pin • V_{IN} < V_{SS}-0.3V (Negative current injection) • V_{IN} > V_{DD}+0.3V (Positive current injection)	 -5 —	 — +5	mA	4

Table continues on the next page...

Table 1. Voltage and current operating requirements (continued)

Symbol	Description	Min.	Max.	Unit	Notes
I_{ICcont}	Contiguous pin DC injection current — regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins • Negative current injection • Positive current injection	 -25 —	 — +25	mA	
V_{ODPU}	Open drain pullup voltage level	V_{DD}	V_{DD}	V	5
V_{RAM}	V_{DD} (V_{DD_INT}) voltage required to retain RAM	1.2	—	V	
V_{RFVBAT}	V_{BAT} voltage required to retain the VBAT register file	V_{POR_VBAT}	—	V	

1. For DDR1/DDR2, connect V_{REF_DDR} to the same reference voltage used for the memory. For LPDDR1, connect V_{REF_DDR} to the V_{DD_DDR} voltage.
2. All 5 V tolerant digital I/O pins are internally clamped to V_{SS} through an ESD protection diode. There is no diode connection to V_{DD}. If V_{IN} is less than V_{DIO_MIN}, a current limiting resistor is required. If V_{IN} greater than V_{DIO_MIN} (=VSS-0.3V) is observed, then there is no need to provide current limiting resistors at the pads. The negative DC injection current limiting resistor is calculated as $R=(V_{DIO\_MIN}-V_{IN})/|I_{ICDIO}|$.
3. Analog pins are defined as pins that do not have an associated general purpose I/O port function. Additionally, EXTAL and XTAL are analog pins.
4. All analog pins are internally clamped to V_{SS} and V_{DD} through ESD protection diodes. If V_{IN} is less than V_{AIO_MIN} or greater than V_{AIO_MAX}, a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R=(V_{AIO\_MIN}-V_{IN})/|I_{ICAIO}|$. The positive injection current limiting resistor is calculated as $R=(V_{IN}-V_{AIO\_MAX})/|I_{ICAIO}|$. Select the larger of these two calculated resistances if the pin is exposed to positive and negative injection currents.
5. Open drain outputs must be pulled to VDD.

5.2.2 LVD and POR operating requirements

Table 2. LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Falling VDD POR detect voltage	0.8	1.1	1.5	V	
V_{LVDH}	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	
 V_{LVW1H} V_{LVW2H} V_{LVW3H} V_{LVW4H}	Low-voltage warning thresholds — high range • Level 1 falling (LVWV=00) • Level 2 falling (LVWV=01) • Level 3 falling (LVWV=10) • Level 4 falling (LVWV=11)	 2.62 2.72 2.82 2.92	 2.70 2.80 2.90 3.00	 2.78 2.88 2.98 3.08	 V V V V	1
V_{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	±80	—	mV	
V_{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
 V_{LVW1L} V_{LVW2L}	Low-voltage warning thresholds — low range • Level 1 falling (LVWV=00)	 1.74 1.84	 1.80 1.90	 1.86 1.96	 V V	1

Table continues on the next page...

Table 4. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{OL_Tamper}	Output low current total for Tamper pins	—	—	100	mA	
I_{INA}	Input leakage current, analog pins and digital pins configured as analog inputs • $V_{SS} \le V_{IN} \le V_{DD}$ • All pins except EXTAL32, XTAL32, EXTAL, XTAL • EXTAL (PTA18) and XTAL (PTA19) • EXTAL32, XTAL32	 — — —	 0.002 0.004 0.075	 0.5 1.5 10	 µA µA µA	1, 2
I_{IND}	Input leakage current, digital pins • $V_{SS} \le V_{IN} \le V_{IL}$ • All digital pins • $V_{IN} = V_{DD}$ • All digital pins except PTD7 • PTD7	 — — —	 0.002 0.002 0.004	 0.5 0.5 1	 µA µA µA	2, 3
I_{IND}	Input leakage current, digital pins • $V_{IL} < V_{IN} < V_{DD}$ • V_{DD} = 3.6 V • V_{DD} = 3.0 V • V_{DD} = 2.5 V • V_{DD} = 1.7 V	 — — — —	 18 12 8 3	 26 19 13 6	 µA µA µA µA	2, 3, 4
I_{IND}	Input leakage current, digital pins • $V_{DD} < V_{IN} < 5.5$ V	 —	 1	 50	 µA	2, 3
Z_{IND}	Input impedance examples, digital pins • V_{DD} = 3.6 V • V_{DD} = 3.0 V • V_{DD} = 2.5 V • V_{DD} = 1.7 V	 — — — —	 — — — —	 48 55 57 85	 kΩ kΩ kΩ kΩ	2, 5
I_{IN_DDR}	Input leakage current (per DDR pin) for full temperature range	—	—	1	µA	
I_{IN_DDR}	Input leakage current (per DDR pin) at 25°C	—	—	0.025	µA	
I_{IN_Tamper}	Input leakage current (per Tamper pin) for full temperature range	—	—	1	µA	
I_{IN_Tamper}	Input leakage current (per Tamper pin) at 25°C	—	—	0.025	µA	
R_{PU}	Internal pullup resistors (except Tamper pins)	20	—	50	kΩ	6
R_{PD}	Internal pulldown resistors (except Tamper pins)	20	—	50	kΩ	7
R_{ODT}	On-die termination (ODT) resistance for DDR2 • $R_{tt1(eff)}$ - 75 Ω • $R_{tt2(eff)}$ - 150 Ω	60 120	— —	90 180	Ω Ω	

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.
2. Digital pins have an associated GPIO port function and have 5V tolerant inputs, except EXTAL and XTAL.
3. Internal pull-up/pull-down resistors disabled.
4. Characterized, not tested in production.
5. Examples calculated using V_{IL} relation, V_{DD}, and max I_{IND}: $Z_{IND}=V_{IL}/I_{IND}$. This is the impedance needed to pull a high signal to a level below V_{IL} due to leakage when $V_{IL} < V_{IN} < V_{DD}$. These examples assume signal source low = 0 V. See Figure 2.
6. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{SS}
7. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{DD}

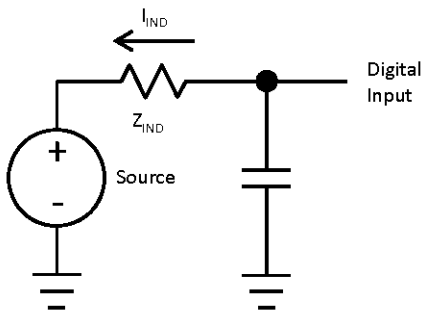

Figure 2. 5 V Tolerant Input IIND Parameter

5.2.4 Power mode transition operating behaviors

All specifications except t_{POR}, and VLLSx→RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 100 MHz
- Bus clock = 50 MHz
- FlexBus clock = 50 MHz
- Flash clock = 25 MHz
- MCG mode: FEI

Table 5. Power mode transition operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip. • V_{DD} slew rate ≥ 5.7 kV/s • V_{DD} slew rate < 5.7 kV/s	 — —	 300 1.7 V / (V_{DD} slew rate)	µs	1
	• VLLS1 → RUN	—	160	µs	
	• VLLS2 → RUN	—	114	µs	

Table continues on the next page...

4. Proper PC board layout procedures must be followed to achieve specifications.
5. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

NOTE

The 32 kHz oscillator works in low power mode by default and cannot be moved into high power/gain mode.

6.3.3 32 kHz oscillator electrical characteristics

6.3.3.1 32 kHz oscillator DC electrical specifications

Table 18. 32kHz oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{BAT}	Supply voltage	1.71	—	3.6	V
R_F	Internal feedback resistor	—	100	—	MΩ
C_{para}	Parasitical capacitance of EXTAL32 and XTAL32	—	5	7	pF
V_{pp}[1]	Peak-to-peak amplitude of oscillation	—	0.6	—	V

1. When a crystal is being used with the 32 kHz oscillator, the EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.

6.3.3.2 32 kHz oscillator frequency specifications

Table 19. 32 kHz oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal	—	32.768	—	kHz	
t_{start}	Crystal start-up time	—	1000	—	ms	1
$v_{ec\_extal32}$	Externally provided input clock amplitude	700	—	V_{BAT}	mV	2, 3

1. Proper PC board layout procedures must be followed to achieve specifications.
2. This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The oscillator remains enabled and XTAL32 must be left unconnected.
3. The parameter specified is a peak-to-peak value and V_{IH} and V_{IL} specifications do not apply. The voltage of the applied clock must be within the range of V_{SS} to V_{BAT}.

6.4 Memories and memory interfaces

6.4.1 Flash (FTFE) electrical specifications

This section describes the electrical characteristics of the FTFE module.

6.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 20. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{hvpgm8}	Program Phrase high-voltage time	—	7.5	18	µs	
$t_{hversscr}$	Erase Flash Sector high-voltage time	—	13	113	ms	1
$t_{hversblk128k}$	Erase Flash Block high-voltage time for 128 KB	—	104	1808	ms	1
$t_{hversblk256k}$	Erase Flash Block high-voltage time for 256 KB	—	208	3616	ms	1

1. Maximum time based on expectations at cycling end-of-life.

6.4.1.2 Flash timing specifications — commands

Table 21. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	Read 1s Block execution time					
$t_{rd1blk128k}$	• 128 KB data flash	—	—	0.5	ms	
$t_{rd1blk256k}$	• 256 KB program flash	—	—	1.0	ms	
	256 KB data flash					
$t_{rd1sec4k}$	Read 1s Section execution time (4 KB flash)	—	—	100	µs	1
t_{pgmchk}	Program Check execution time	—	—	80	µs	1
t_{rdrsrc}	Read Resource execution time	—	—	40	µs	1
t_{pgm8}	Program Phrase execution time	—	70	150	µs	
	Erase Flash Block execution time					2
$t_{ersblk128k}$	• 128 KB data flash	—	110	925	ms	
$t_{ersblk256k}$	• 256 KB program flash	—	220	1850	ms	
	256 KB data flash					
t_{ersscr}	Erase Flash Sector execution time	—	15	115	ms	2
$t_{pgmsec4k}$	Program Section execution time (4KB flash)	—	20	—	ms	
	Read 1s All Blocks execution time					
$t_{rd1allx}$	• FlexNVM devices	—	—	3.4	ms	
$t_{rd1alln}$	• Program flash only devices	—	—	3.4	ms	
t_{rdonce}	Read Once execution time	—	—	30	µs	1
$t_{pgmonce}$	Program Once execution time	—	70	—	µs	
t_{ersall}	Erase All Blocks execution time	—	650	5600	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	µs	1
	Swap Control execution time					

Table continues on the next page...

6.4.1.5 Write endurance to FlexRAM for EEPROM

When the FlexNVM partition code is not set to full data flash, the EEPROM data set size can be set to any of several non-zero values.

The bytes not assigned to data flash via the FlexNVM partition code are used by the FTFE to obtain an effective endurance increase for the EEPROM data. The built-in EEPROM record management system raises the number of program/erase cycles that can be attained prior to device wear-out by cycling the EEPROM data through a larger EEPROM NVM storage space.

While different partitions of the FlexNVM are available, the intention is that a single choice for the FlexNVM partition code and EEPROM data set size is used throughout the entire lifetime of a given application. The EEPROM endurance equation and graph shown below assume that only one configuration is ever used.

$$\text{Writes\_subsystem} = \frac{\text{EEPROM} - 2 \times \text{EEESPLIT} \times \text{EEESIZE}}{\text{EEESPLIT} \times \text{EEESIZE}} \times \text{Write\_efficiency} \times n_{\text{nvmcycee}}$$

where

- Writes_subsystem — minimum number of writes to each FlexRAM location for subsystem (each subsystem can have different endurance)
- EEPROM — allocated FlexNVM for each EEPROM subsystem based on DEPART; entered with the Program Partition command
- EEESPLIT — FlexRAM split factor for subsystem; entered with the Program Partition command
- EEESIZE — allocated FlexRAM based on DEPART; entered with the Program Partition command
- Write_efficiency —
  - 0.25 for 8-bit writes to FlexRAM
  - 0.50 for 16-bit or 32-bit writes to FlexRAM
- $n_{nvmcycee}$ — EEPROM-backup cycling endurance

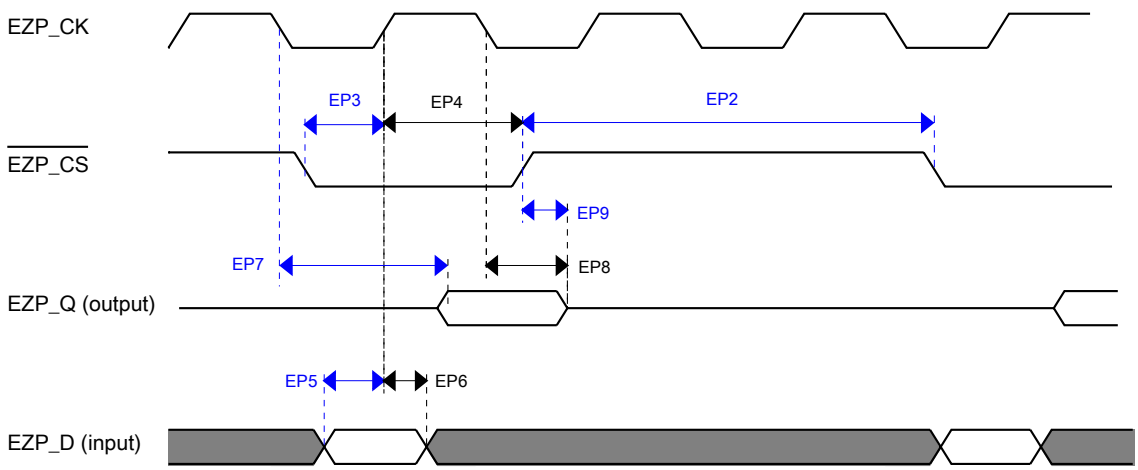

Figure 12. EzPort Timing Diagram

6.4.3 NFC specifications

The NAND flash controller (NFC) implements the interface to standard NAND flash memory devices. This section describes the timing parameters of the NFC.

In the following table:

- T_H is the flash clock high time and
- T_L is flash clock low time,

which are defined as:

$$T_{NFC} = T_L + T_H = \frac{T_{input\ clock}}{SCALER}$$

The SCALER value is derived from the fractional divider specified in the SIM's CLKDIV4 register:

$$SCALER = \frac{SIM\_CLKDIV4[NFCFRAC] + 1}{SIM\_CLKDIV4[NFCDIV] + 1}$$

In case the reciprocal of SCALER is an integer, the duty cycle of NFC clock is 50%, means $T_H = T_L$. In case the reciprocal of SCALER is not an integer:

$$T_L = (1 + SCALER / 2) \times \frac{T_{NFC}}{2}$$

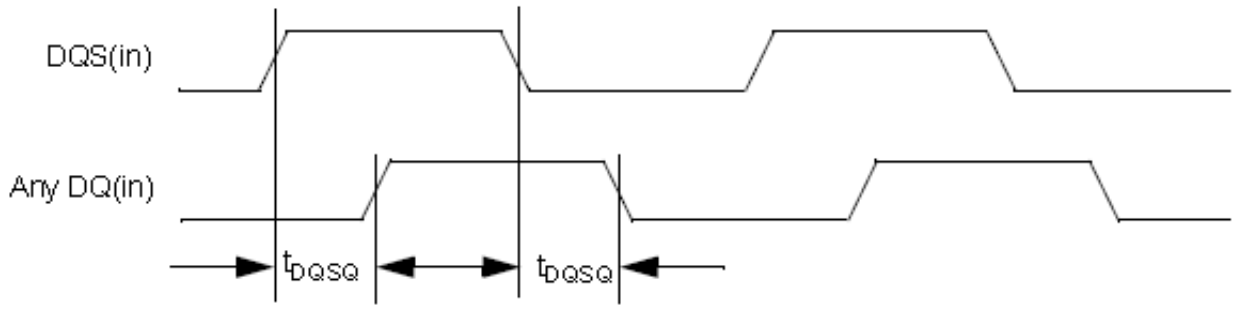

Figure 20. DDR read timing, DQ vs. DQS

6.4.5 Flexbus switching specifications

All processor bus timings are synchronous; input setup/hold and output delay are given in respect to the rising edge of a reference clock, FB_CLK. The FB_CLK frequency may be the same as the internal system bus frequency or an integer divider of that frequency.

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the Flexbus output clock (FB_CLK). All other timing relationships can be derived from these values.

Table 27. Flexbus limited voltage range switching specifications

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	FB_CLK	MHz	
FB1	Clock period	20	—	ns	
FB2	Address, data, and control output valid	—	11.5	ns	1
FB3	Address, data, and control output hold	0.5	—	ns	1
FB4	Data and $\overline{\text{FB\_TA}}$ input setup	8.5	—	ns	2
FB5	Data and $\overline{\text{FB\_TA}}$ input hold	0.5	—	ns	2

1. Specification is valid for all FB_AD[31:0], $\overline{\text{FB\_BE/BWE}n}$, $\overline{\text{FB\_CS}n}$, $\overline{\text{FB\_OE}}$, FB_R/$\overline{\text{W}}$,$\overline{\text{FB\_TBST}}$, FB_TSIZ[1:0], FB_ALE, and $\overline{\text{FB\_TS}}$.
2. Specification is valid for all FB_AD[31:0] and $\overline{\text{FB\_TA}}$.

Table 28. Flexbus full voltage range switching specifications

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	
	Frequency of operation	—	FB_CLK	MHz	
FB1	Clock period	1/FB_CLK	—	ns	
FB2	Address, data, and control output valid	—	13.5	ns	1
FB3	Address, data, and control output hold	0	—	ns	1

Table continues on the next page...

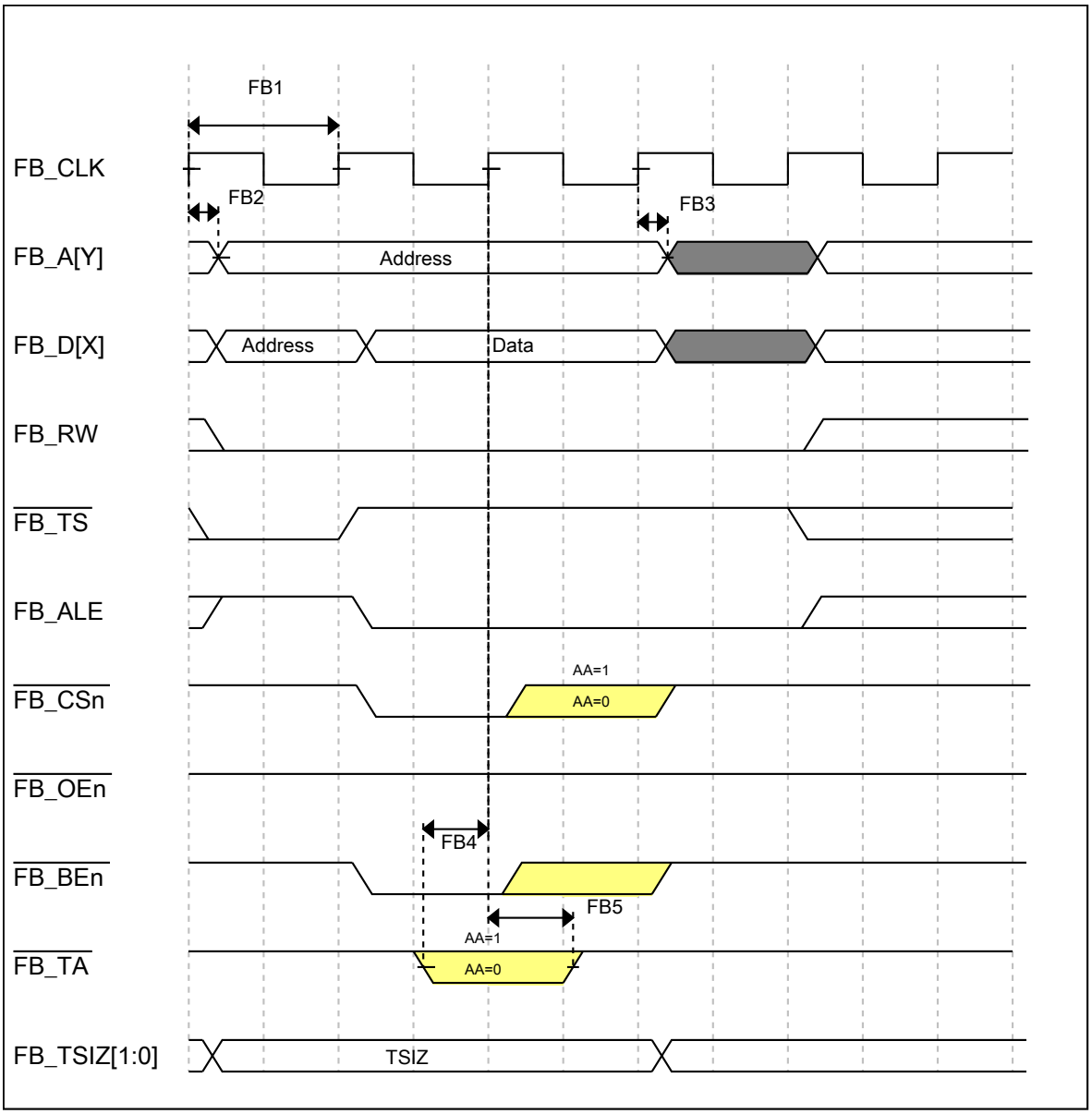

Figure 22. FlexBus write timing diagram

6.5 Security and integrity modules

6.5.1 DryIce Tamper Electrical Specifications

Information about security-related modules is not included in this document and is available only after a nondisclosure agreement (NDA) has been signed. To request an NDA, please contact your local Freescale sales representative.

Table 29. 16-bit ADC operating conditions (continued)

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
		No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	20.000	—	818.330	ksps	
C_{rate}	ADC conversion rate	16-bit mode No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	37.037	—	461.467	ksps	5

1. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.
3. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 8 Ω analog source resistance. The R_{AS}/C_{AS} time constant should be kept to < 1 ns.
4. To use the maximum ADC conversion clock frequency, CFG2[ADHSC] must be set and CFG1[ADLPC] must be clear.
5. For guidelines and examples of conversion rate calculation, download the ADC calculator tool.

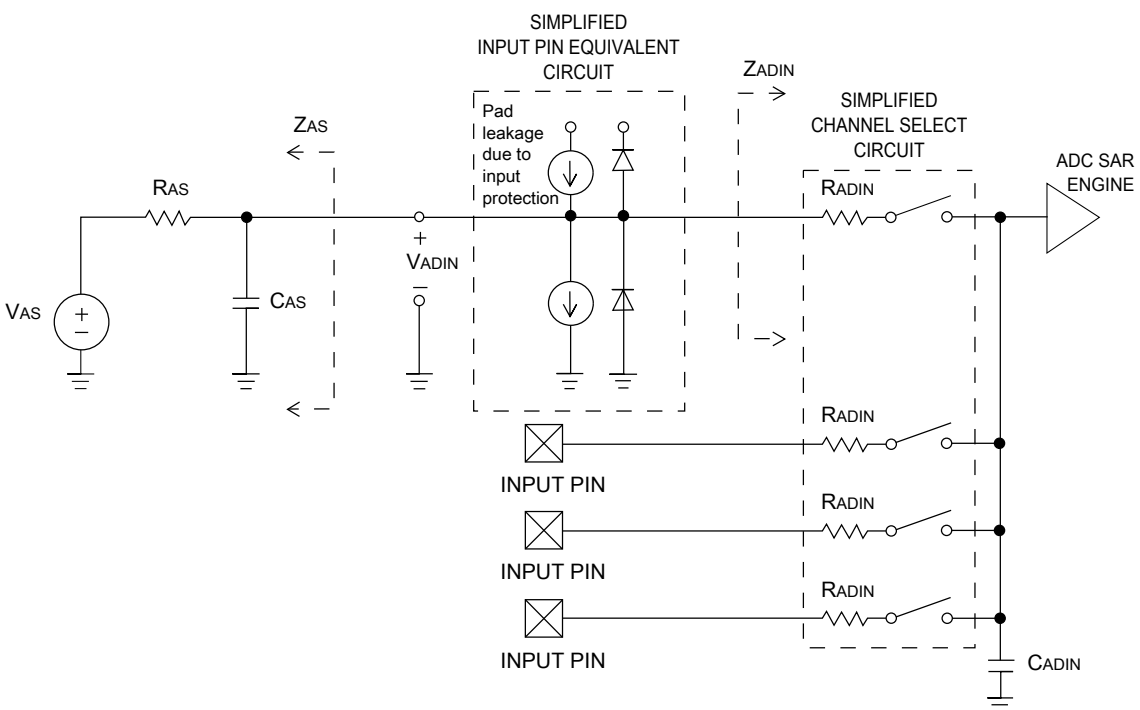

Figure 23. ADC input impedance equivalency diagram

6.6.1.2 16-bit ADC electrical characteristics

Table 33. Comparator and 6-bit DAC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
INL	6-bit DAC integral non-linearity	–0.5	—	0.5	LSB[3]
DNL	6-bit DAC differential non-linearity	–0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.6 to V_{DD}–0.6 V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to CMP_DACCR[DACEN], CMP_DACCR[VRSEL], CMP_DACCR[VOSEL], CMP_MUXCR[PSEL], and CMP_MUXCR[MSEL]) and the comparator output settling to a stable level.
3. 1 LSB = $V_{reference}$/64

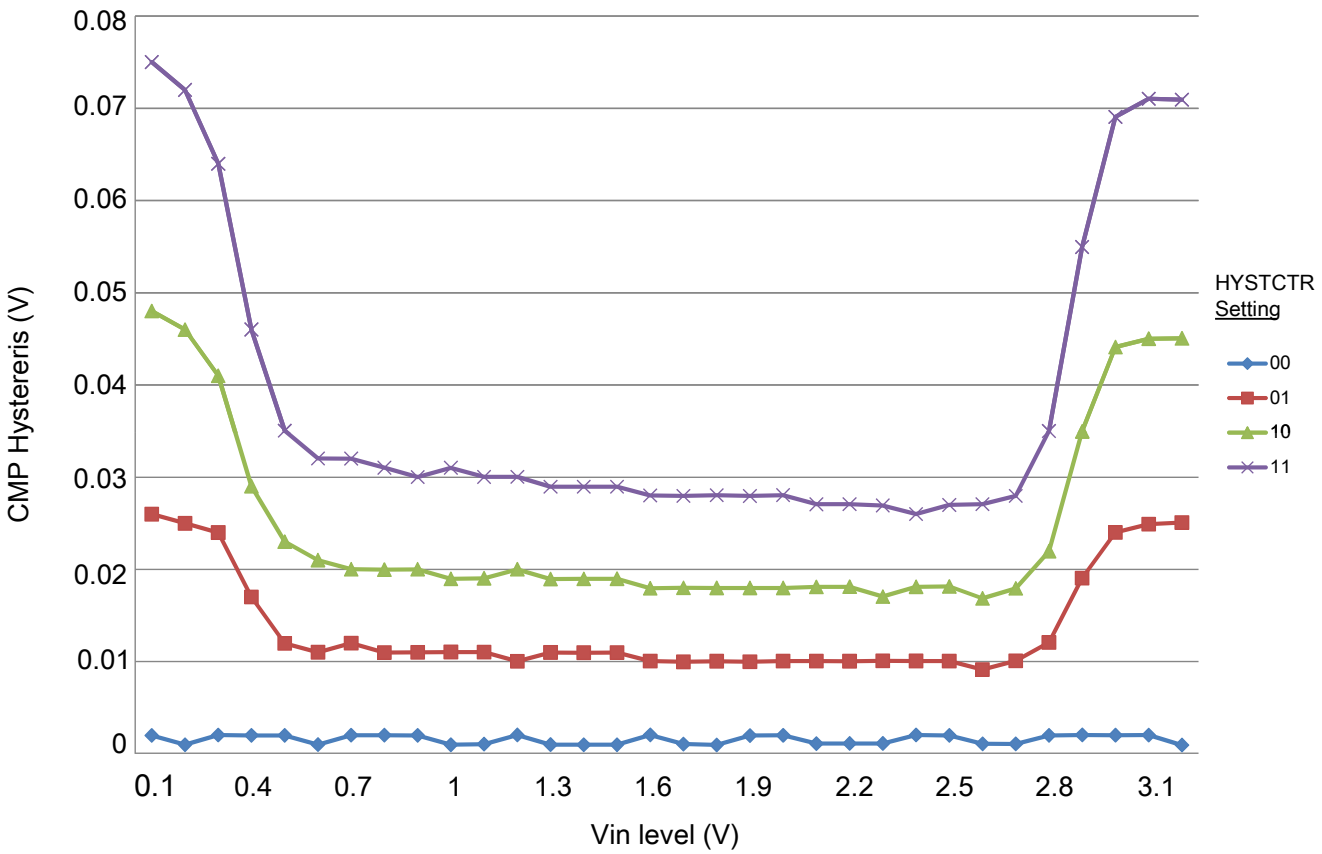

Figure 26. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 0)

Table 47. Master mode DSPI timing (full voltage range) (continued)

Num	Description	Min.	Max.	Unit	Notes
DS2	DSPI_SCK output high/low time	(t_{SCK}/2) - 4	($t_{SCK/2}$) + 4	ns	
DS3	DSPI_PCS*n* valid to DSPI_SCK delay	(t_{BUS} x 2) – 4	—	ns	2
DS4	DSPI_SCK to DSPI_PCS*n* invalid delay	(t_{BUS} x 2) – 4	—	ns	3
DS5	DSPI_SCK to DSPI_SOUT valid	—	10	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-4.5	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	20.5	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.
2. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
3. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

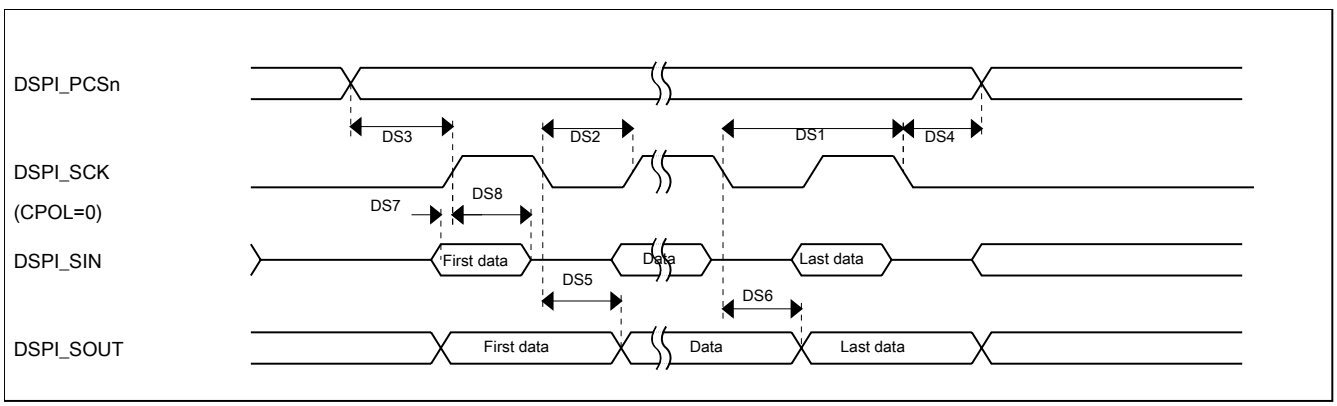

Figure 35. DSPI classic SPI timing — master mode

Table 48. Slave mode DSPI timing (full voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
	Frequency of operation	—	7.5	MHz
DS9	DSPI_SCK input cycle time	8 x t_{BUS}	—	ns
DS10	DSPI_SCK input high/low time	(t_{SCK}/2) - 4	($t_{SCK/2}$) + 4	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	20	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	19	ns
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	19	ns

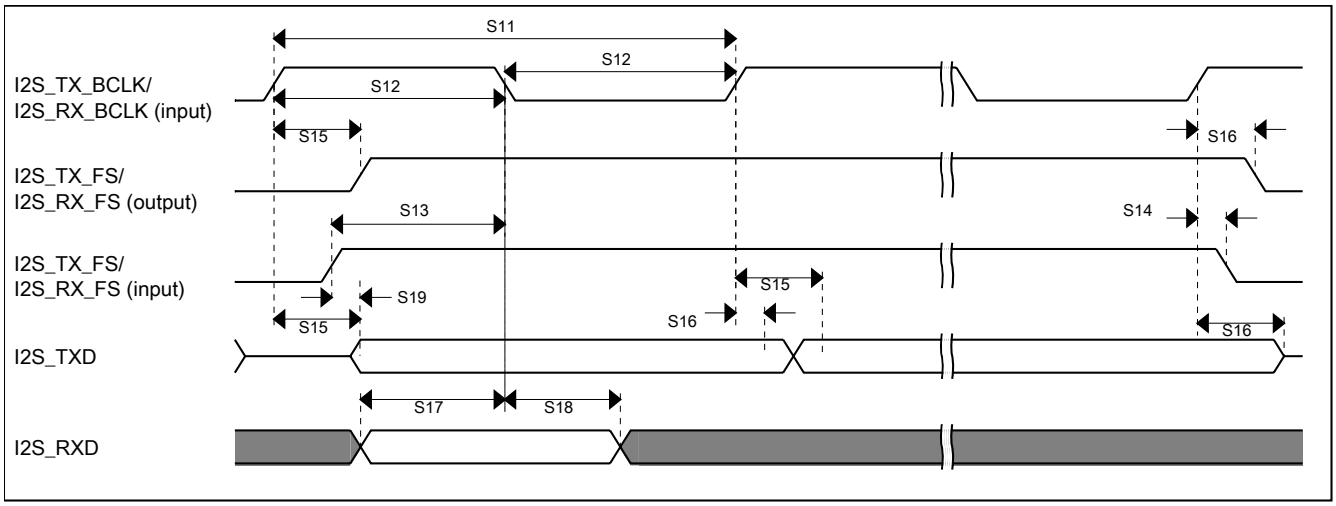

Figure 42. I2S/SAI timing — slave modes

6.8.12.3 VLPR, VLPW, and VLPS mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in VLPR, VLPW, and VLPS modes.

Table 56. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	62.5	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	250	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	45	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	45	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	-1.6	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	45	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

NOTE

- Ts is the GLCD_LSCLK period. GLCD_VSYNC, GLCD_HSYNC, and GLCD_OE can be programmed as active high or active low. In the preceding figure, all 3 signals are active low. GLCD_LSCLK can be programmed to be deactivated during the GLCD_VSYNC pulse or the GLCD_OE deasserted period. In the preceding figure, GLCD_LSCLK is always active.
- XMAX is defined in number of pixels in one line.

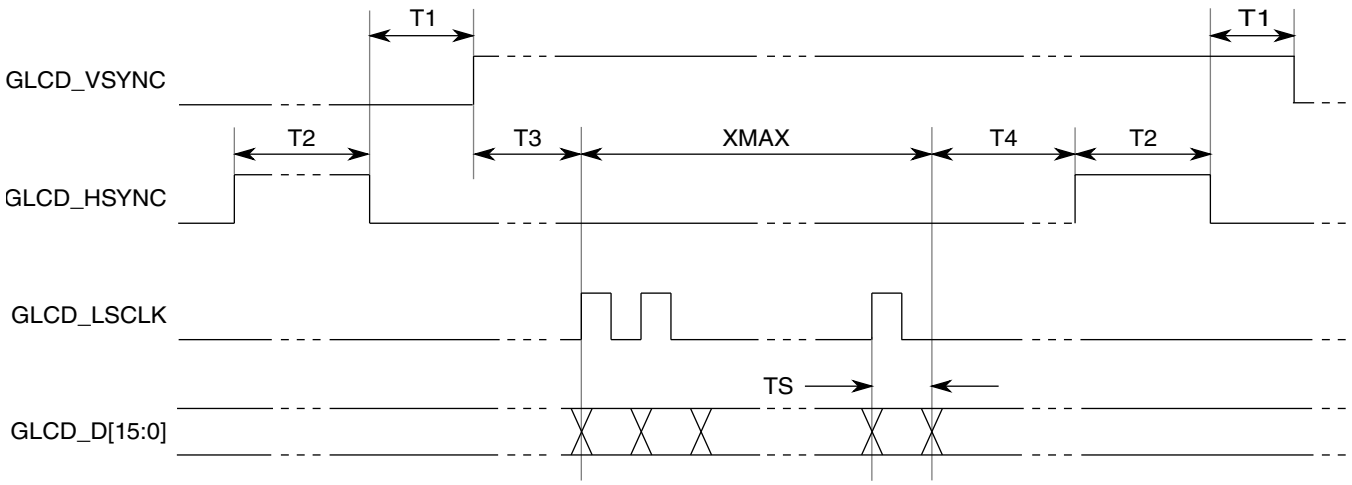

Figure 47. Non-TFT Mode Panel Timing

Table 61. Non-TFT Mode Panel Timing

Num	Description	Min.	Max.	Unit
T1	GLCD_HSYNC to GLCD_VSYNC delay	2	HWAIT2 + 2	Tpix
T2	GLCD_HSYNC pulse width	1	HWIDTH + 1	Tpix
T3	GLCD_VSYNC to GLCD_LSCLK	—	0 ≤ T3 ≤ Ts	—
T4	GLCD_LSCLK to GLCD_HSYNC	1	HWAIT1 + 1	Tpix

NOTE

Ts is the GLCD_LSCLK period while Tpix is the pixel clock period. GLCD_VSYNC, GLCD_HSYNC, and GLCD_LSCLK can be programmed as active high or active low. In the preceding figure, all these 3 signals are active high. When it is in CSTN mode or monochrome mode with bus width = 1, T3 = Tpix = Ts. When it is in monochrome mode with bus width = 2, 4 and 8, T3 = 1, 2 and 4 Tpix respectively.

256 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
K16	PTF5	ADC2_SE5b	ADC2_SE5b	PTF5		FTM3_CH5		I2S1_TX_FS		GLCD_D1	
J16	PTF6	ADC2_SE6b	ADC2_SE6b	PTF6		FTM3_CH6		I2S1_TX_ BCLK		GLCD_D2	
H15	PTB19	TSI0_CH12	TSI0_CH12	PTB19	CAN0_RX	FTM2_CH1	I2S0_TX_FS	FB_OE_b	FTM2_QD_ PHB		
G13	PTB20	ADC2_SE4a	ADC2_SE4a	PTB20	SPI2_PCS0			FB_AD31/ NFC_DATA15	CMP0_OUT		
G14	PTB21	ADC2_SE5a	ADC2_SE5a	PTB21	SPI2_SCK			FB_AD30/ NFC_DATA14	CMP1_OUT		
G15	PTB22	DISABLED		PTB22	SPI2_SOUT			FB_AD29/ NFC_DATA13	CMP2_OUT		
H16	PTB23	DISABLED		PTB23	SPI2_SIN	SPI0_PCS5		FB_AD28/ NFC_DATA12	CMP3_OUT		
G16	PTC0	ADC0_SE14/ TSI0_CH13	ADC0_SE14/ TSI0_CH13	PTC0	SPI0_PCS4	PDB0_EXTRG		FB_AD14/ NFC_DATA11	I2S0_TXD1		
F13	PTC1/ LLWU_P6	ADC0_SE15/ TSI0_CH14	ADC0_SE15/ TSI0_CH14	PTC1/ LLWU_P6	SPI0_PCS3	UART1_RTS_ b	FTM0_CH0	FB_AD13/ NFC_DATA10	I2S0_TXD0		
F14	PTC2	ADC0_SE4b/ CMP1_IN0/ TSI0_CH15	ADC0_SE4b/ CMP1_IN0/ TSI0_CH15	PTC2	SPI0_PCS2	UART1_CTS_ b	FTM0_CH1	FB_AD12/ NFC_DATA9	I2S0_TX_FS		
E13	PTC3/ LLWU_P7	CMP1_IN1	CMP1_IN1	PTC3/ LLWU_P7	SPI0_PCS1	UART1_RX	FTM0_CH2	CLKOUT	I2S0_TX_ BCLK		
F15	PTF7	ADC2_SE7b	ADC2_SE7b	PTF7		FTM3_CH7	UART3_RX	I2S1_TXD1		GLCD_D3	
L9	VSS	VSS	VSS								
K10	VDD	VDD	VDD								
F16	PTF8	DISABLED		PTF8		FTM3_FLT0	UART3_TX	I2S1_MCLK		GLCD_D4	
E14	PTC4/ LLWU_P8	DISABLED		PTC4/ LLWU_P8	SPI0_PCS0	UART1_TX	FTM0_CH3	FB_AD11/ NFC_DATA8	CMP1_OUT	I2S1_TX_ BCLK	
E15	PTC5/ LLWU_P9	DISABLED		PTC5/ LLWU_P9	SPI0_SCK	LPTMR0_ ALT2	I2S0_RXD0	FB_AD10/ NFC_DATA7	CMP0_OUT	I2S1_TX_FS	
F12	PTC6/ LLWU_P10	CMP0_IN0	CMP0_IN0	PTC6/ LLWU_P10	SPI0_SOUT	PDB0_EXTRG	I2S0_RX_ BCLK	FB_AD9/ NFC_DATA6	I2S0_MCLK		
G12	PTC7	CMP0_IN1	CMP0_IN1	PTC7	SPI0_SIN	USB_SOF_ OUT	I2S0_RX_FS	FB_AD8/ NFC_DATA5			
H12	PTC8	ADC1_SE4b/ CMP0_IN2	ADC1_SE4b/ CMP0_IN2	PTC8		FTM3_CH4	I2S0_MCLK	FB_AD7/ NFC_DATA4			
F11	PTC9	ADC1_SE5b/ CMP0_IN3	ADC1_SE5b/ CMP0_IN3	PTC9		FTM3_CH5	I2S0_RX_ BCLK	FB_AD6/ NFC_DATA3	FTM2_FLT0		
G11	PTC10	ADC1_SE6b	ADC1_SE6b	PTC10	I2C1_SCL	FTM3_CH6	I2S0_RX_FS	FB_AD5/ NFC_DATA2	I2S1_MCLK		
H11	PTC11/ LLWU_P11	ADC1_SE7b	ADC1_SE7b	PTC11/ LLWU_P11	I2C1_SDA	FTM3_CH7	I2S0_RXD1	FB_RW_b/ NFC_WE			
J12	PTC12	DISABLED		PTC12		UART4_RTS_ b		FB_AD27	FTM3_FLT0		
K13	PTC13	DISABLED		PTC13		UART4_CTS_ b		FB_AD26			

256 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
J4	PTD8	DISABLED		PTD8	I2C0_SCL	UART5_RX			FB_A16/ NFC_CLE		
F7	PTD9	DISABLED		PTD9	I2C0_SDA	UART5_TX			FB_A17/ NFC_ALE		
E6	PTD10	DISABLED		PTD10		UART5_RTS_b			FB_A18/ NFC_RE		
G5	PTD11	DISABLED		PTD11	SPI2_PCS0	UART5_CTS_b	SDHC0_CLKIN		FB_A19	GLCD_CONTRAST	
F5	PTD12	DISABLED		PTD12	SPI2_SCK	FTM3_FLT0	SDHC0_D4		FB_A20	GLCD_PCLK	
F4	PTD13	DISABLED		PTD13	SPI2_SOUT		SDHC0_D5		FB_A21	GLCD_DE	
E5	PTD14	DISABLED		PTD14	SPI2_SIN		SDHC0_D6		FB_A22	GLCD_HFS	
E4	PTD15	DISABLED		PTD15	SPI2_PCS1		SDHC0_D7		FB_A23	GLCD_VFS	
F6	PTF15	DISABLED		PTF15			UART0_RTS_b			GLCD_D11	
E1	PTF16	DISABLED		PTF16	SPI2_PCS0	FTM0_CH3	UART0_CTS_b/ UART0_COL_b	GLCD_D12			
B1	DDR_VDD	DDR_VDD		DDR_VDD							
A1	DDR_VSS	DDR_VSS		DDR_VSS							
D3	DDR_DQS1	DISABLED		DDR_DQS1							
D1	DDR_DQ8	DISABLED		DDR_DQ8							
C1	DDR_DQ9	DISABLED		DDR_DQ9							
B5	DDR_VDD	DDR_VDD		DDR_VDD							
A5	DDR_VSS	DDR_VSS		DDR_VSS							
D5	DDR_VSS	DDR_VSS		DDR_VSS							
C2	DDR_DQ10	DISABLED		DDR_DQ10							
B2	DDR_DQ11	DISABLED		DDR_DQ11							
C3	DDR_DQ12	DISABLED		DDR_DQ12							
B8	DDR_VDD	DDR_VDD		DDR_VDD							
A12	DDR_VSS	DDR_VSS		DDR_VSS							
C4	DDR_DQ13	DISABLED		DDR_DQ13							
B3	DDR_DQ14	DISABLED		DDR_DQ14							
A2	DDR_DQ15	DISABLED		DDR_DQ15							
A3	DDR_DM1	DISABLED		DDR_DM1							
E8	DDR_VSS	DDR_VSS		DDR_VSS							
B12	DDR_VDD	DDR_VDD		DDR_VDD							
A16	DDR_VSS	DDR_VSS		DDR_VSS							
C6	DDR_VREF	DDR_VREF		DDR_VREF							
C5	DDR_DQ0	DISABLED		DDR_DQ0							
B4	DDR_DQ1	DISABLED		DDR_DQ1							
A4	DDR_DQ2	DISABLED		DDR_DQ2							
C16	DDR_VDD	DDR_VDD		DDR_VDD							

256 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
C7	DDR_VSS	DDR_VSS		DDR_VSS							
B6	DDR_DQ3	DISABLED		DDR_DQ3							
D6	DDR_DQ4	DISABLED		DDR_DQ4							
A6	DDR_DQ5	DISABLED		DDR_DQ5							
A7	DDR_ODT	DISABLED		DDR_ODT							
E11	DDR_VSS	DDR_VSS		DDR_VSS							
D2	DDR_VDD	DDR_VDD		DDR_VDD							
C9	DDR_VSS	DDR_VSS		DDR_VSS							
B7	DDR_DQ6	DISABLED		DDR_DQ6							
A8	DDR_DQ7	DISABLED		DDR_DQ7							
C8	DDR_DQS0	DISABLED		DDR_DQS0							
D9	DDR_DM0	DISABLED		DDR_DM0							
D4	DDR_VDD	DDR_VDD		DDR_VDD							
C14	DDR_VSS	DDR_VSS		DDR_VSS							
A9	DDR_BA0	DISABLED		DDR_BA0							
B10	DDR_BA1	DISABLED		DDR_BA1							
B9	DDR_BA2	DISABLED		DDR_BA2							
A10	DDR_CKB	DISABLED		DDR_CKB							
A11	DDR_CK	DISABLED		DDR_CK							
D7	DDR_VDD	DDR_VDD		DDR_VDD							
D8	DDR_VSS	DDR_VSS		DDR_VSS							
D10	DDR_A0	DISABLED		DDR_A0							
C11	DDR_A1	DISABLED		DDR_A1							
B11	DDR_A2	DISABLED		DDR_A2							
C12	DDR_A3	DISABLED		DDR_A3							
E10	DDR_VDD	DDR_VDD		DDR_VDD							
D12	DDR_VSS	DDR_VSS		DDR_VSS							
C10	DDR_A4	DISABLED		DDR_A4							
A13	DDR_A5	DISABLED		DDR_A5							
A14	DDR_A6	DISABLED		DDR_A6							
D11	DDR_A7	DISABLED		DDR_A7							
A15	DDR_A8	DISABLED		DDR_A8							
E12	DDR_VDD	DDR_VDD		DDR_VDD							
E3	DDR_VSS	DDR_VSS		DDR_VSS							
B16	DDR_CKE	DISABLED		DDR_CKE							
B15	DDR_A9	DISABLED		DDR_A9							
B13	DDR_A10	DISABLED		DDR_A10							
B14	DDR_A11	DISABLED		DDR_A11							
C15	DDR_A12	DISABLED		DDR_A12							
D16	DDR_A13	DISABLED		DDR_A13							