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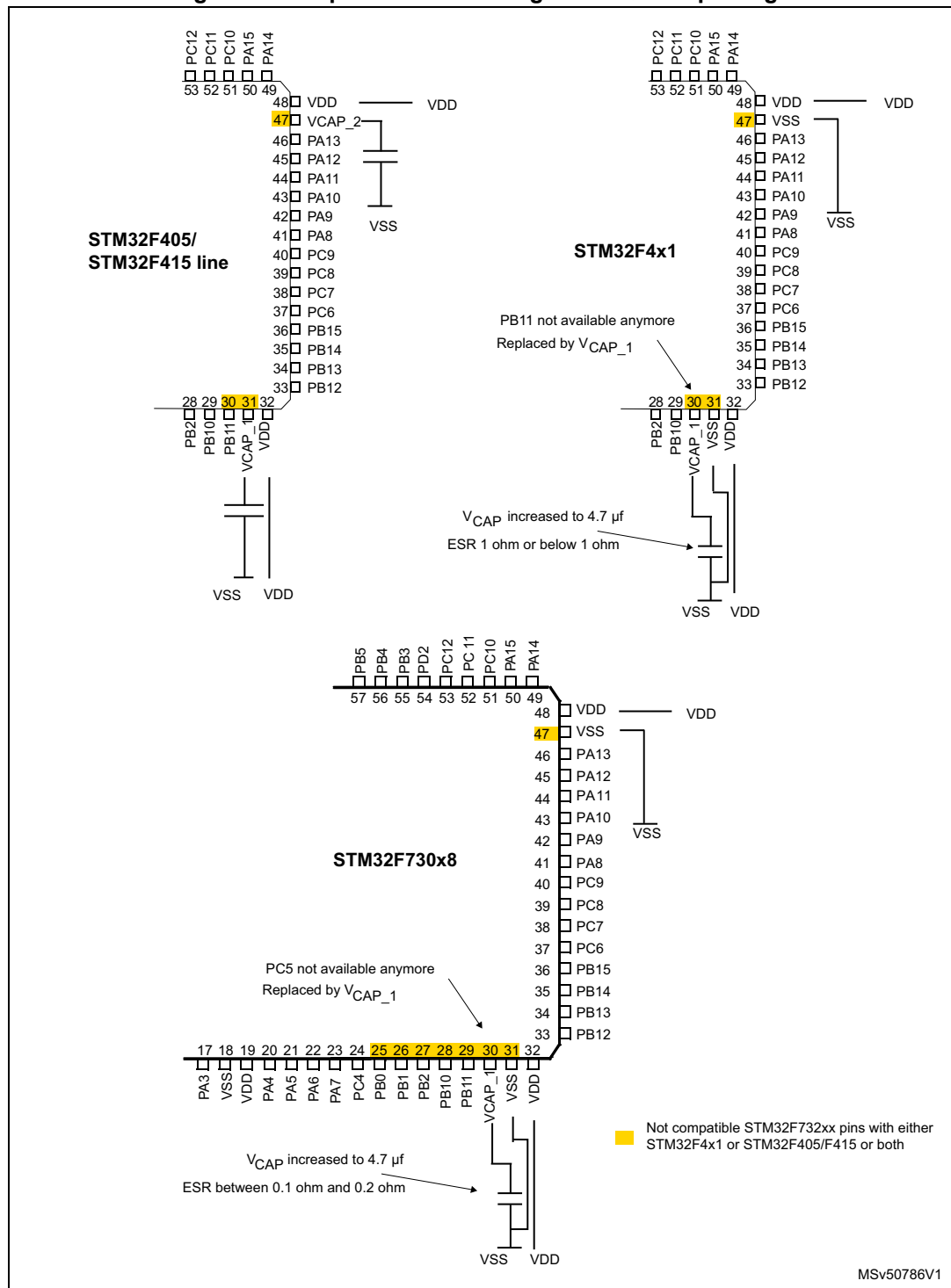
"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	216MHz
Connectivity	CANbus, EBI/EMI, I ² C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	82
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f730v8t6

Figure 2. Compatible board design for LQFP64 package



3.7 DMA controller (DMA)

The devices feature two general-purpose dual-port DMAs (DMA1 and DMA2) with 8 streams each. They are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. They feature dedicated FIFOs for APB/AHB peripherals, support burst transfer and are designed to provide the maximum peripheral bandwidth (AHB/APB).

The two DMA controllers support a circular buffer management, so that no specific code is needed when the controller reaches the end of the buffer. The two DMA controllers also have a double buffering feature, which automates the use and switching of two memory buffers without requiring any special code.

Each stream is connected to dedicated hardware DMA requests, with support for software trigger on each stream. The configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals:

- SPI and I²S
- I²C
- USART
- General-purpose, basic and advanced-control timers TIMx
- DAC
- SDMMC
- ADC
- SAI
- Quad-SPI

3.13 Boot modes

At startup, the boot memory space is selected by the BOOT pin and BOOT_ADDx option bytes, allowing to program any boot memory address from 0x0000 0000 to 0x3FFF FFFF which includes:

- All Flash address space mapped on ITCM or AXIM interface
- All RAM address space: ITCM, DTCM RAMs and SRAMs mapped on AXIM interface
- The System memory bootloader

The boot loader is located in system memory. It is used to reprogram the Flash memory through a serial interface.

3.14 Power supply schemes

- $V_{DD} = 1.7$ to 3.6 V: external power supply for I/Os and the internal regulator (when enabled), provided externally through V_{DD} pins.
- V_{SSA} , $V_{DDA} = 1.7$ to 3.6 V: external analog power supplies for ADC, DAC, Reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS} , respectively.
- $V_{BAT} = 1.65$ to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

Note: The V_{DD}/V_{DDA} minimum value of 1.7 V is obtained when the internal reset is OFF (refer to [Section 3.15.2: Internal reset OFF](#)). Refer to [Table 3: Voltage regulator configuration mode versus device operating mode](#) to identify the packages supporting this option.

- The $V_{DDSDMMC}$ can be connected either to V_{DD} or an external independent power supply (1.8 to 3.6 V) for the SDMMC2 pins (clock, command, and 4-bit data). For example, when the device is powered at 1.8 V, an independent power supply 2.7 V can be connected to $V_{DDSDMMC}$. When the $V_{DDSDMMC}$ is connected to a separated power supply, it is independent from V_{DD} or V_{DDA} but it must be the last supply to be provided and the first to disappear. The following conditions $V_{DDSDMMC}$ must be respected:
 - During the power-on phase ($V_{DD} < V_{DD_MIN}$), $V_{DDSDMMC}$ should be always lower than V_{DD}
 - During the power-down phase ($V_{DD} < V_{DD_MIN}$), $V_{DDSDMMC}$ should be always lower than V_{DD}
 - The $V_{DDSDMMC}$ rising and falling time rate specifications must be respected
 - In the operating mode phase, $V_{DDSDMMC}$ could be lower or higher than V_{DD} : All associated GPIOs powered by $V_{DDSDMMC}$ are operating between $V_{DDSDMMC_MIN}$ and $V_{DDSDMMC_MAX}$.
- The V_{DDUSB} can be connected either to V_{DD} or an external independent power supply (3.0 to 3.6 V) for USB transceivers (refer to [Figure 6](#) and [Figure 7](#)). For example, when the device is powered at 1.8 V, an independent power supply 3.3 V can be connected to the V_{DDUSB} . When the V_{DDUSB} is connected to a separated power supply, it is independent from V_{DD} or V_{DDA} but it must be the last supply to be provided and the first to disappear. The following conditions V_{DDUSB} must be respected:
 - During the power-on phase ($V_{DD} < V_{DD_MIN}$), V_{DDUSB} should be always lower than V_{DD}
 - During the power-down phase ($V_{DD} < V_{DD_MIN}$), V_{DDUSB} should be always lower than V_{DD}

3.20.1 Advanced-control timers (TIM1, TIM8)

The advanced-control timers (TIM1, TIM8) can be seen as three-phase PWM generators multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead times. They can also be considered as complete general-purpose timers. Their 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge- or center-aligned modes)
- One-pulse mode output

If configured as standard 16-bit timers, they have the same features as the general-purpose TIMx timers. If configured as 16-bit PWM generators, they have full modulation capability (0-100%).

The advanced-control timer can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

The TIM1 and TIM8 support independent DMA request generation.

3.20.2 General-purpose timers (TIMx)

There are ten synchronizable general-purpose timers embedded in the STM32F730x8 devices (see [Table 6](#) for differences).

- **TIM2, TIM3, TIM4, TIM5**

The STM32F730x8 include 4 full-featured general-purpose timers: TIM2, TIM5, TIM3, and TIM4. The TIM2 and TIM5 timers are based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. The TIM3 and TIM4 timers are based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. They all feature 4 independent channels for input capture/output compare, PWM or one-pulse mode output. This gives up to 16 input capture/output compare/PWMs on the largest packages.

The TIM2, TIM3, TIM4, TIM5 general-purpose timers can work together, or with the other general-purpose timers and the advanced-control timers TIM1 and TIM8 via the Timer Link feature for synchronization or event chaining.

Any of these general-purpose timers can be used to generate PWM outputs.

TIM2, TIM3, TIM4, TIM5 all have independent DMA request generation. They are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 4 hall-effect sensors.

- **TIM9, TIM10, TIM11, TIM12, TIM13, and TIM14**

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM10, TIM11, TIM13, and TIM14 feature one independent channel, whereas TIM9 and TIM12 have two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers. They can also be used as simple time bases.

3.20.3 Basic timers TIM6 and TIM7

These timers are mainly used for the DAC trigger and waveform generation. They can also be used as a generic 16-bit time base.

The TIM6 and TIM7 support independent DMA request generation.

Table 10. STM32F730x8 pin and ball definition (continued)

Pin Number				Pin name (function after reset) ⁽¹⁾	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP64	LQFP100	LQFP144	UFBGA176						
-	-	78	R15	PB15	I/O	FT	-	OTG_HS_DP	-
-	55	79	P15	PD8	I/O	FT	-	USART3_TX, FMC_D13, EVENTOUT	-
-	56	80	P14	PD9	I/O	FT	-	USART3_RX, FMC_D14, EVENTOUT	-
-	57	81	N15	PD10	I/O	FT	-	USART3_CK, FMC_D15, EVENTOUT	-
-	58	82	N14	PD11	I/O	FT	-	USART3_CTS, QUADSPI_BK1_IO0, SAI2_SD_A, FMC_A16/FMC_CLE, EVENTOUT	-
-	59	83	N13	PD12	I/O	FT	-	TIM4_CH1, LPTIM1_IN1, USART3_RTS, QUADSPI_BK1_IO1, SAI2_FS_A, FMC_A17/FMC_ALE, EVENTOUT	-
-	60	84	M15	PD13	I/O	FT	-	TIM4_CH2, LPTIM1_OUT, QUADSPI_BK1_IO3, SAI2_SCK_A, FMC_A18, EVENTOUT	-
-	-	85	-	VSS	S	-	-	-	-
-	-	86	J13	VDD	S	-	-	-	-
-	61	87	M14	PD14	I/O	FT	-	TIM4_CH3, UART8_CTS, FMC_D0, EVENTOUT	-
-	62	88	L14	PD15	I/O	FT	-	TIM4_CH4, UART8_RTS, FMC_D1, EVENTOUT	-
-	-	89	L15	PG2	I/O	FT	-	FMC_A12, EVENTOUT	-
-	-	90	K15	PG3	I/O	FT	-	FMC_A13, EVENTOUT	-
-	-	91	K14	PG4	I/O	FT	-	FMC_A14/FMC_BA0, EVENTOUT	-
-	-	92	K13	PG5	I/O	FT	-	FMC_A15/FMC_BA1, EVENTOUT	-
-	-	-	-	PG6	I/O	FT	-	EVENTOUT	-
-	-	-	-	PG7	I/O	FT	-	USART6_CK, FMC_INT, EVENTOUT	-



Table 12. STM32F730x8 alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11/LPTIM1	I2C1/2/3/USART1	SPI1/I2S1/ SPI2/I2S2/ SPI3/I2S3/ SPI4/5	SPI2/I2S2/ SPI3/I2S3/ SPI3/I2S3/ SAI1/ UART4	SPI2/I2S2/SPI3/I2S3/ USART1/2/3/USART5	SAI2/USART6/USART4/5/7/8/OTG1_FS	CAN1/TIM12/13/14/QUADSPI/ ADSPI/ FMC/ OTG2_HS	SAI2/QUADSPI/SDMMC2/OTG2_HS/OTG1_FS	SDMMC2	UART7/FMC/SDMMC1/OTG2_FS	SYS
Port G	PG0	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A10	EVEN TOUT
	PG1	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A11	EVEN TOUT
	PG2	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A12	EVEN TOUT
	PG3	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A13	EVEN TOUT
	PG4	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A14/ FMC_BA0	EVEN TOUT
	PG5	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A15/ FMC_BA1	EVEN TOUT
	PG6	-	-	-	-	-	-	-	-	-	-	-	-	-	EVEN TOUT
	PG7	-	-	-	-	-	-	-	-	USART6_CK	-	-	-	FMC_INT	EVEN TOUT
	PG8	-	-	-	-	-	-	-	-	USART6_RTS	-	-	-	FMC_SCLK	EVEN TOUT
	PG9	-	-	-	-	-	-	-	-	USART6_RX	QUADSPI_BK2_IO2	SAI2_FS_B	SDMMC2_D0	FMC_NE2/ FMC_NCE	EVEN TOUT
	PG10	-	-	-	-	-	-	-	-	-	-	SAI2_SD_B	SDMMC2_D1	FMC_NE3	EVEN TOUT

1. When bypassing the voltage regulator, the two 2.2 μF V_{CAP} capacitors are not required and should be replaced by two 100 nF decoupling capacitors.

Table 19. VCAP1 operating conditions in the LQFP64 package⁽¹⁾

Symbol	Parameter	Conditions
CEXT	Capacitance of external capacitor	4.7 μF
ESR	ESR of external capacitor	between 0.1 Ω and 0.2 Ω

1. When bypassing the voltage regulator, the 4.7 μF V_{CAP} capacitor is not required and should be replaced by two 100 nF decoupling capacitors.

6.3.3 Operating conditions at power-up / power-down (regulator ON)

Subject to general operating conditions for T_A .

Table 20. Operating conditions at power-up / power-down (regulator ON)

Symbol	Parameter	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	20	∞	$\mu\text{s/V}$
	V_{DD} fall time rate	20	∞	

6.3.4 Operating conditions at power-up / power-down (regulator OFF)

Subject to general operating conditions for T_A .

Table 21. Operating conditions at power-up / power-down (regulator OFF)⁽¹⁾

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	Power-up	20	∞	$\mu\text{s/V}$
	V_{DD} fall time rate	Power-down	20	∞	
t_{VCAP}	V_{CAP_1} and V_{CAP_2} rise time rate	Power-up	20	∞	
	V_{CAP_1} and V_{CAP_2} fall time rate	Power-down	20	∞	

1. To reset the internal logic at power-down, a reset must be applied on pin PA0 when V_{DD} reach below 1.08 V.

6.3.5 Reset and power control block characteristics

The parameters given in [Table 22](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 16](#).

Table 32. Typical and maximum current consumptions in Standby mode

Symbol	Parameter	Conditions	Typ ⁽¹⁾			Max ⁽²⁾			Unit
			T _A = 25 °C			T _A = 25 °C	T _A = 85 °C	T _A = 105 °C	
			V _{DD} = 1.7 V	V _{DD} = 2.4 V	V _{DD} = 3.3 V	V _{DD} = 3.3 V			
I _{DD_STBY}	Supply current in Standby mode	Backup SRAM OFF, RTC and LSE OFF	1.09	1.13	1.4	4	27	55	µA
		Backup SRAM ON, RTC and LSE OFF	1.85	1.88	2.17	5	30	60	
		Backup SRAM OFF, RTC ON and LSE in low drive mode	1.65	1.86	2.43	7	47	95.5	
		Backup SRAM OFF, RTC ON and LSE in medium low drive mode	1.67	1.88	2.46	7	47.5	97	
		Backup SRAM OFF, RTC ON and LSE in medium high drive mode	1.8	2.01	2.61	7.5	50.5	102.5	
		Backup SRAM OFF, RTC ON and LSE in high drive mode	1.92	2.13	2.73	8	53	107	
		Backup SRAM ON, RTC ON and LSE in low drive mode	2.39	2.6	3.23	9	62	127	
		Backup SRAM ON, RTC ON and LSE in Medium low drive mode	2.41	2.64	3.25	9	63	128	
		Backup SRAM ON, RTC ON and LSE in Medium high drive mode	2.67	2.89	2.53	10	68	139	
		Backup SRAM ON, RTC ON and LSE in High drive mode	2.68	2.9	3.51	10	68	138	

1. PDR is OFF for V_{DD}=1.7V. When the PDR is OFF (internal reset OFF), the typical current consumption is reduced by additional 1.2 µA.
2. Guaranteed by characterization results.

Table 35. Peripheral current consumption (continued)

Peripheral		I _{DD} (Typ) ⁽¹⁾			Unit
		Scale 1	Scale 2	Scale 3	
APB1 (up to 54 MHz)	TIM2	19.3	18.2	15.6	μA/MHz
	TIM3	15	14	12.2	
	TIM4	15.7	15.1	12.8	
	TIM5	18	16.9	14.4	
	TIM6	3.7	3.1	2.8	
	TIM7	3.5	2.9	2.5	
	TIM12	8.1	7.8	6.4	
	TIM13	6.1	5.1	4.7	
	TIM14	6.3	5.6	4.7	
	LPTIM1	9.4	9.8	8.3	
	WWDG	2.4	1.3	1.4	
	SPI2/I2S2 ⁽³⁾	6.7	6	5.3	
	SPI3/I2S3 ⁽³⁾	4.8	3.8	3.3	
	USART2	13.3	12	10.6	
	USART3	12.8	12	10.3	
	UART4	11.7	10.7	9.2	
	UART5	11.7	10.2	8.9	
	I2C1	10.6	9.6	8.3	
	I2C2	10.6	9.6	8.3	
	I2C3	10.7	9.8	8.3	
	CAN1	8.9	8	6.9	
	PWR	11.3	11.3	8.9	
	DAC ⁽⁴⁾	6.1	5.1	4.4	
	UART7	13.3	12	10.3	
	UART8	12.6	11.6	9.7	

6.3.10 Internal clock source characteristics

The parameters given in [Table 42](#) and [Table 43](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 16](#).

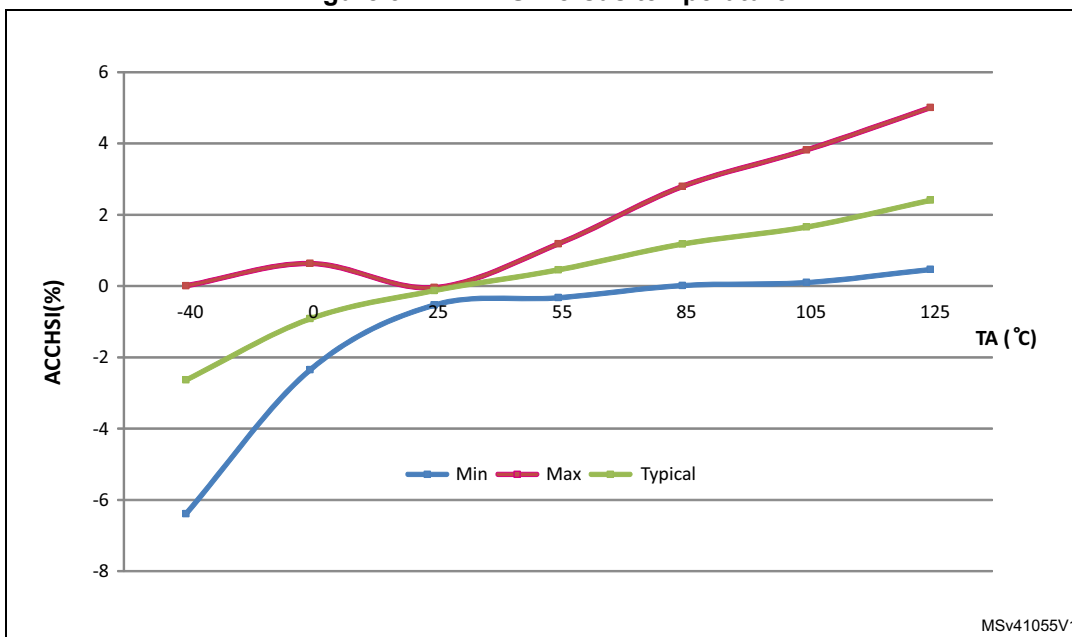
High-speed internal (HSI) RC oscillator

Table 42. HSI oscillator characteristics ⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	16	-	MHz
ACC_{HSI}	HSI user trimming step ⁽²⁾	-	-	-	1	%
	Accuracy of the HSI oscillator	$T_A = -40$ to $105\text{ }^{\circ}\text{C}$ ⁽³⁾	- 8	-	4.5	%
		$T_A = -10$ to $85\text{ }^{\circ}\text{C}$ ⁽³⁾	- 4	-	4	%
		$T_A = 25\text{ }^{\circ}\text{C}$ ⁽⁴⁾	- 1	-	1	%
$t_{su(HSI)}$ ⁽²⁾	HSI oscillator startup time	-	-	2.2	4	μs
$I_{DD(HSI)}$ ⁽²⁾	HSI oscillator power consumption	-	-	60	80	μA

1. $V_{DD} = 3.3\text{ V}$, $T_A = -40$ to $105\text{ }^{\circ}\text{C}$ unless otherwise specified.
2. Guaranteed by design.
3. Guaranteed by characterization results.
4. Factory calibrated, parts not soldered.

Figure 32. ACCHSI versus temperature



1. Guaranteed by characterization results.

Table 53. Flash memory programming (continued)

Symbol	Parameter	Conditions	Min ⁽¹⁾	Typ	Max ⁽¹⁾	Unit
t _{ME}	Mass erase time	Program/erase parallelism (PSIZE) = x 8	-	7718	9883	ms
		Program/erase parallelism (PSIZE) = x 16	-	4869	6379	
		Program/erase parallelism (PSIZE) = x 32	-	3503	5180	
V _{prog}	Programming voltage	32-bit program operation	2.7	-	3	V
		16-bit program operation	2.1	-	3.6	V
		8-bit program operation	1.7	-	3.6	V

1. Guaranteed by characterization results.
2. The maximum programming time is measured after 10 K erase operations.

Table 54. Flash memory programming with V_{PP}

Symbol	Parameter	Conditions	Min ⁽¹⁾	Typ	Max ⁽¹⁾	Unit
t _{prog}	Double word programming	T _A = 0 to +40 °C V _{DD} = 3.3 V V _{PP} = 8.5 V	-	16	100 ⁽²⁾	μs
t _{ERASE16KB}	Sector (16 KB) erase time		-	180	-	ms
t _{ERASE128KB}	Sector (128 KB) erase time		-	900	-	
t _{ERASE64KB}	Sector (64 KB) erase time		-	450	-	
t _{ME}	Mass erase time	-	-	6.9	-	s
V _{prog}	Programming voltage	-	2.7	-	3.6	V
V _{PP}	V _{PP} voltage range	-	7	-	9	V
I _{PP}	Minimum current sunk on the V _{PP} pin	-	10	-	-	mA
t _{VPP} ⁽³⁾	Cumulative time during which V _{PP} is applied	-	-	-	1	hour

1. Guaranteed by design.
2. The maximum programming time is measured after 10 K erase operations.
3. V_{PP} should only be connected during programming/erasing.

Table 55. Flash memory endurance and data retention

Symbol	Parameter	Conditions ⁽¹⁾	Value	Unit
			Min ⁽²⁾	
N _{END}	Endurance	T _A = -40 to +85 °C (6 suffix versions) T _A = -40 to +105 °C (7 suffix versions)	10	kcycles
t _{RET}	Data retention	1 kcycle ⁽³⁾ at T _A = 85 °C	30	Years
		1 kcycle ⁽³⁾ at T _A = 105 °C	10	
		10 kcycles ⁽³⁾ at T _A = 55 °C	20	

Table 58. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value ⁽¹⁾	Unit
$V_{\text{ESD(HBM)}}$	Electrostatic discharge voltage (human body model)	$T_A = +25\text{ }^{\circ}\text{C}$ conforming to ANSI/ESDA/JEDEC JS-001-2012	2	2000	V
$V_{\text{ESD(CDM)}}$	Electrostatic discharge voltage (charge device model)	$T_A = +25\text{ }^{\circ}\text{C}$ conforming to ANSI/ESD STM5.3.1-2009, all the packages excepted WLCSP100	3	250	

1. Guaranteed by characterization results.

Static latchup

Two complementary static tests are required on six parts to assess the latchup performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latchup standard.

Table 59. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	$T_A = +105\text{ }^{\circ}\text{C}$ conforming to JESD78A	II level A

6.3.19 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of $-5\text{ }\mu\text{A}/+0\text{ }\mu\text{A}$ range), or other functional failure (for example reset, oscillator frequency deviation).

Negative induced leakage current is caused by negative injection and positive induced leakage current by positive injection.

The test results are given in [Table 60](#).

Unless otherwise specified, the parameters given in [Table 63](#) are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in [Table 16](#).

Table 63. I/O AC characteristics⁽¹⁾⁽²⁾

OSPEEDRy [1:0] bit value ⁽¹⁾	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
00	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽³⁾	$C_L = 50 \text{ pF}, V_{DD} \geq 2.7 \text{ V}$	-	-	4	MHz
			$C_L = 50 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	2	
			$C_L = 10 \text{ pF}, V_{DD} \geq 2.7 \text{ V}$	-	-	8	
			$C_L = 10 \text{ pF}, V_{DD} \geq 1.8 \text{ V}$	-	-	4	
			$C_L = 10 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	3	
	$t_{f(\text{IO})\text{out}}/$ $t_{r(\text{IO})\text{out}}$	Output high to low level fall time and output low to high level rise time	$C_L = 50 \text{ pF}, V_{DD} = 1.7 \text{ V to } 3.6 \text{ V}$	-	-	100	ns
01	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽³⁾	$C_L = 50 \text{ pF}, V_{DD} \geq 2.7 \text{ V}$	-	-	25	MHz
			$C_L = 50 \text{ pF}, V_{DD} \geq 1.8 \text{ V}$	-	-	12.5	
			$C_L = 50 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	10	
			$C_L = 10 \text{ pF}, V_{DD} \geq 2.7 \text{ V}$	-	-	50	
			$C_L = 10 \text{ pF}, V_{DD} \geq 1.8 \text{ V}$	-	-	20	
			$C_L = 10 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	12.5	
	$t_{f(\text{IO})\text{out}}/$ $t_{r(\text{IO})\text{out}}$	Output high to low level fall time and output low to high level rise time	$C_L = 50 \text{ pF}, V_{DD} \geq 2.7 \text{ V}$	-	-	10	ns
			$C_L = 10 \text{ pF}, V_{DD} \geq 2.7 \text{ V}$	-	-	6	
			$C_L = 50 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	20	
			$C_L = 10 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	10	
10	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽³⁾	$C_L = 40 \text{ pF}, V_{DD} \geq 2.7 \text{ V}$	-	-	50 ⁽⁴⁾	MHz
			$C_L = 10 \text{ pF}, V_{DD} \geq 2.7 \text{ V}$	-	-	100 ⁽⁴⁾	
			$C_L = 40 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	25	
			$C_L = 10 \text{ pF}, V_{DD} \geq 1.8 \text{ V}$	-	-	50	
			$C_L = 10 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	42.5	
	$t_{f(\text{IO})\text{out}}/$ $t_{r(\text{IO})\text{out}}$	Output high to low level fall time and output low to high level rise time	$C_L = 40 \text{ pF}, V_{DD} \geq 2.7 \text{ V}$	-	-	6	ns
			$C_L = 10 \text{ pF}, V_{DD} \geq 2.7 \text{ V}$	-	-	4	
			$C_L = 40 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	10	
			$C_L = 10 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	6	

Table 78. DAC characteristics (continued)

Symbol	Parameter	Min	Typ	Max	Unit	Comments
$I_{VREF+}^{(4)}$	DAC DC V_{REF} current consumption in quiescent mode (Standby mode)	-	170	240	μA	With no load, worst code (0x800) at $V_{REF+} = 3.6 V$ in terms of DC consumption on the inputs
		-	50	75		With no load, worst code (0xF1C) at $V_{REF+} = 3.6 V$ in terms of DC consumption on the inputs
$I_{DDA}^{(4)}$	DAC DC V_{DDA} current consumption in quiescent mode ⁽³⁾	-	280	380	μA	With no load, middle code (0x800) on the inputs
		-	475	625	μA	With no load, worst code (0xF1C) at $V_{REF+} = 3.6 V$ in terms of DC consumption on the inputs
DNL ⁽⁴⁾	Differential non linearity Difference between two consecutive code-1LSB)	-	-	± 0.5	LSB	Given for the DAC in 10-bit configuration.
		-	-	± 2	LSB	Given for the DAC in 12-bit configuration.
INL ⁽⁴⁾	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023)	-	-	± 1	LSB	Given for the DAC in 10-bit configuration.
		-	-	± 4	LSB	Given for the DAC in 12-bit configuration.
Offset ⁽⁴⁾	Offset error (difference between measured value at Code (0x800) and the ideal value = $V_{REF+}/2$)	-	-	± 10	mV	Given for the DAC in 12-bit configuration
		-	-	± 3	LSB	Given for the DAC in 10-bit at $V_{REF+} = 3.6 V$
		-	-	± 12	LSB	Given for the DAC in 12-bit at $V_{REF+} = 3.6 V$
Gain error ⁽⁴⁾	Gain error	-	-	± 0.5	%	Given for the DAC in 12-bit configuration
$t_{SETTLING}^{(4)}$	Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value $\pm 4LSB$)	-	3	6	μs	$C_{LOAD} \leq 50 pF$, $R_{LOAD} \geq 5 k\Omega$
THD ⁽⁴⁾	Total Harmonic Distortion Buffer ON	-	-	-	dB	$C_{LOAD} \leq 50 pF$, $R_{LOAD} \geq 5 k\Omega$
Update rate ⁽²⁾	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	-	-	1	MS/s	$C_{LOAD} \leq 50 pF$, $R_{LOAD} \geq 5 k\Omega$

Table 79. Minimum I2CCLK frequency in all I2C modes

Symbol	Parameter	Condition		Min	Unit
f(I2CCLK)	I2CCLK frequency	Standard-mode	-	2	MHz
		Fast-mode	Analog Filter ON DNF=0	10	
			Analog Filter OFF DNF=1	9	
		Fast-mode Plus	Analog Filter ON DNF=0	22.5	
			Analog Filter OFF DNF=1	16	

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

The 20mA output drive requirement in Fast-mode Plus is not supported. This limits the maximum load C_{load} supported in Fm+, which is given by these formulas:

- $Tr(SDA/SCL) = 0.8473 \times R_p \times C_{load}$
- $R_p(min) = (V_{DD} - V_{OL(max)}) / I_{OL(max)}$

Where R_p is the I2C lines pull-up. Refer to [Section 6.3.20: I/O port characteristics](#) for the I2C I/Os characteristics.

All I²C SDA and SCL I/Os embed an analog filter. Refer to the table below for the analog filter characteristics:

Table 80. I2C analog filter characteristics⁽¹⁾

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	50 ⁽²⁾	260 ⁽³⁾	ns

1. Guaranteed by characterization results.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered

Table 101. Synchronous multiplexed NOR/PSRAM read timings⁽¹⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	$2T_{hclk} - 0.5$	-	ns
$t_{d(CLKL-NEXL)}$	FMC_CLK low to FMC_NEx low ($x=0..2$)	-	2	
$t_{d(CLKH-NEXH)}$	FMC_CLK high to FMC_NEx high ($x=0..2$)	$T_{hclk} + 0.5$	-	
$t_{d(CLKL-NADV L)}$	FMC_CLK low to FMC_NADV low	-	1	
$t_{d(CLKL-NADV H)}$	FMC_CLK low to FMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid ($x=16..25$)	-	3	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid ($x=16..25$)	T_{hclk}	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	-	2	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	$T_{hclk} - 0.5$	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	2	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	0	-	
$t_{su(ADV-CLKH)}$	FMC_A/D[15:0] valid data before FMC_CLK high	0.5	-	
$t_h(CLKH-ADV)$	FMC_A/D[15:0] valid data after FMC_CLK high	4	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	2	-	
$t_h(CLKH-NWAIT)$	FMC_NWAIT valid after FMC_CLK high	3	-	

1. Guaranteed by characterization results.

Table 102. Synchronous multiplexed PSRAM write timings⁽¹⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	2Thclk - 0.5	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	2	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0...2)	Thclk +0.5	-	
$t_{d(CLKL-NADV_L)}$	FMC_CLK low to FMC_NADV low	-	1	
$t_{d(CLKL-NADV_H)}$	FMC_CLK low to FMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16...25)	-	3	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16...25)	Thclk	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	1.5	
$t_{d(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	Thclk +0.5	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	3	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	0	-	
$t_{d(CLKL-DATA)}$	FMC_A/D[15:0] valid data after FMC_CLK low	-	3	
$t_{d(CLKL-NBL_L)}$	FMC_CLK low to FMC_NBL low	-	2	
$t_{d(CLKH-NBL_H)}$	FMC_CLK high to FMC_NBL high	Thclk +0.5	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	2	-	
$t_h(CLKH-NWAIT)$	FMC_NWAIT valid after FMC_CLK high	3	-	

1. Guaranteed by characterization results.

Table 107. SDRAM read timings⁽¹⁾

Symbol	Parameter	Min	Max	Unit
$t_{W(SDCLK)}$	FMC_SDCLK period	2Thclk -0.5	2Thclk +0.5	ns
$t_{su(SDCLKH_Data)}$	Data input setup time	1.5	-	
$t_{h(SDCLKH_Data)}$	Data input hold time	2	-	
$t_{d(SDCLKL_Add)}$	Address valid time	-	1.5	
$t_{d(SDCLKL_SDNE)}$	Chip select valid time	-	1.5	
$t_{h(SDCLKL_SDNE)}$	Chip select hold time	0.5	-	
$t_{d(SDCLKL_SDNRAS)}$	SDNRAS valid time	-	1	
$t_{h(SDCLKL_SDNRAS)}$	SDNRAS hold time	0.5	-	
$t_{d(SDCLKL_SDNCAS)}$	SDNCAS valid time	-	1.5	
$t_{h(SDCLKL_SDNCAS)}$	SDNCAS hold time	0	-	

1. Guaranteed by characterization results.

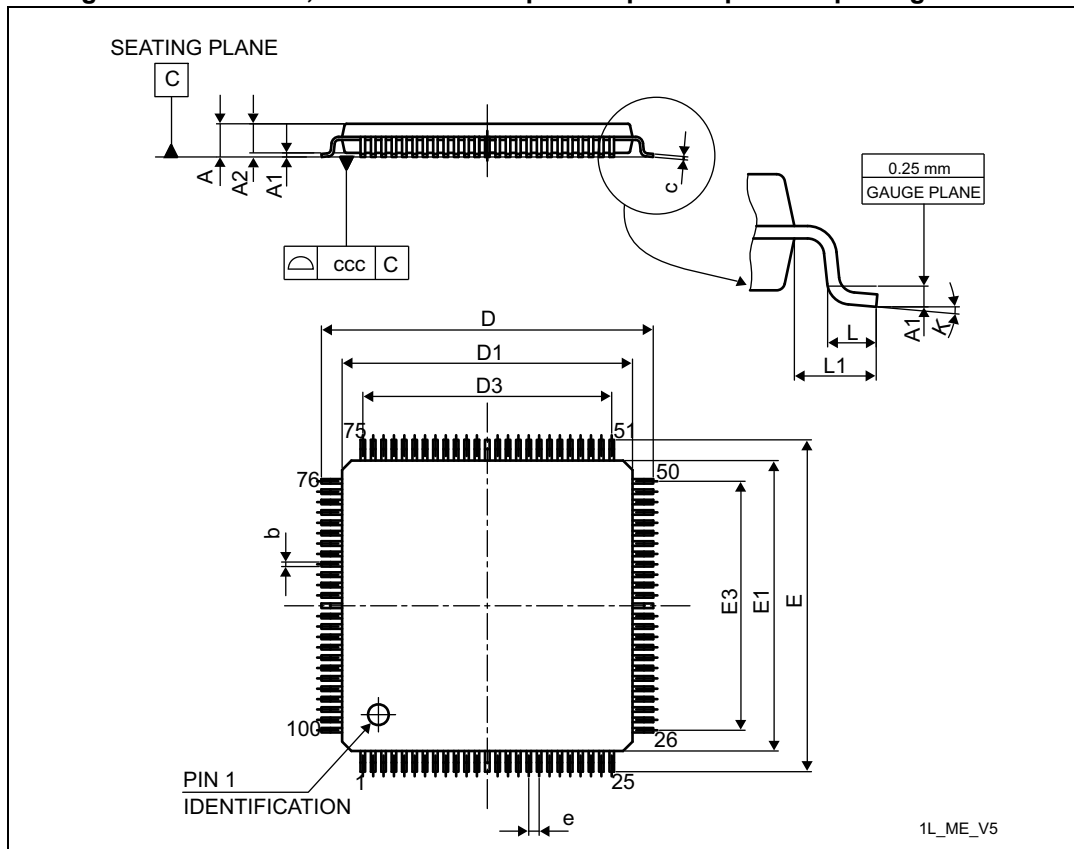
Table 108. LPSPDR SDRAM read timings⁽¹⁾

Symbol	Parameter	Min	Max	Unit
$t_{W(SDCLK)}$	FMC_SDCLK period	2Thclk -0.5	2Thclk +0.5	ns
$t_{su(SDCLKH_Data)}$	Data input setup time	0	-	
$t_{h(SDCLKH_Data)}$	Data input hold time	4.5	-	
$t_{d(SDCLKL_Add)}$	Address valid time	-	1.5	
$t_{d(SDCLKL_SDNE)}$	Chip select valid time	-	1.5	
$t_{h(SDCLKL_SDNE)}$	Chip select hold time	0	-	
$t_{d(SDCLKL_SDNRAS)}$	SDNRAS valid time	-	0.5	
$t_{h(SDCLKL_SDNRAS)}$	SDNRAS hold time	0	-	
$t_{d(SDCLKL_SDNCAS)}$	SDNCAS valid time	-	1.5	
$t_{h(SDCLKL_SDNCAS)}$	SDNCAS hold time	0	-	

1. Guaranteed by characterization results.

7.2 LQFP100, 14 x 14 mm low-profile quad flat package information

Figure 74. LQFP100, 14 x 14 mm 100-pin low-profile quad flat package outline



1. Drawing is not to scale.

Table 116. LQFP100, 14 x 14 mm 100-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

Technical drawing of a cross-section of a square tube. The drawing shows the profile of the tube with dimensions and material specifications.

Dimensions:

- Overall width: 16.7
- Overall height: 16.7
- Inner width: 12.3
- Inner height: 12.3
- Wall thickness (top): 0.5
- Wall thickness (right): 0.3
- Flange thickness (bottom right): 1.2
- Vertical distance from top to inner wall start: 14.3
- Vertical distance from bottom to inner wall start: 16.7

Material Specifications:

- Top flange: 75
- Right flange: 51
- Left flange: 76
- Bottom flange: 26
- Inner wall: 100
- Inner wall (bottom right): 25
- Inner wall (bottom left): 1