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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S12
Core Size	16-Bit
Speed	20MHz
Connectivity	LINbus, SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	3
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 15x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP Exposed Pad
Supplier Device Package	48-HLQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/sm912f634dv2ae

2 Pin Assignment

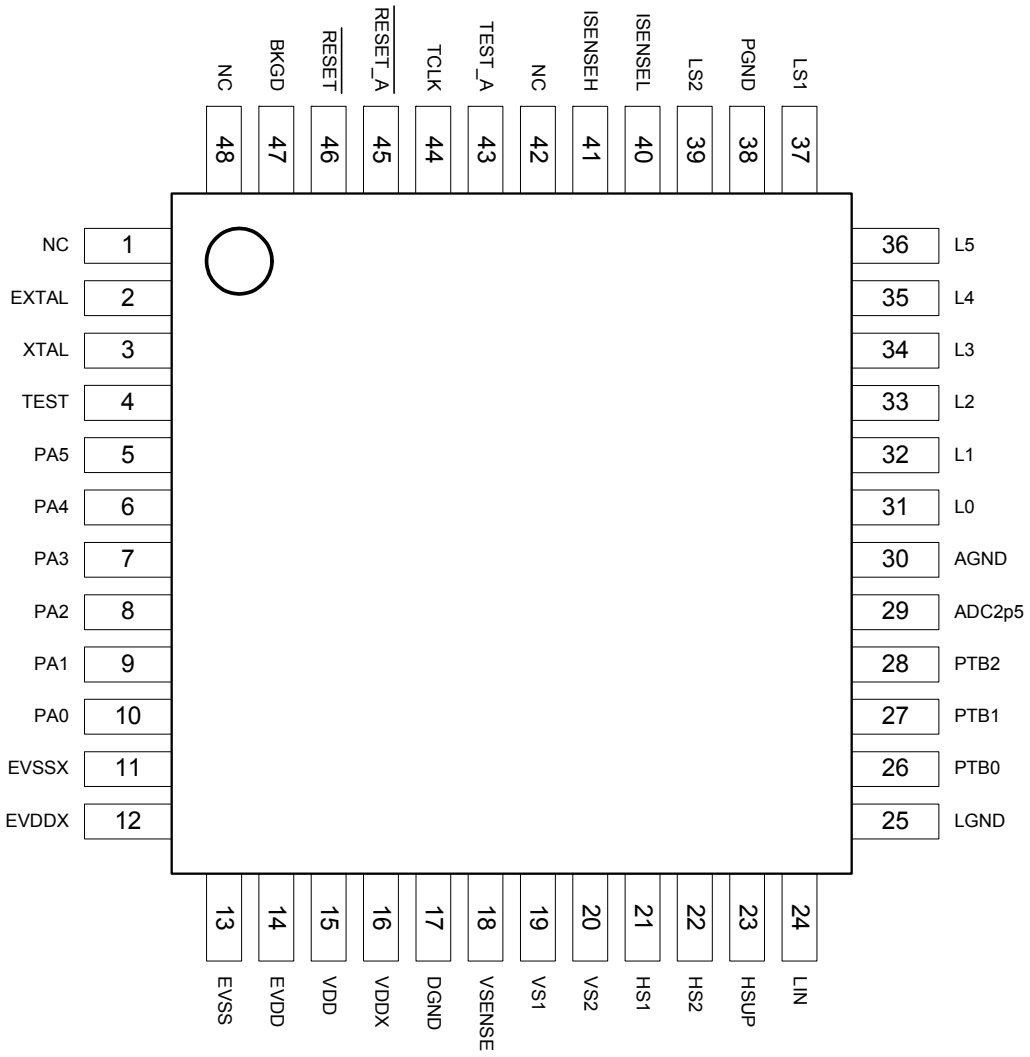


Figure 4. S/MM912F634 Pin Out

NOTE

The device exposed pad (package option AE only) is recommended to be connected to GND.

Not all pins are available for analog die option 2. See Section 4.2.3, “Analog Die Options" for details.

2.1 S/MM912F634 Pin Description

The following table gives a brief description of all available pins on the S/MM912F634 package. Refer to the highlighted chapter for detailed information.

Table 3. S/MM912F634 Pin Description

Pin #	Pin Name	Formal Name	Description
1	NC	Not connected Pin	This pin is reserved for alternative function and should be left floating or connected to GND.
2	EXTAL	MCU Oscillator Pin	EXTAL is one of the optional crystal/resonator driver and external clock pins. On reset, all the device clocks are derived from the Internal Reference Clock. See Section 4.33, “External Oscillator (S12SOSCFPV1)".

Table 3. S/MM912F634 Pin Description (continued)

Pin #	Pin Name	Formal Name	Description
36	L5	High Voltage Input 5	This pins is the High Voltage Input 5 with the following shared functions: • L5 - Digital High Voltage Input 5. When used as digital input, a series resistor (R_{Lx}) must be used to protect against automotive transients.(5) • AD8 - Analog Input 8 with selectable divider for 0…5.0 V and 0…18 V measurement range. • WU5 - Selectable Wake-up input 5 for wake-up and cyclic sense during low power mode. See Section 4.16, “High Voltage Inputs - Lx". Note: This pin function is not available on all device configurations.
37	LS1	Low-side Output 1	Low-side output 1 used to drive small inductive loads like relays. The output is short-circuit protected, includes active clamp circuitry and can be also controlled by the PWM module. See Section 4.12, “Low-side Drivers - LSx".
38	PGND	Power Ground Pin	This pin is the device Low-side Ground connection. DGND, LGND and AGND are internally connected to PGND via a back to back diode.
39	LS2	Low-side Output 2	Low-side output 2 used to drive small inductive loads like relays. The output is short-circuit protected, includes active clamp circuitry and can be also controlled by the PWM module. See Section 4.12, “Low-side Drivers - LSx".
40	ISENSEL	Current Sense Pins L	Current Sense differential input “Low”. This pin is used in combination with ISENSEH to measure the voltage drop across a shunt resistor. See Section 4.20, “Current Sense Module - ISENSE". Note: This pin function is not available on all device configurations.
41	ISENSEH	Current Sense Pins H	Current Sense differential input “High”. This pin is used in combination with ISENSEL to measure the voltage drop across a shunt resistor. Section 4.20, “Current Sense Module - ISENSE". Note: This pin function is not available on all device configurations.
42	NC	Not connected Pin	This pin is reserved for alternative function and should be left floating.
43	TEST_A	Test Mode Pin	Analog die Test Mode pin for Test Mode only. This pin must be grounded in user mode.
44	TCLK	Test Clock Input	Test Mode Clock Input pin for Test Mode only. The pin can be used to disable the internal watchdog for development purpose in user mode. See Section 4.9, “Window Watchdog". The pin is recommended to be grounded in user mode.
45	$\overline{\text{RESET\_A}}$	Reset I/O	Bidirectional Reset I/O pin of the analog die. Active low signal. Internal pull-up. V_{DDX} based. See Section 4.7, “Resets". To be externally connected to the $\overline{\text{RESET}}$ pin.
46	$\overline{\text{RESET}}$	MCU Reset Pin	The $\overline{\text{RESET}}$ pin is an active low bidirectional control signal. It acts as an input to initialize the MCU to a known start-up state, and an output when an internal MCU function causes a reset. The $\overline{\text{RESET}}$ pin has an internal pull-up device to EVDDX.
47	BKGD	MCU Background Debug and Mode Pin	The BKGD/MODC pin is used as a pseudo-open-drain pin for the background debug communication. It is used as MCU operating mode select pin during reset. The state of this pin is latched to the MODC bit at the rising edge of $\overline{\text{RESET}}$. The BKGD pin has a pull-up device.
48	NC	Not connected Pin	This pin is reserved for alternative function and should be left floating or connected to GND.

Note:

4. An optional filter capacitor C_{VSENSE} is recommended to be placed between the board connector and R_{VSENSE} to GND for increased ESD performance.
5. An optional filter capacitor C_{Lx} is recommended to be placed between the board connector and R_{Lx} to GND for increased ESD performance.

2.2 MCU Die Signal Properties

This section describes the external MCU signals. It includes a table of signal properties.

Table 4. Signal Properties Summary

Pin Name Function 1	Pin Name Function 2	Power Supply	Internal Pull Resistor		Description
			CTRL	Reset State	
EXTAL	—	V_{DD}	NA	NA	Oscillator pins
XTAL	—	V_{DD}	NA	NA	
$\overline{\text{RESET}}$	—	V_{DDX}	Pull-up		External reset

Table 8. Operating Conditions (continued)

Ratings	Symbol	Value	Unit
MCU Digital logic supply voltage[12]	V_{EDD}	2.25 to 2.75	V
MCU External Oscillator	f_{OSC}	4.0 to 16	MHz
MCU Bus frequency	f_{BUS}	f_{BUSMAX}[13]	MHz
Operating Ambient Temperature, MM912x634xVxxx	T_A	-40 to 105	°C
Operating Junction Temperature - Analog Die	T_{J_A}	-40 to 150	°C
Operating Junction Temperature - MCU Die	T_{J_M}	-40 to 140	°C

Note:
12. During power up and power down sequence always $V_{DD} < V_{DDX}$
13. f_{BUSMAX} frequency ratings differ by device and is specified in Table 1

3.4 Supply Currents

This section describes the current consumption characteristics of the device as well as the conditions for the measurements.

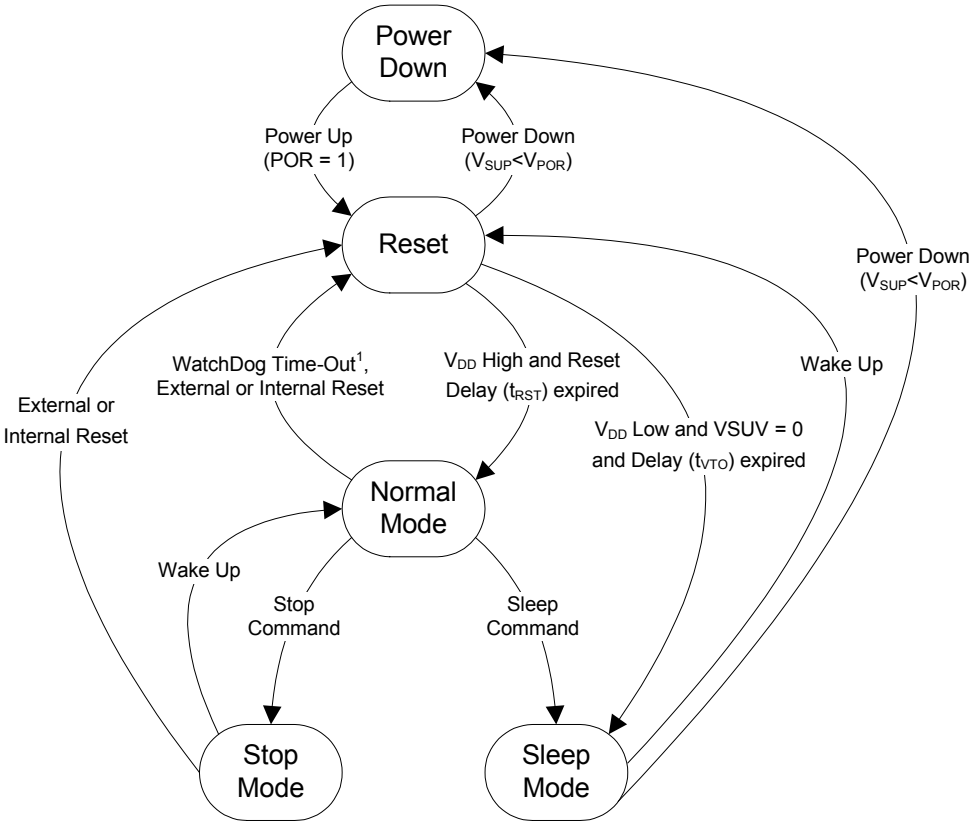
3.4.1 Measurement Conditions

All measurements are without output loads. Unless otherwise noted, the currents are measured in MCU special single chip mode and the CPU code is executed from RAM.

Table 9. Supply Currents

Ratings	Symbol	Min	Typ[14]	Max	Unit
Normal Mode analog die only, excluding external loads, LIN Recessive State (5.5 V ≤ V_{SUP} ≤ 18 V, 2.25 V ≤ E_{VDD} ≤ 2.75 V, 4.5 V ≤ E_{VDDX} ≤ 5.5 V, -40 °C ≤ T_{J_A} ≤ 150 °C).	I_{RUN_A}	-	5.0	8.0	mA
Normal Mode MCU die only (T_{J_M} = 140 °C; V_{DD} = 2.75 V, V_{DDX} = 5.5 V, f_{OSC} = 4.0 MHz, f_{BUS} = f_{BUSMAX}[18])[15]	I_{RUN_M}	-	12.5	15	mA
Stop Mode internal analog die only, excluding external loads, LIN Recessive State, Lx enabled, measured at VS1+VS2 (5.5 V ≤ V_{SUP} ≤ 18 V, 2.25 V ≤ E_{VDD} ≤ 2.75 V, 4.5 V ≤ E_{VDDX} ≤ 5.5 V) -40 °C ≤ T_{J_A} ≤ 125 °C 125 °C < T_{J_A} ≤ 140 °C	I_{STOP_A}	 - -	 20 -	 40 50	µA
Stop Mode MCU die only (V_{DD} = 2.75 V, V_{DDX} = 5.5 V, f_{OSC} = 4.0 MHz, f_{BUS} = f_{BUSMAX}[18]; MCU in STOP; RTI and COP off)[16] T_{J_M} = 140 °C T_{J_M} = 105 °C T_{J_M} = 25 °C	I_{STOP_M}	 - - -	 0.135 0.035 0.010	 0.400 0.200 0.030	mA
Stop Mode MCU die only (V_{DD} = 2.75 V, V_{DDX} = 5.5 V, f_{OSC} = 4.0 MHz, f_{BUS} = f_{BUSMAX}[18]; MCU in STOP; RTI and COP on)[16] T_{J_M} = 140 °C T_{J_M} = 105 °C T_{J_M} = 25 °C	I_{STOP_M}	 - - -	 0.205 0.104 0.079	 0.500 0.300 0.110	mA
Wait Mode MCU die only (T_{J_M} = 140 °C; V_{DD} = 2.75 V, V_{DDX} = 5.5 V, f_{OSC} = 4.0 MHz, f_{BUS} = f_{BUSMAX}[18]; All modules except RTI disabled)[17]	I_{WAIT_M}	-	7.0	12	mA
Sleep Mode (VDD = VDDX = OFF; 5.5 V ≤ V_{SUP} ≤ 18 V; -40 °C ≤ T_{J_A} ≤ 150 °C; 3.0 V < L_X < 1.0 V).	I_{SLEEP}	-	15	28	µA
Cyclic Sense Supply Current Adder (5.0 ms Cycle)	I_{CS}	-	15	20	µA

Note:
14. Typical values noted reflect the approximate parameter mean at T_A = 25 °C
15. I_{RUN_M} denotes the sum of the currents flowing into VDD and VDDX.
16. I_{STOP_M} denotes the sum of the currents flowing into VDD and VDDX.
17. I_{WAIT_M} denotes the sum of the currents flowing into VDD and VDDX.
18. f_{BUSMAX} frequency ratings differ by device and is specified in Table 1.



[1] Initial WD to be served within t_{WDTO} to enable Window WD

Figure 16. Modes of Operation and Transitions

4.3.1 Power Down Mode

For the device power (VS1) below V_{POR}, the S/MM912F634 analog die is virtually in Power Down mode. Once VS1>V_{POR}, the S/MM912F634 analog die enters Reset mode with the condition “Power On Reset - POR”.

4.3.2 Reset Mode

The S/MM912F634 analog die enters Reset mode if a reset condition occurs (POR - Power On Reset, LVR- Low Voltage Reset, Low Voltage VDDX Reset - LVRX, WDR - Watchdog Reset, EXR - External Reset, and WUR - Wake-up Sleep Reset).

For internal reset sources, the $\overline{\text{RESET\_A}}$ pin is driven low for t_{RST} after the reset condition is gone. After this delay, the $\overline{\text{RESET\_A}}$ pin is released. With a high detected on the $\overline{\text{RESET\_A}}$ pin, VDD>V_{LVR} and VDDX>V_{LVRX} the S/MM912F634 analog die enters in Normal mode.

To avoid short-circuit conditions being present for a long time, a t_{VTO} timeout is implemented. Once VDD < V_{LVR} or VDDX < V_{LVRX} with VS1 > (V_{LVRI}+ V_{LVR_H}) for more than t_{VTO}, the S/MM912F634 analog die transitions directly to Sleep mode.

The Reset Status Register (RSR) indicates the source of the reset by individual flags.

- POR - Power On Reset
- LVR - Low Voltage Reset VDD
- LVRX - Low Voltage Reset VDDX
- WDR - Watchdog Reset
- EXR - External Reset
- WUR - Wake-up Sleep Reset

4.5.2 Low Power Mode Operation

The D2D module is disabled in SLEEP mode. In Stop mode, the D2DINT signal is used to wake-up a powered down MCU. As the MCU could wake up without the S/MM912F634 analog die, a special command is recognized as a wake-up event during Stop mode. See Section 4.3, “Modes of Operation".

4.5.2.1 Normal Mode / Stop Mode

NOTE

The maximum allowed clock speed of the interface is limited to f_{D2D}.

While in Normal or Stop mode, D2DCLK acts as input only with pull present. D2D[3:0] operates as an input/output with pull-down always present. D2DINT acts as output only.

4.5.2.2 Sleep Mode

While in Sleep mode, all Interface data pins are pulled down to DGND to reduce power consumption.

4.6 Interrupts

Interrupts are used to signal a microcontroller that a peripheral needs to be serviced. While in Stop mode, the interrupt signal is used to signal Wake-up events. The interrupts are signaled by an active high level of the D2DINT pin, which remains high until the interrupt is acknowledged via the D2D-Interface. Interrupts are only asserted while in Normal mode.

4.6.1 Interrupt Source Identification

Once an Interrupt is signalized, there are two options to identify the corresponding source(s).

4.6.1.1 Interrupt Source Mirror

NOTE

The VSI - Voltage Status Interrupt combines the five status flags for the Low Battery Interrupt, Low Voltage Interrupt, High Voltage Interrupt, Voltage Regulator Overvoltage Interrupt, and the Voltage Regulator High Temperature Interrupt. The specific source can be identified by reading the Voltage Status Register - VSR.

All Interrupt sources in S/MM912F634 analog die are mirrored to a special Interrupt Source Register (ISR). This register is read only and indicates all currently pending Interrupts. Reading this register does not acknowledge any interrupt. An additional D2D access is necessary to serve the specific module.

4.6.1.1.1 Interrupt Source Register (ISR)

Table 78. Interrupt Source Register (ISR)

Offset[71] 0x00 (0x00 and 0x01 for 8Bit access) Access: User read

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	HOT	LSOT	HSOT	LINOT	SCI	RX	TX	ERR	TOV	CH3	CH2	CH1	CH0	VSI
W																

Note:

71. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

4.6.2.6 TIM Channel 1 Interrupt (CH1)

See Section 4.18, “Basic Timer Module - TIM (TIM16B4C)".

4.6.2.7 TIM Channel 2 Interrupt (CH2)

See Section 4.18, “Basic Timer Module - TIM (TIM16B4C)".

4.6.2.8 TIM Channel 3 Interrupt (CH3)

See Section 4.18, “Basic Timer Module - TIM (TIM16B4C)".

4.6.2.9 TIM Timer Overflow Interrupt (TOV)

See Section 4.18, “Basic Timer Module - TIM (TIM16B4C)".

4.6.2.10 SCI Error Interrupt (ERR)

See Section 4.15, “Serial Communication Interface (S08SCIV4)".

4.6.2.11 SCI Transmit Interrupt (TX)

See Section 4.15, “Serial Communication Interface (S08SCIV4)".

4.6.2.12 SCI Receive Interrupt (RX)

See Section 4.15, “Serial Communication Interface (S08SCIV4)".

4.6.2.13 LIN Driver Overtemperature Interrupt (LINOT)

Acknowledge the interrupt by reading the LIN Register - LINR. To issue a new interrupt, the condition has to vanish and occur again. See Section 4.14, “LIN Physical Layer Interface - LIN" for details on the LIN Register including masking information.

4.6.2.14 High-side Overtemperature Interrupt (HSOT)

Acknowledge the interrupt by reading the High-side Status Register - HSSR. To issue a new interrupt, the condition has to vanish and occur again. See Section 4.11, “High-side Drivers - HS" for details on the High-side Status Register including masking information.

4.6.2.15 Low-side Overtemperature Interrupt (LSOT)

Acknowledge the interrupt by reading the Low-side Status Register - LSSR. To issue a new interrupt, the condition has to vanish and occur again. See Section 4.12, “Low-side Drivers - LSx" for details on the Low-side Status Register including masking information.

4.6.2.16 HSUP Overtemperature Interrupt (HOT)

Acknowledge the interrupt by reading the Hall Supply Register - HSR. To issue a new interrupt, the condition has to vanish and occur again. See Section 4.10, “Hall Sensor Supply Output - HSUP" for details on the Hall Supply Register including masking information.

4.6.2.17 High Voltage Interrupt (HVI)

Acknowledge the interrupt by reading the Voltage Status Register - VSR. To issue a new interrupt, the condition has to vanish and occur again. See Section 4.4, “Power Supply" for details on the Voltage Status Register including masking information.

4.6.2.18 Voltage Regulator Overvoltage Interrupt (VROVI)

Acknowledge the interrupt by reading the Voltage Status Register - VSR. To issue a new interrupt, the condition has to vanish and occur again. See Section 4.4, “Power Supply" for details on the Voltage Status Register including masking information.

4.7 Resets

To protect the system during critical events, the S/MM912F634 analog die drives the RESET_A pin low during the presence of the reset condition. In addition, the RESET_A pin is monitored for external reset events. To match the MCU, the RESET_A pin is based on the VDDX voltage level.

After an internal reset condition has gone, the RESET_A stays low for an additional time t_{RST} before being released. Entering reset mode causes all S/MM912F634 analog die registers to be initialized to their RESET default. The only registers with valid information are the Reset Status Register (RSR) and the Wake-up Source Register (WUS).

4.7.1 Reset Sources

In the S/MM912F634 six reset sources exist.

4.7.1.1 POR - Analog Die Power On Reset

To indicate the device power supply (VS1) was below V_{POR} or the S/MM912F634 analog die was powered up, the POR condition is set. See Section 4.3, “Modes of Operation".

4.7.1.2 LVR - Low Voltage Reset - VDD

With the VDD voltage regulator output voltage falling below V_{LVR}, the Low Voltage Reset condition becomes present. As the VDD Regulator is shutdown once a LVRX condition is detected, The actual cause could be also a low voltage condition at the VDDX regulator. See Section 4.4, “Power Supply".

4.7.1.3 LVRX - Low Voltage Reset - VDDX

With the VDDX voltage regulator output voltage falling below V_{LVRX}, the Low Voltage Reset condition becomes present. See Section 4.4, “Power Supply".

4.7.1.4 WUR - Wake-up Reset

While in Sleep mode, any active wake-up event causes a S/MM912F634 analog die transition from Sleep to Reset Mode.
To determine the wake-up source, refer to Section 4.8, “Wake-up / Cyclic Sense".

4.7.1.5 EXR - External Reset

Any low level voltage at the RESET_A pin with a duration > t_{RSTDF} issues an External Reset event. This reset source is also active in Stop mode.

4.7.1.6 WDR - Watchdog Reset

Any incorrect serving if the S/MM912F634 analog die Watchdog results in a Watchdog Reset. Refer to the Section 4.9, “Window Watchdog" for details.

4.7.2 Register Definition

4.7.2.1 Reset Status Register (RSR)

Table 83. Reset Status Register (RSR)

Offset[73] 0x15 Access: User read

	7	6	5	4	3	2	1	0
R	0	0	WDR	EXR	WUR	LVRX	LVR	POR
W								

Note:
73. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 133. SCIS1 Field Descriptions (continued)

Field	Description
1 FE	**Framing Error Flag** — FE is set at the same time as RDRF when the receiver detects a logic 0 where the stop bit was expected. This suggests the receiver was not properly aligned to a character frame. To clear FE, read SCIS1 with FE = 1 and then read the SCI data register (SCID). 0 No framing error detected. This does not guarantee the framing is correct. 1 Framing error.
0 PF	**Parity Error Flag** — PF is set at the same time as RDRF when parity is enabled (PE = 1) and the parity bit in the received character does not agree with the expected parity value. To clear PF, read SCIS1 and then read the SCI data register (SCID). 0 No parity error. 1 Parity error.

4.15.2.5 SCI Status Register 2 (SCIS2)

This register has one read-only status flag.

Table 134. SCI Status Register 2 (SCIS2)

Offset[104] 0x45 Access: User read/write

	7	6	5	4	3	2	1	0
R	LBKDIF	RXEDGIF	0	RXINV[92]	RWUID	BRK13	LBKDE	RAF
W								
Reset	0	0	0	0	0	0	0	0

Note:
104. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 135. SCIS2 Field Descriptions

Field	Description
7 LBKDIF	**LIN Break Detect Interrupt Flag** — LBKDIF is set when the LIN break detect circuitry is enabled and a LIN break character is detected. LBKDIF is cleared by writing a “1” to it. 0 No LIN break character has been detected. 1 LIN break character has been detected.
6 RXEDGIF	**RxD Pin Active Edge Interrupt Flag** — RXEDGIF is set when an active edge (falling if RXINV = 0, rising if RXINV=1) on the RxD pin occurs. RXEDGIF is cleared by writing a “1” to it. 0 No active edge on the receive pin has occurred. 1 An active edge on the receive pin has occurred.
4 RXINV[105]	**Receive Data Inversion** — Setting this bit reverses the polarity of the received data input. 0 Receive data not inverted 1 Receive data inverted
3 RWUID	**Receive Wake Up Idle Detect**— RWUID controls whether the idle character wakes up the receiver sets the IDLE bit. 0 During receive standby state (RWU = 1), the IDLE bit does not get set upon detection of an idle character. 1 During receive standby state (RWU = 1), the IDLE bit gets set upon detection of an idle character.
2 BRK13	**Break Character Generation Length** — BRK13 is used to select a longer transmitted break character length. Detection of a framing error is not affected by the state of this bit. 0 Break character is transmitted with length of 10 bit times (11 if M = 1) 1 Break character is transmitted with length of 13 bit times (14 if M = 1)
1 LBKDE	**LIN Break Detection Enable**— LBKDE is used to select a longer break character detection length. While LBKDE is set, framing error (FE) and receive data register full (RDRF) flags are prevented from setting. 0 Break character detection disabled 1 Break character detection enabled

Note:
105. Setting RXINV inverts the RxD input for all cases: data bits, start and stop bits, break, and idle.

After receiving the stop bit into the receive shifter, and provided the receive data register is not already full, the data character is transferred to the receive data register and the receive data register full (RDRF) status flag is set. If RDRF was already set indicating the receive data register (buffer) was already full, the overrun (OR) status flag is set and the new data is lost. Because the SCI receiver is double-buffered, the program has one full character time after RDRF is set before the data in the receive data buffer must be read to avoid a receiver overrun.

When a program detects the receiving data register is full (RDRF = 1), it gets the data from the receive data register by reading SCID. The RDRF flag is cleared automatically by a 2-step sequence which is normally satisfied in the course of the user's program handling receive data. Refer to Section 4.15.3.4, "Interrupts and Status Flags" for more details about flag clearing.

4.15.3.3.1 Data Sampling Technique

The SCI receiver uses a 16× baud rate clock for sampling. The receiver starts by taking logic level samples at 16 times the baud rate to search for a falling edge on the RxD serial data input pin. A falling edge is defined as a logic 0 sample after three consecutive logic 1 samples. The 16× baud rate clock is used to divide the bit time into 16 segments labeled RT1 through RT16. When a falling edge is located, three more samples are taken at RT3, RT5, and RT7 to make sure this was a real start bit and not merely noise. If at least two of these three samples are 0, the receiver assumes it is synchronized to a receive character.

The receiver then samples each bit time, including the start and stop bits, at RT8, RT9, and RT10 to determine the logic level for this bit. The logic level is interpreted to be of the majority of the samples taken during the bit time. In the case of the start bit, the bit is assumed to be 0 if at least two of the samples at RT3, RT5, and RT7 are 0 even if one or all of the samples taken at RT8, RT9, and RT10 are 1s. If any sample in any bit time (including the start and stop bits) in a character frame fails to agree with the logic level for this bit, the noise flag (NF) is set when the received character is transferred to the receive data buffer.

The falling edge detection logic continuously looks for falling edges, and if an edge is detected, the sample clock is resynchronized to bit times. This improves the reliability of the receiver in the presence of noise or mismatched baud rates. It does not improve worst case analysis because some characters do not have any extra falling edges anywhere in the character frame.

In the case of a framing error, provided the received character was not a break character, the sampling logic searching for a falling edge is filled with three logic 1 samples so a new start bit can be detected almost immediately.

In the case of a framing error, the receiver is inhibited from receiving any new characters until the framing error flag is cleared. The receive shift register continues to function, but a complete character cannot transfer to the receive data buffer if FE is still set.

4.15.3.3.2 Receiver Wake-up Operation

Receiver wake-up is a hardware mechanism allowing an SCI receiver to ignore the characters in a message intended for a different SCI receiver. In such a system, all receivers evaluate the first character(s) of each message, and as soon as they determine the message is intended for a different receiver, they write logic 1 to the receiver wake up (RWU) control bit in SCIC2. When RWU bit is set, the status flags associated with the receiver (with the exception of the idle bit, IDLE, when RWUID bit is set) are inhibited from setting, thus eliminating the software overhead for handling the unimportant message characters. At the end of a message, or at the beginning of the next message, all receivers automatically force RWU to 0 so all receivers wake up in time to look at the first character(s) of the next message.

4.15.3.3.2.1 Idle-line Wake-up

When WAKE = 0, the receiver is configured for idle-line wake-up. In this mode, RWU is cleared automatically when the receiver detects a full character time of the idle-line level. The M control bit selects 8-bit or 9-bit data mode which determines how many bit times of idle are needed to constitute a full character time (10 or 11 bit times because of the start and stop bits).

When RWU is one and RWUID is zero, the idle condition waking up the receiver does not set the IDLE flag. The receiver wakes up and waits for the first data character of the next message which sets the RDRF flag and generate an interrupt if enabled. When RWUID is one, any idle condition sets the IDLE flag and generates an interrupt if enabled, regardless of whether RWU is zero or one.

The idle-line type (ILT) control bit selects one of two ways to detect an idle line. When ILT = 0, the idle bit counter starts after the start bit so the stop bit and any logic 1s at the end of a character count toward the full character time of idle. When ILT = 1, the idle bit counter does not start until after a stop bit time, so the idle detection is not affected by the data in the last character of the previous message.

9-bit data mode typically is used in conjunction with parity to allow eight bits of data plus the parity in the ninth bit. Or it is used with address-mark wake-up so the ninth data bit can serve as the wake-up bit. In custom protocols, the ninth bit can also serve as a software-controlled marker.

4.15.3.5.2 Stop Mode Operation

During all stop modes, clocks to the SCI module are halted. In stop1 and stop2 modes, all SCI register data is lost and must be re-initialized upon recovery from these two stop modes. No SCI module registers are affected in stop3 mode.

The receive input active edge detect circuit is still active in stop3 mode, but not in stop2. An active edge on the receive input brings the CPU out of stop3 mode if the interrupt is not masked (RXEDGIE = 1).

Note that because the clocks are halted, the SCI module resumes operation upon exit from stop (only in stop3 mode). Software should ensure stop mode is not entered while there is a character being transmitted out of or received into the SCI module.

4.15.3.5.3 Loop Mode

When LOOPS = 1, the RSRC bit in the same register chooses between loop mode (RSRC = 0) or single-wire mode (RSRC = 1). Loop mode is sometimes used to check software, independent of connections in the external system, to help isolate system problems. In this mode, the transmitter output is internally connected to the receiver input and the RxD pin is not used by the SCI, so it reverts to a general purpose port I/O pin.

4.15.3.5.4 Single-wire Operation

When LOOPS = 1, the RSRC bit in the same register chooses between loop mode (RSRC = 0) or single-wire mode (RSRC = 1). Single-wire mode is used to implement a half-duplex serial connection. The receiver is internally connected to the transmitter output and to the TxD pin. The RxD pin is not used and reverts to a general purpose port I/O pin.

In single-wire mode, the TXDIR bit in SCIC3 controls the direction of serial data on the TxD pin. When TXDIR = 0, the TxD pin is an input to the SCI receiver and the transmitter is temporarily disconnected from the TxD pin so an external device can send serial data to the receiver. When TXDIR = 1, the TxD pin is an output driven by the transmitter. In single-wire mode, the internal loop back connection from the transmitter to the receiver causes the receiver to receive characters sent out by the transmitter.

4.16 High Voltage Inputs - Lx

Six High Voltage capable inputs are implemented with the following features:

- Digital Input Capable
- Analog Input Capable with selectable voltage divider.
- Wake-up Capable during Low Power mode. See Section 4.8, “Wake-up / Cyclic Sense".

When used as analog inputs to sense voltages outside the module a series resistor must be used on the used input. When a Lx input is not selected in the analog multiplexer, the voltage divider is disconnected from this input. When a Lx input is selected in the analog multiplexer, it is disconnected in low power mode if configured as Wake-up input. Unused Lx pins are recommended to be connected to GND to improve EMC behavior.

4.16.1 Register Definition

4.16.1.1 Lx Status Register (LXR)

Table 140. Lx Status Register (LXR)

Offset[109] 0x08 Access: User read

	7	6	5	4	3	2	1	0
R	0	0	L5	L4	L3	L2	L1	L0
W								

Note:
109. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

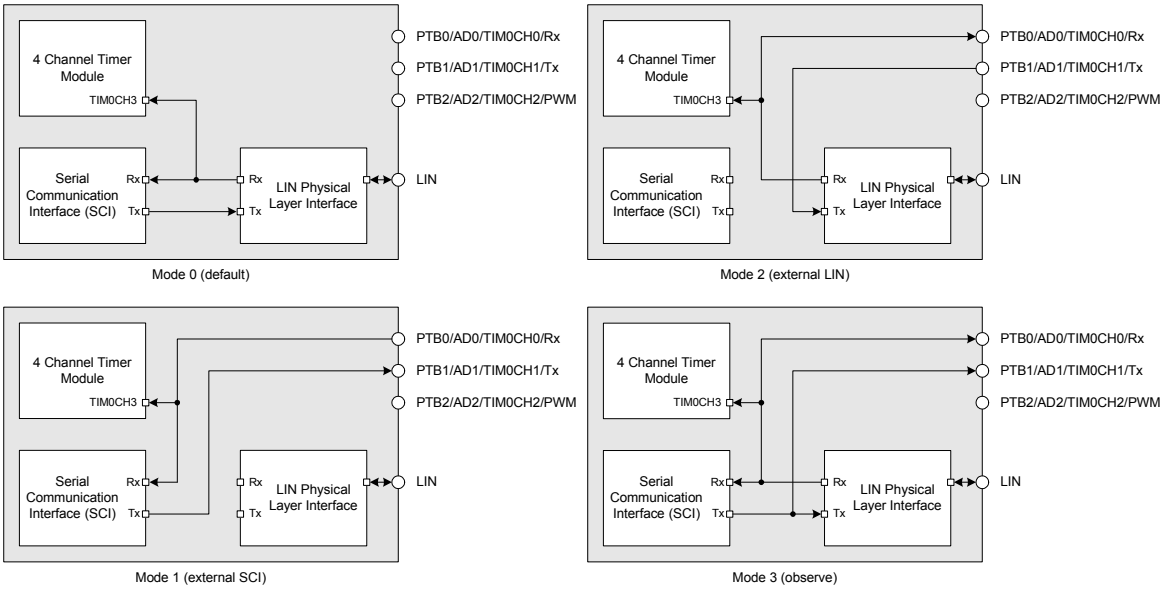


Figure 35. Alternative SCI / LIN Functionality

4.17.3 Alternative PWM Functionality

As an alternative routing for the PWM channel (0 or 1) output, the PortB 2 (PTB2) can be configured to output one of the two PWM channels defined in the Section 4.13, “PWM Control Module (PWM8B2C)". The selection and output enable can be configured in the Port B Configuration Register 2 (PTBC2).

4.17.4 Register definition

4.17.4.1 Port B Configuration Register 1 (PTBC1)

Table 145. Port B Configuration Register 1 (PTBC1)

Offset[111] 0x20 Access: User read/write

	7	6	5	4	3	2	1	0
R	0	PUEB2	PUEB1	PUEB0	0	DDRB2	DDRB1	DDRB0
W								
Reset	0	0	0	0	0	0	0	0

Note:
111. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 146. PTBC1 - Register Field Descriptions

Field	Description
6-4 PUEB[2-0]	Pull-up Enable Port B[2…0] 0 - Pull-up disabled on PTBx pin. 1- Pull-up enabled on PTBx pin.
2-0 DDRB[2-0]	Data Direction Port B[2….0] 0 - PTBx configured as input. 1 - PTBx configured as output.

NOTE

The pull-up resistor is not active once the port is configured as an output.

Table 202. S/MM912F634 Analog Die Trimming Registers (continued)

0xF2	CTR2	R	0	0	0	SLPBGTRE	SLPBG_LOCK	SLPBGTR2	SLPBGTR1	SLPBGTR0
	Trimming Reg 2	W								
0xF3	CTR3	R	OFFCTRE	OFFCTR2	OFFCTR1	OFFCTR0	CTR3_E	CTR3_2	CTR3_1	CTR3_0
	Trimming Reg 3	W								

Note:
145. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

At system startup, the trimming information have to be copied from the MCU IFR Flash location to the corresponding S/MM912F634 analog die trimming registers. The following table shows the register correlation.

Table 203. S/MM912F634 - MCU vs. Analog Die Trimming Register Correlation

Name	MCU IFR Address	Analog Offset(146)
CTR0	0x4C	0xF0
CTR1	0x4D	0xF1
CTR2	0x4E	0xF2
CTR3	0x4F	0xF3

Note:
146. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

4.25.2 Register Descriptions

4.25.2.1 Trimming Register 0 (CTR0)

Table 204. Trimming Register 0 (CTR0)

Offset(147) 0xF0 — Access: User read/write

	7	6	5	4	3	2	1	0
R W	LINTRE	LINTR	WDCTRE	CTR0_4	CTR0_3	WDCTR2	WDCTR1	WDCTR0
Reset	0	0	0	0	0	0	0	0

Note:
147. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 205. CTR0 - Register Field Descriptions

Field	Description
7 LINTRE	LIN trim enable 0 - no trim can be done 1- trim can be done by setting LINTR bit
6 LINTR	LIN trim bit 0 - default slope 1 - adjust the slope
5 WDCTRE	Watchdog trim enable 0 - no trim can be done 1 - trim can be done by setting WDCTR[2:0] bits
4 CTR0_4	Spare Trim bit 4

- COP module (Computer Operating Properly watchdog)
- RTI module (Real Time Interrupt)
- Memory Options
    - 32 k byte Flash
    - 2.0 k byte RAM
- Flash General Features
    - Erase sector size 512 bytes
    - Automated program and erase algorithm
- Serial Peripheral Interface Module (SPI)
    - Configurable for 8 or 16-bit data size
- Input/Output
    - Up to 6 general-purpose input/output (I/O) pins
    - Hysteresis on all input pins
    - Configurable drive strength on all output pins
- Die 2 Die Initiator (D2DI)
    - Up to 2.0 Mbyte/s data rate
    - Configurable 4-bit or 8-bit wide data path
- 20 MHz maximum CPU bus frequency (16 MHz for MM912F634CV2AP)

4.26.1.2 Modes of Operation

Memory map and bus interface modes:

- Normal operating mode
    - Normal single-chip mode
- Special Operating mode
    - Special single-chip mode with active background debug mode

Low-power modes:

- System stop mode
- System wait mode

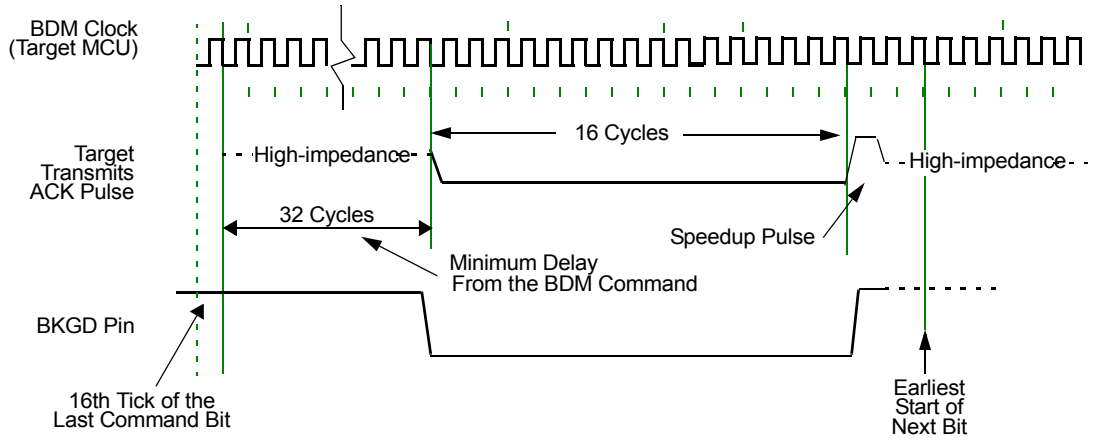


Figure 63. Target Acknowledge Pulse (ACK)

Figure 64 shows the ACK handshake protocol in a command level timing diagram. The READ_BYTE instruction is used as an example. First, the 8-bit instruction opcode is sent by the host, followed by the address of the memory location to be read. The target BDM decodes the instruction. A bus cycle is grabbed (free or stolen) by the BDM and it executes the READ_BYTE operation. Having retrieved the data, the BDM issues an ACK pulse to the host controller, indicating the addressed byte is ready to be retrieved. After detecting the ACK pulse, the host initiates the byte retrieval process. Note that data is sent in the form of a word and the host needs to determine which is the appropriate byte based on whether the address was odd or even.

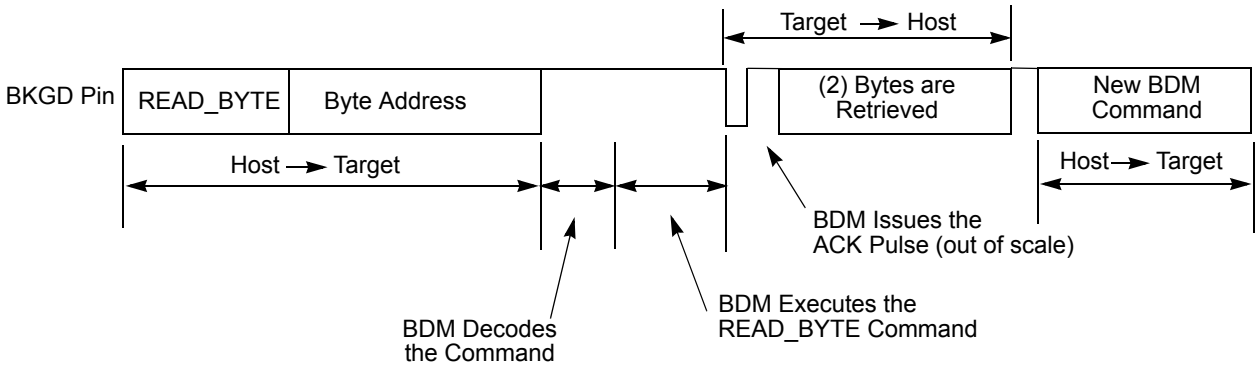


Figure 64. Handshake Protocol at Command Level

NOTE

The only place the BKGD pin can have an electrical conflict is when one side is driving low and the other side is issuing a speedup pulse (high). Other “highs” are pulled rather than driven. However, at low rates the time of the speedup pulse can become lengthy and so the potential conflict time becomes longer as well.

Differently from the normal bit transfer (where the host initiates the transmission), the serial interface ACK handshake pulse is initiated by the target MCU by issuing a negative edge in the BKGD pin. The hardware handshake protocol in Figure 63 specifies the timing when the BKGD pin is being driven, so the host should follow this timing constraint in order to avoid the risk of an electrical conflict in the BKGD pin.

NOTE

The ACK pulse does not provide a timeout. This means for the GO_UNTIL command, it can not be distinguished if a stop or wait has been executed (command discarded and ACK not issued) or if the “UNTIL” condition (BDM active) is just not reached yet. Hence in any case where the ACK pulse of a command is not issued the possible pending command should be aborted before issuing a new command. See the handshake abort procedure described in Section 4.30.4.8, “Hardware Handshake Abort Procedure".

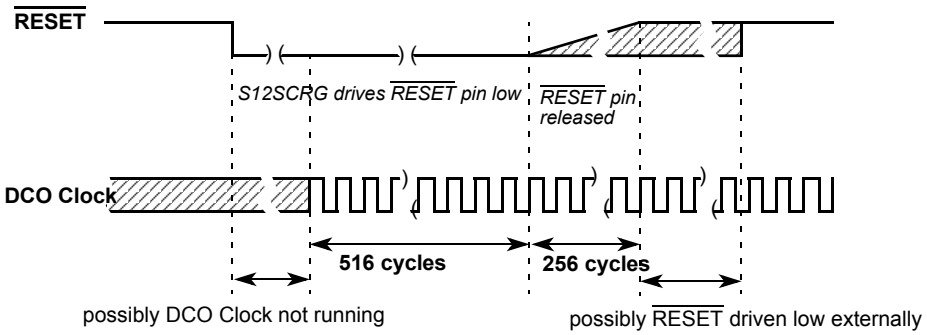


Figure 75. RESET Timing

4.32.5.2.1 Oscillator Monitor Reset

In case of loss of clock, or the oscillator frequency is below the failure assert frequency f_{OMFA} (see device electrical characteristics for values), the 9S12I32PIMV1 generates a Oscillator Monitor Reset.

4.32.5.2.2 Computer Operating Properly Watchdog (COP) Reset

A COP timeout generates a reset. See COP description for details.

4.32.5.2.3 Power-On Reset

The on-chip voltage POR circuitry detects when V_{DD} to the MCU has reached a certain level and asserts a Power-on reset.

4.32.6 Interrupts

The interrupts/reset vectors requested by the 9S12I32PIMV1 are listed in Table 338. Refer to MCU specification for related vector addresses and priorities.

Table 338. 9S12I32PIMV1 Interrupt Vectors

Interrupt Source	CCR Mask	Local Enable
FLL LOCK interrupt	I bit	CRGCTL1 (LOCKIE)

4.32.6.1 Description of Interrupt Operation

4.32.6.1.1 FLL Lock Interrupt

The 9S12I32PIMV1 generates a FLL Lock interrupt when the lock condition (LOCKST status bit) of the FLL has changed, either from a locked state to an unlocked state or vice versa. Lock interrupts are locally disabled by setting the LOCKIE bit to zero. The FLL Lock interrupt flag (LOCKIF) is set to1 when the lock condition has changed, and is cleared to 0 by writing a 1 to the LOCKIF bit.

4.33 External Oscillator (S12SOSCFPV1)

4.33.1 Introduction

The full swing Pierce oscillator (OSCFSP) module provides a robust clock source with an external crystal or ceramic resonator.

4.33.2 Features

The S12SCRG module provides the following features:

- Full rail-to-rail (2.5 V nominal) swing oscillation with low EM susceptibility
- High noise immunity due to input hysteresis
- Low power consumption due to operation with 2.5 V (nominal) supply

4.36.1.3 Block Diagram

A block diagram of the Flash module is shown in Figure 81.

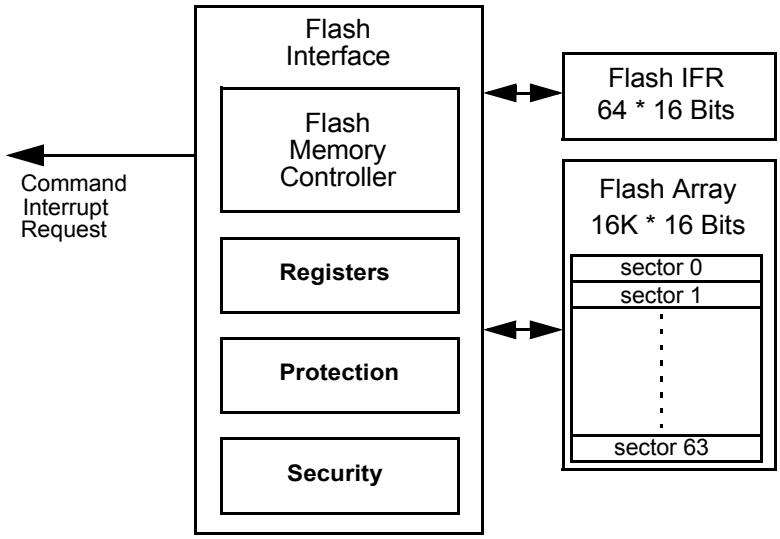


Figure 81. S12SFTSR32K Block Diagram

4.36.2 External Signal Description

The Flash module has no external signals.

4.36.3 Memory Map and Register Definition

This section describes the Flash array map, Flash IFR map, and Flash register map shown in Figure 82.

4.36.3.1 Flash Array Map

The MCU memory map places the Flash array addresses between Flash array base + 0x0000 and 0x7FFF.

4.36.3.4.2 Flash Reserved1 Register (FRSV1)

The FRSV1 register is reserved for factory testing.

Table 373. Flash Reserved1 Register (FRSV1)

0x0107

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

All FRSV1 bits read 0 and are not writable.

4.36.3.4.3 Flash Address Registers (FADDR)

NOTE

The LSB of the MCU global address is not stored in the FADDR registers, since the Flash block is not byte addressable.

The FADDR registers are the Flash address registers.

Table 374. Flash Address High Register (FADDRHI - Normal Mode)

0x0108

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

Table 375. Flash Address Low Register (FADDRLO - Normal Mode)

0x0109

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

Table 376. Flash Address High Register (FADDRHI - Special Mode)

0x0108

	7	6	5	4	3	2	1	0
R	0	0	FAB[13:8]					
W								
Reset	0	0	0	0	0	0	0	0

4.36.7 Resets

4.36.7.1 Flash Reset Sequence

On each reset, the Flash module executes a reset sequence to hold CPU activity, while reading the following resources from the Flash block:

- MCU control parameters (see Section 4.36.3.2)
- Flash protection byte (see Section 4.36.3.1.1 and Section 4.36.3.3.5)
- Flash nonvolatile byte (see Section 4.36.3.1.1)
- Flash security byte (see Section 4.36.3.1.1 and Section 4.36.3.3.2)

4.36.7.2 Reset While Flash Command Active

If a reset occurs while any Flash command is in progress, the command is immediately aborted. The state of the Flash array address being programmed or the sector/block being erased is not guaranteed.

4.36.8 Interrupts

NOTE

Vector addresses and their relative interrupt priority are determined at the MCU level.

The Flash module can generate an interrupt when all Flash command operations have completed, when the Flash address, data and command buffers are empty.

Table 390. Flash Interrupt Sources

Interrupt Source	Interrupt Flag	Local Enable	Global (CCR) Mask
Flash Address, Data and Command Buffers empty	CBEIF (FSTAT register)	CBEIE (FCNFG register)	I Bit
All Flash commands completed	CCIF (FSTAT register)	CCIE (FCNFG register)	I Bit

4.36.8.1 Description of Flash Interrupt Operation

The logic used for generating interrupts is shown in Figure 90. The Flash module uses the CBEIF and CCIF flags in combination with the CBIE and CCIE enable bits to generate the Flash command interrupt request.

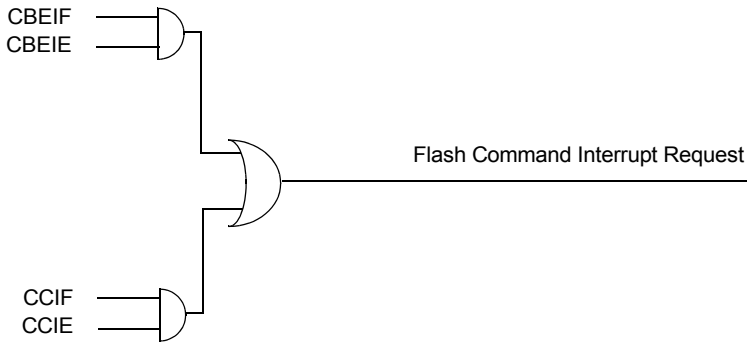


Figure 90. Flash Command Interrupt Implementation

For a detailed description of the register bits, refer to Section 4.36.3.3.4, “Flash Configuration Register (FCNFG)" and Section 4.36.3.4, “Flash Status Register (FSTAT)".

Table 391. Signal Properties

Name	Primary (D2DEN=1)	I/O	Secondary (D2DEN=0)	Reset	Comment	Pull-down
D2DDAT[7:0]	Bi-directional Data Lines	I/O	GPIO	0	driven low if in STOP mode	Active[197]
D2DCLK	Interface Clock Signal	O	GPIO	0	low if in STOP mode	—
$\overline{\text{D2DINT}}$	Active High Interrupt	I	GPIO	—	—	Active[198]

Note:
197. Active if in input state, only if D2DEN=1
198. only if D2DEN=1

See the port interface module (PIM) guide for details of the GPIO function.

4.37.3 Memory Map and Register Definition

4.37.3.1 Memory Map

The D2DI memory map is split into three sections.

1. An eight byte set of control registers.
2. A 256 byte window for blocking transactions.
3. A 256 byte window for non-blocking transactions.

See the chapter “Device Memory Map” for the register layout (distribution of these sections).

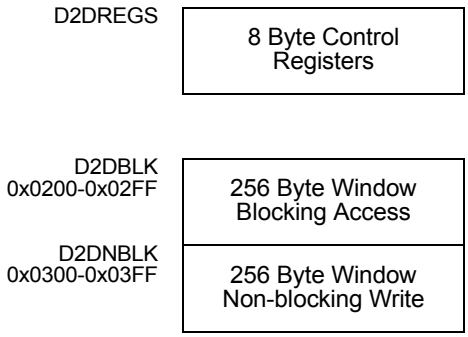


Figure 92. D2DI Top Level Memory Map

- The SCK is output for the master mode and input for the slave mode.
- The $\overline{SS}$ is the input or output for the master mode, and it is always the input for the slave mode.
- The bidirectional mode does not affect SCK and $\overline{SS}$ functions.

4.38.4.6 Error Conditions

The SPI has one error condition:

- Mode fault error

4.38.4.6.1 Mode Fault Error

NOTE

If a mode fault error occurs and a received data byte is pending in the receive shift register, this data byte is lost.

If the $\overline{SS}$ input becomes low while the SPI is configured as a master, it indicates a system error where more than one master may be trying to drive the MOSI and SCK lines simultaneously. This condition is not permitted in normal operation. The MODF bit in the SPI status register is set automatically, provided the MODFEN bit is set.

In the special case where the SPI is in master mode and MODFEN bit is cleared, the $\overline{SS}$ pin is not used by the SPI. In this case, the mode fault error function is inhibited and MODF remains cleared. In case the SPI system is configured as a slave, the $\overline{SS}$ pin is a dedicated input pin. Mode fault error doesn't occur in slave mode.

If a mode fault error occurs, the SPI is switched to slave mode, with the exception that the slave output buffer is disabled. So SCK, MISO, and MOSI pins are forced to be high-impedance inputs, to avoid any possibility of conflict with another output driver. A transmission in progress is aborted and the SPI is forced into idle state.

If the mode fault error occurs in the bidirectional mode for a SPI system configured in master mode, output enable of the MOMI (MOSI in bidirectional mode) is cleared if it was set. No mode fault error occurs in the bidirectional mode for SPI system configured in slave mode.

The mode fault flag is cleared automatically by a read of the SPI status register (with MODF set), followed by a write to the SPI control register 1. If the mode fault flag is cleared, the SPI becomes a normal master or slave again.

4.38.4.7 Low Power Mode Options

4.38.4.7.1 SPI in Run Mode

In run mode with the SPI system enable (SPE) bit in the SPI control register clear, the SPI system is in a low-power, disabled state. SPI registers remain accessible, but clocks to the core of this module are disabled.

4.38.4.7.2 SPI in Wait Mode

NOTE

Care must be taken when expecting data from a master while the slave is in wait or stop mode. Even though the shift register continues to operate, the rest of the SPI is shut down (i.e., a SPIF interrupt is **not** generated until exiting stop or wait mode). Also, the byte from the shift register is not copied into the SPIDR register until after the slave SPI has exited wait or stop mode. In slave mode, a received byte pending in the receive shift register is lost when entering wait or stop mode. An SPIF flag and SPIDR copy is generated only if wait mode is entered or exited during a transmission. If the slave enters wait mode in idle mode and exits wait mode in idle mode, neither a SPIF nor a SPIDR copy occurs.

SPI operation in wait mode depends upon the state of the SPISWAI bit in SPI control register 2.

- If SPISWAI is clear, the SPI operates normally when the CPU is in wait mode
- If SPISWAI is set, SPI clock generation ceases and the SPI module enters a power conservation state when the CPU is in wait mode.
- If SPISWAI is set and the SPI is configured for master, any transmission and reception in progress stops at wait mode entry. The transmission and reception resumes when the SPI exits wait mode.