Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| - , | . |
| $ - | %/ 0& |
| $ , # | %1 |
| , | ) 0 2# |
| $ | 3$ , - 4! 5 4 , ! 5 |
| - | 6 ! 7$6 - . 5 - 8 8 6 |
| 9 . | 0: |
| - , # | &) %; 1 <&) %; * %= |
| - | >7! , 2 |
| - 5 . , # | |
| 5! , # | %) 0; * % |
| ? , <? ? = | & %? @ ( %? |
| 6 $ | ! 6 &' * &/ &) |
| . | |
| . | A/ B$ @ %0 B$ < ! = |
| | , |
| - $ | : ' ?>C>9 6 5 * - |
| , 6 - | : ' 6 C>9 < *' = |
| - 457 | D * %/ 0& E' / |

## 24.2. SmaRTClock Clocking Sources

The SmaRTClock peripheral is clocked from its own timebase, independent of the system clock. The SmaRTClock timebase can be derived from an external CMOS clock, the internal LFO, or the SmaRT-Clock oscillator circuit, which has two modes of operation: Crystal Mode, and Self-Oscillate Mode. The oscillation frequency is 32.768 kHz in Crystal Mode and can be programmed in the range of 10 kHz to 40 kHz in Self-Oscillate Mode. The internal LFO frequency is 16.4 kHz ±20%. The frequency of the SmaRTClock oscillator can be measured with respect to another oscillator using an on-chip timer. See Section “32. Timers” on page 448 for more information on how this can be accomplished.

Note: The SmaRTClock timebase can be selected as the system clock and routed to a port pin. See Section “23. Clocking Sources” on page 291 for information on selecting the system clock source and Section “27. Port Input/Output” on page 356 for information on how to route the system clock to a port pin. The SmaRTClock timebase can also be routed to a port pin while the device is in its ultra low power sleep mode. See the PMU0MD register description for details.

### 24.2.1. Using the SmaRTClock Oscillator with a Crystal or External CMOS Clock

When using Crystal Mode, a 32.768 kHz crystal should be connected between XTAL3 and XTAL4. No other external components are required. The following steps show how to start the SmaRTClock crystal oscillator in software:

1. Configure the XTAL3 and XTAL4 pins for Analog I/O.
2. Set SmaRTClock to Crystal Mode (XMODE = 1).
3. Disable Automatic Gain Control (AGCEN) and enable Bias Doubling (BIASX2) for fast crystal startup.
4. Set the desired loading capacitance (RTC0XCF).
5. Enable power to the SmaRTClock oscillator circuit (RTC0EN = 1).
6. Wait 20 ms.
7. Poll the SmaRTClock Clock Valid Bit (CLKVLD) until the crystal oscillator stabilizes.
8. Poll the SmaRTClock Load Capacitance Ready Bit (LOADRDY) until the load capacitance reaches its programmed value.
9. Enable Automatic Gain Control (AGCEN) and disable Bias Doubling (BIASX2) for maximum power savings.
10. Enable the SmaRTClock missing clock detector.
11. Wait 2 ms.
12. Clear the PMU0CF wake-up source flags.

In Crystal Mode, the SmaRTClock oscillator may be driven by an external CMOS clock. The CMOS clock should be applied to XTAL3. XTAL34 should be left floating. In this mode, the external CMOS clock is ac coupled into the SmaRTClock and should have a minimum voltage swing of 400 mV. The CMOS clock signal voltage should not exceed VDD or drop below GND. Bias levels closer to VDD will result in lower I/O power consumption because the XTAL3 pin has a built-in weak pull-up. The SmaRTClock oscillator should be configured to its lowest bias setting with AGC disabled. The CLKVLD bit is indeterminate when using a CMOS clock, however, the OSCFAIL bit may be checked 2 ms after SmaRTClock oscillator is powered on to ensure that there is a valid clock on XTAL3. The CLKVLD bit is forced low when BIASX2 is disabled.

## SFR Definition 26.11. LCD0TOGR: LCD0 Toggle Rate

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | | | | | TOGR[3:0] | | | |
| Type | R/W | R/W | R/W | R/W | R/W | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

SFR Page = 0x2; SFR Address = 0x9F

| Bit | Name | Function |
|---|---|---|
| 7:4 | Unused | Read = 0000. Write = Don't Care. |
| 3:0 | TOGR[3:0] | LCD Toggle Rate Divider.<br>Sets the LCD Toggle Rate according to the following equation:<br>$\text{LCD Toggle Rate} = \frac{\text{Refresh Rate_umux_mode_u2}}{\text{Toggle Rate Divider}}$<br>0000: Reserved.<br>0001: Reserved.<br>0010: Toggle Rate Divider is set to divide by 2.<br>0011: Toggle Rate Divider is set to divide by 4.<br>0100: Toggle Rate Divider is set to divide by 8.<br>0101: Toggle Rate Divider is set to divide by 16.<br>0110: Toggle Rate Divider is set to divide by 32.<br>0111: Toggle Rate Divider is set to divide by 64.<br>1000: Toggle Rate Divider is set to divide by 128.<br>1001: Toggle Rate Divider is set to divide by 256.<br>1010: Toggle Rate Divider is set to divide by 512.<br>1011: Toggle Rate Divider is set to divide by 1024.<br>1100: Toggle Rate Divider is set to divide by 2048.<br>1101: Toggle Rate Divider is set to divide by 4096.<br>All other values reserved. |

## 27.4. Port Match

Port match functionality allows system events to be triggered by a logic value change on P0 or P1. A software controlled value stored in the PnMAT registers specifies the expected or normal logic values of P0 and P1. A Port mismatch event occurs if the logic levels of the Port's input pins no longer match the software controlled value. This allows Software to be notified if a certain change or pattern occurs on P0 or P1 input pins regardless of the XBRn settings.

The PnMASK registers can be used to individually select which P0 and P1 pins should be compared against the PnMAT registers. A Port mismatch event is generated if (P0 & P0MASK) does not equal (PnMAT & P0MASK) or if (P1 & P1MASK) does not equal (PnMAT & P1MASK).

A Port mismatch event may be used to generate an interrupt or wake the device from a low power mode. See Section "17. Interrupt Handler" on page 237 and Section "19. Power Management" on page 262 for more details on interrupt and wake-up sources.

### SFR Definition 27.4. P0MASK: Port0 Mask Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | P0MASK[7:0] | | | | | | | |
| Type | R/W | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

SFR Page= 0x0; SFR Address = 0xC7

| Bit | Name | Function |
|---|---|---|
| 7:0 | P0MASK[7:0] | Port0 Mask Value.<br>Selects the P0 pins to be compared with the corresponding bits in P0MAT.<br>0: P0.n pin pad logic value is ignored and cannot cause a Port Mismatch event.<br>1: P0.n pin pad logic value is compared to P0MAT.n. |

### SFR Definition 27.5. P0MAT: Port0 Match Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | P0MAT[7:0] | | | | | | | |
| Type | R/W | | | | | | | |
| Reset | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

SFR Page= 0x0; SFR Address = 0xD7

| Bit | Name | Function |
|---|---|---|
| 7:0 | P0MAT[7:0] | Port 0 Match Value.<br>Match comparison value used on Port 0 for bits in P0MASK which are set to 1.<br>0: P0.n pin logic value is compared with logic LOW.<br>1: P0.n pin logic value is compared with logic HIGH. |

## SFR Definition 27.12. P0DRV: Port0 Drive Strength

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | P0DRV[7:0] | | | | | | | |
| Type | R/W | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

SFR Page = 0xF; SFR Address = 0xA4

| Bit | Name | Function |
|---|---|---|
| 7:0 | P0DRV[7:0] | Drive Strength Configuration Bits for P0.7–P0.0 (respectively).<br>Configures digital I/O Port cells to high or low output drive strength.<br>0: Corresponding P0.n Output has low output drive strength.<br>1: Corresponding P0.n Output has high output drive strength. |

## SFR Definition 27.13. P1: Port1

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | P1[7:0] | | | | | | | |
| Type | R/W | | | | | | | |
| Reset | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

SFR Page = All Pages; SFR Address = 0x90; Bit-Addressable

| Bit | Name | Description | Write | Read |
|---|---|---|---|---|
| 7:0 | P1[7:0] | Port 1 Data.<br>Sets the Port latch logic value or reads the Port pin logic state in Port cells configured for digital I/O. | 0: Set output latch to logic LOW.<br>1: Set output latch to logic HIGH. | 0: P1.n Port pin is logic LOW.<br>1: P1.n Port pin is logic HIGH. |

## SFR Definition 27.38. P6DRV: Port6 Drive Strength

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | P6DRV[7:0] | | | | | | | |
| Type | R/W | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

SFR Page = 0xF; SFR Address = 0xAA

| Bit | Name | Function |
|---|---|---|
| 7:0 | P6DRV[7:0] | Drive Strength Configuration Bits for P6.7–P6.0 (respectively).<br>Configures digital I/O Port cells to high or low output drive strength.<br>0: Corresponding P6.n Output has low output drive strength.<br>1: Corresponding P6.n Output has high output drive strength. |

## SFR Definition 27.39. P7: Port7

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | | | | | | | | P7.0 |
| Type | | | | | | | | R/W |
| Reset | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

SFR Page = 0xF; SFR Address = 0xDC

| Bit | Name | Description | Read | Write |
|---|---|---|---|---|
| 7:1 | Unused | Read = 0000000b; Write = Don't Care. | | |
| 0 | P7.0 | Port 7 Data.<br>Sets the Port latch logic value or reads the Port pin logic state in Port cells configured for digital I/O. | 0: Set output latch to logic LOW.<br>1: Set output latch to logic HIGH. | 0: P7.0 Port pin is logic LOW.<br>1: P7.0 Port pin is logic HIGH. |

Table 29.2. Timer Settings for Standard Baud Rates
Using an External 22.1184 MHz Oscillator

| | Frequency: 22.1184 MHz | | | | | | |
|---|---|---|---|---|---|---|---|
| | Target Baud Rate (bps) | Baud Rate % Error | Oscilla-tor Divide Factor | Timer Clock Source | SCA1–SCA0 (pre-scale select) [1] | T1M[1] | Timer 1 Reload Value (hex) |
| SYSCLK from Internal Osc. | 230400 | 0.00% | 96 | EXTCLK / 8 | 11 | 0 | 0xFA |
| | 115200 | 0.00% | 192 | EXTCLK / 8 | 11 | 0 | 0xF4 |
| | 57600 | 0.00% | 384 | EXTCLK / 8 | 11 | 0 | 0xE8 |
| | 28800 | 0.00% | 768 | EXTCLK / 8 | 11 | 0 | 0xD0 |
| | 14400 | 0.00% | 1536 | EXTCLK / 8 | 11 | 0 | 0xA0 |
| | 9600 | 0.00% | 2304 | EXTCLK / 8 | 11 | 0 | 0x70 |

Notes:
1. SCA1–SCA0 and T1M bit definitions can be found in Section 32.1.
2. X = Don’t care.

wire slave mode), and the serial input data synchronously with the slave's system clock. If the master issues SCK, NSS, and the serial input data asynchronously, the maximum data transfer rate (bits/sec) must be less than 1/10 the system clock frequency. In the special case where the master only wants to transmit data to the slave and does not need to receive data from the slave (i.e. half-duplex operation), the SPI slave can receive data at a maximum data transfer rate (bits/sec) of 1/4 the system clock frequency. This is provided that the master issues SCK, NSS, and the serial input data synchronously with the slave's system clock.

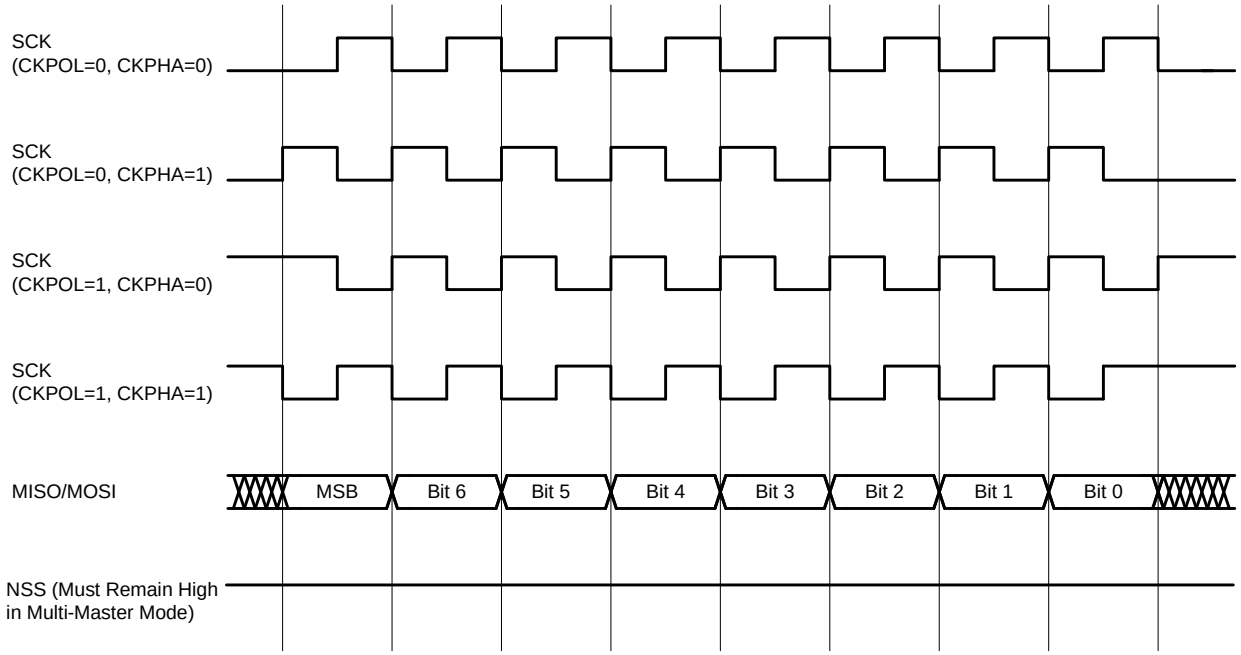


Figure 30.5. Master Mode Data/Clock Timing

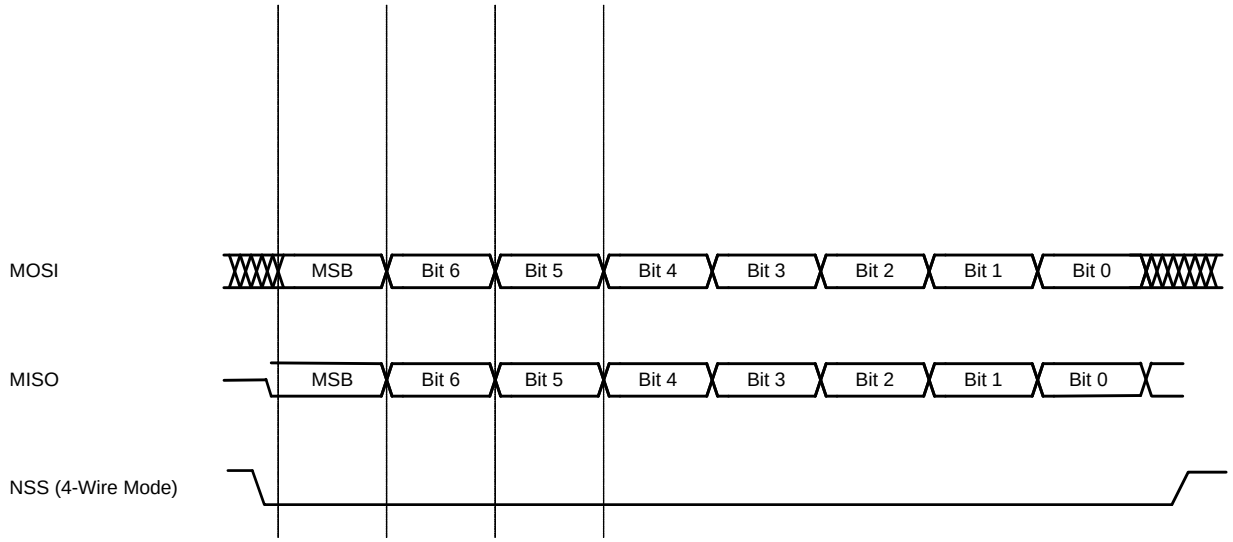


Figure 30.6. Slave Mode Data/Clock Timing (CKPHA = 0)

## SFR Definition 32.6. TH0: Timer 0 High Byte

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TH0[7:0] | | | | | | | |
| Type | R/W | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

SFR Page = 0x0; SFR Address = 0x8C

| Bit | Name | Function |
|---|---|---|
| 7:0 | TH0[7:0] | Timer 0 High Byte.<br>The TH0 register is the high byte of the 16-bit Timer 0. |

## SFR Definition 32.7. TH1: Timer 1 High Byte

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TH1[7:0] | | | | | | | |
| Type | R/W | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

SFR Page = 0x0; SFR Address = 0x8D

| Bit | Name | Function |
|---|---|---|
| 7:0 | TH1[7:0] | Timer 1 High Byte.<br>The TH1 register is the high byte of the 16-bit Timer 1. |

### 32.3.2. 8-Bit Timers with Auto-Reload

When T3SPLIT is set, Timer 3 operates as two 8-bit timers (TMR3H and TMR3L). Both 8-bit timers operate in auto-reload mode as shown in Figure 32.8. TMR3RLL holds the reload value for TMR3L; TMR3RLH holds the reload value for TMR3H. The TR3 bit in TMR3CN handles the run control for TMR3H. TMR3L is always running when configured for 8-bit Mode.

Each 8-bit timer may be configured to use SYSCLK, SYSCLK divided by 12, the external oscillator clock source divided by 8, or the SmaRTClock. The Timer 3 Clock Select bits (T3MH and T3ML in CKCON) select either SYSCLK or the clock defined by the Timer 3 External Clock Select bits (T3XCLK[1:0] in TMR3CN), as follows:

| T3MH | T3XCLK[1:0] | TMR3H Clock Source |
|---|---|---|
| 0 | 00 | SYSCLK / 12 |
| 0 | 01 | SmaRTClock |
| 0 | 10 | Reserved |
| 0 | 11 | External Clock / 8 |
| 1 | X | SYSCLK |

| T3ML | T3XCLK[1:0] | TMR3L Clock Source |
|---|---|---|
| 0 | 00 | SYSCLK / 12 |
| 0 | 01 | SmaRTClock |
| 0 | 10 | Reserved |
| 0 | 11 | External Clock / 8 |
| 1 | X | SYSCLK |

The TF3H bit is set when TMR3H overflows from 0xFF to 0x00; the TF3L bit is set when TMR3L overflows from 0xFF to 0x00. When Timer 3 interrupts are enabled, an interrupt is generated each time TMR3H overflows. If Timer 3 interrupts are enabled and TF3LEN (TMR3CN.5) is set, an interrupt is generated each time either TMR3L or TMR3H overflows. When TF3LEN is enabled, software must check the TF3H and TF3L flags to determine the source of the Timer 3 interrupt. The TF3H and TF3L interrupt flags are not cleared by hardware and must be manually cleared by software.

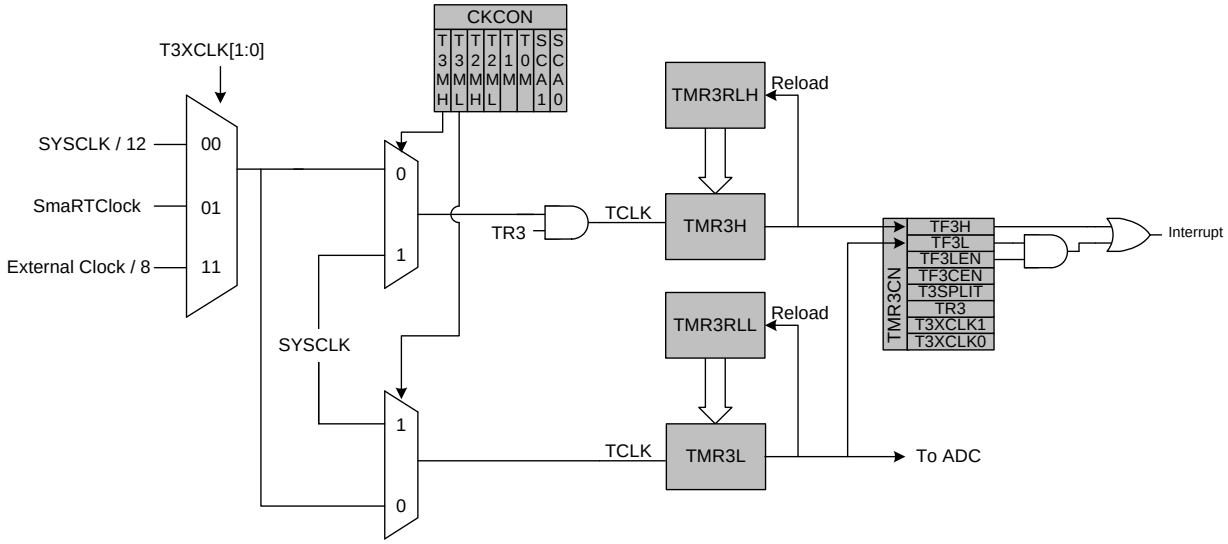


Figure 32.8. Timer 3 8-Bit Mode Block Diagram

### 32.3.3. SmaRTClock /External Oscillator Capture Mode

The Capture Mode in Timer 3 allows either SmaRTClock or the external oscillator period to be measured against the system clock or the system clock divided by 12. SmaRTClock and the external oscillator period can also be compared against each other.

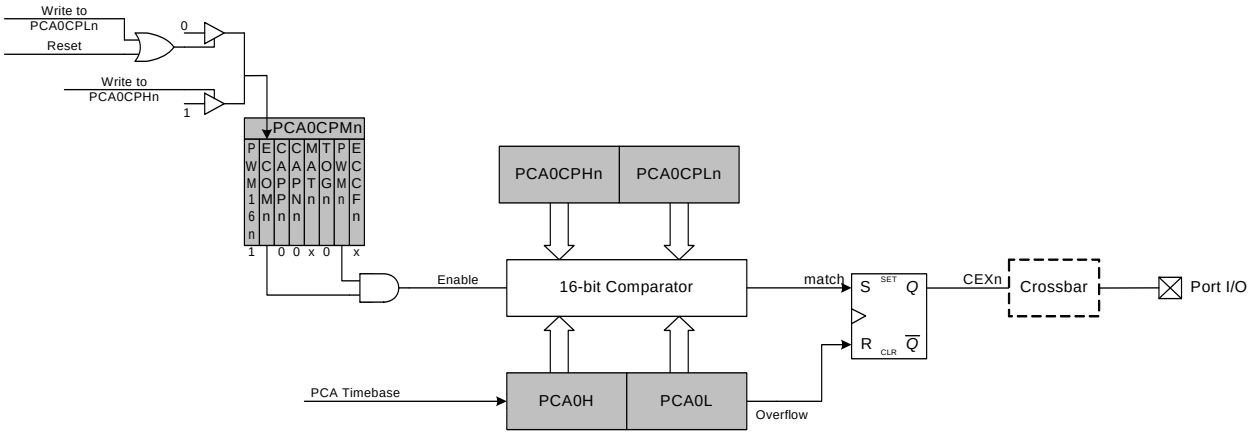


Figure 33.10. PCA 16-Bit PWM Mode

## 33.4. Watchdog Timer Mode

A programmable watchdog timer (WDT) function is available through the PCA Module 5. The WDT is used to generate a reset if the time between writes to the WDT update register (PCA0CPH2) exceed a specified limit. The WDT can be configured and enabled/disabled as needed by software.

With the WDTE bit set in the PCA0MD register, Module 5 operates as a watchdog timer (WDT). The Module 5 high byte is compared to the PCA counter high byte; the Module 5 low byte holds the offset to be used when WDT updates are performed. The Watchdog Timer is enabled on reset. Writes to some PCA registers are restricted while the Watchdog Timer is enabled. The WDT will generate a reset shortly after code begins execution. To avoid this reset, the WDT should be explicitly disabled (and optionally re-configured and re-enabled if it is used in the system).

### 33.4.1. Watchdog Timer Operation

While the WDT is enabled:

- PCA counter is forced on.
- Writes to PCA0L and PCA0H are not allowed.
- PCA clock source bits (CPS2–CPS0) are frozen.
- PCA Idle control bit (CIDL) is frozen.
- Module 5 is forced into software timer mode.
- Writes to the Module 5 mode register (PCA0CPM5) are disabled.

While the WDT is enabled, writes to the CR bit will not change the PCA counter state; the counter will run until the WDT is disabled. The PCA counter run control bit (CR) will read zero if the WDT is enabled but user software has not enabled the PCA counter. If a match occurs between PCA0CPH5 and PCA0H while the WDT is enabled, a reset will be generated. To prevent a WDT reset, the WDT may be updated with a write of any value to PCA0CPH5. Upon a PCA0CPH5 write, PCA0H plus the offset held in PCA0CPL5 is loaded into PCA0CPH5. (See Figure 33.11.)

## 34.2. C2 Pin Sharing

The C2 protocol allows the C2 pins to be shared with user functions so that in-system debugging and Flash programming may be performed. This is possible because C2 communication is typically performed when the device is in the halt state, where all on-chip peripherals and user software are stalled. In this halted state, the C2 interface can safely ‘borrow’ the C2CK (RST) and C2D pins. In most applications, external resistors are required to isolate C2 interface traffic from the user application. A typical isolation configuration is shown in Figure 34.1.

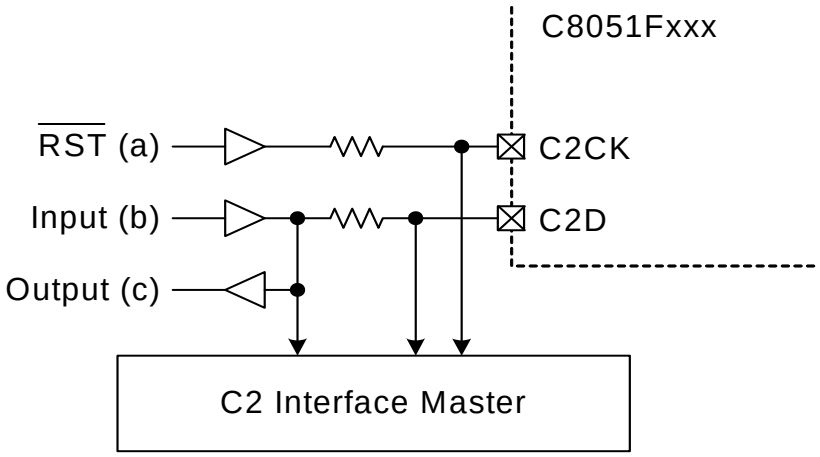


Figure 34.1. Typical C2 Pin Sharing

The configuration in Figure 34.1 assumes the following:

1. The user input (b) cannot change state while the target device is halted.
2. The RST pin on the target device is used as an input only.

Additional resistors may be necessary depending on the specific application.