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Details

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Product Status	Not For New Designs
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	EBI/EMI, Serial Port
Peripherals	POR, WDT
Number of I/O	36
Program Memory Size	-
Program Memory Type	ROMIess
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w77ic32a25pl

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80h				Indirect	RAM				
7Fh									1
0.01-				Direct	RAM				
30N 2Eh	75	75	70	70	7B	74	70	78	1
2Fh	77	76	75	70	73	72	75	70	1
2Dh	6F	6F	6D	60	6B	64	69	68	1
2Ch	67	66	65	64	63	62	61	60	1
2Bh	5F	5E	5D	5C	5B	5A	59	58	1
2Ah	57	56	55	54	53	52	51	50	1
29h	4F	4E	4D	4C	4B	4A	49	48	
28h	47	46	45	44	43	42	41	40	Bit Addressable
27h	3F	3E	3D	3C	3B	3A	39	38	
26h	37	36	35	34	33	32	31	30	20H–2FH
25h	2F	2E	2D	2C	2B	2A	29	28]
24h	27	26	25	24	23	22	21	20	
23h	1F	1E	1D	1C	1B	1A	19	18	
22h	17	16	15	14	13	12	11	10	
21h	0F	0E	0D	0C	0B	0A	09	08	4
20h	07	06	05	04	03	02	01	00	↓ '
1Fh				Banl	k 3				
18N 17h									4
10h				Banl	k 2				
0Fh				Ban	z 1				1
08h				Dalli					
07h				Banl	k ()				
00h				Ban]

Figure 2. Scratchpad RAM / Register Addressing



MD2-0: Stretch MOVX select bits: These three bits are used to select the stretch value for the MOVX instruction. Using a variable MOVX length enables the user to access slower external memory devices or peripherals without the need for external circuits. The RD or WR strobe will be stretched by the selected interval. When accessing the on-chip SRAM, the MOVX instruction is always in 2 machine cycles regardless of the stretch setting. By default, the stretch has value of 1. If the user needs faster accessing, then a stretch value of 0 should be selected.

MD2	MD1	MD0	Stretch value	MOVX duration
0	0	0	0	2 machine cycles
0	0	1	1	3 machine cycles (Default)
0	1	0	2	4 machine cycles
0	1	1	3	5 machine cycles
1	0	0	4	6 machine cycles
1	0	1	5	7 machine cycles
1	1	0	6	8 machine cycles
1	1	1	7	9 machine cycles

Port 1

Bit:	7	6	5	4	3	2	1	0
	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
Mnemonic: P1						Addre	ess: 90h	

- P1.7-0: General purpose I/O port. Most instructions will read the port pins in case of a port read access, however in case of read-modify-write instructions, the port latch is read. Some pins also have alternate input or output functions. This alternate functions are described below:
 - P1.0 : T2 External I/O for Timer/Counter 2 P1.1 : T2EX Timer/Counter 2 Capture/Reload Trigger P1.2 : RXD1 Serial Port 1 Receive P1.3 : TXD1 Serial Port 1 Transmit P1.4 : INT2 **External Interrupt 2** P1.5 : INT3 **External Interrupt 3** P1.6 : INT4 **External Interrupt 4** P1.7 : INT5 **External Interrupt 5**

External Interrupt Flag



IE5: External Interrupt 5 flag. Set by hardware when a falling edge is detected on INT5.

IE4: External Interrupt 4 flag. Set by hardware when a rising edge is detected on INT4.

IE3: External Interrupt 3 flag. Set by hardware when a falling edge is detected on INT5 .

IE2: External Interrupt 2 flag. Set by hardware when a rising edge is detected on INT2.



Table 3. Instruction Timing for W77IC32, continued

INSTRUCTION	HEX OP-CODE	BYTES	W77IC32 MACHINE CYCLES	W77IC32 CLOCK CYCLES	8032 CLOCK CYCLES	W77IC32 VS. 8032 SPEED RATIO
MOV @R0, direct	A6	2	2	8	12	1.5
MOV @R1, direct	A7	2	2	8	12	1.5
MOV @R0, #data	76	2	2	8	12	1.5
MOV @R1, #data	77	2	2	8	12	1.5
MOV direct, A	F5	2	2	8	12	1.5
MOV direct, R0	88	2	2	8	12	1.5
MOV direct, R1	89	2	2	8	12	1.5
MOV direct, R2	8A	2	2	8	12	1.5
MOV direct, R3	8B	2	2	8	12	1.5
MOV direct, R4	8C	2	2	8	12	1.5
MOV direct, R5	8D	2	2	8	12	1.5
MOV direct, R6	8E	2	2	8	12	1.5
MOV direct, R7	8F	2	2	8	12	1.5
MOV direct, @R0	86	2	2	8	12	1.5
MOV direct, @R1	87	2	2	8	12	1.5
MOV direct, direct	85	3	3	12	24	2
MOV direct, #data	75	3	3	12	24	2
MOV DPTR, #data 16	90	3	3	12	24	2
MOVC A, @A+DPTR	93	1	2	8	24	3
MOVC A, @A+PC	83	1	2	8	24	3
MOVX A, @R0	E2	1	2 - 9	8 - 36	24	3 - 0.66
MOVX A, @R1	E3	1	2 - 9	8 - 36	24	3 - 0.66
MOVX A, @DPTR	E0	1	2 - 9	8 - 36	24	3 - 0.66
MOVX @R0, A	F2	1	2 - 9	8 - 36	24	3 - 0.66
MOVX @R1, A	F3	1	2 - 9	8 - 36	24	3 - 0.66
MOVX @DPTR, A	F0	1	2 - 9	8 - 36	24	3 - 0.66
MOV C, bit	A2	2	2	8	12	1.5
MOV bit, C	92	2	2	8	24	3
ORL A, R0	48	1	1	4	12	3
ORL A, R1	49	1	1	4	12	3
ORL A, R2	4A	1	1	4	12	3
ORL A, R3	4B	1	1	4	12	3



Table 3. Instruction Timing for W77IC32, continued

INSTRUCTION	HEX OP-CODE	BYTES	W77IC32 MACHINE CYCLES	W77IC32 CLOCK CYCLES	8032 CLOCK CYCLES	W77IC32 VS. 8032 SPEED RATIO
ORL A, R4	4C	1	1	4	12	3
ORL A, R5	4D	1	1	4	12	3
ORL A, R6	4E	1	1	4	12	3
ORL A, R7	4F	1	1	4	12	3
ORL A, @R0	46	1	1	4	12	3
ORL A, @R1	47	1	1	4	12	3
ORL A, direct	45	2	2	8	12	1.5
ORL A, #data	44	2	2	8	12	1.5
ORL direct, A	42	2	2	8	12	1.5
ORL direct, #data	43	3	3	12	24	2
ORL C, bit	72	2	2	8	24	3
ORL C, /bit	A0	2	2	6	24	3
PUSH direct	C0	2	2	8	24	3
POP direct	D0	2	2	8	24	3
RET	22	1	2	8	24	3
RETI	32	1	2	8	24	3
RL A	23	1	1	4	12	3
RLC A	33	1	1	4	12	3
RR A	03	1	1	4	12	3
RRC A	13	1	1	4	12	3
SETB C	D3	1	1	4	12	3
SETB bit	D2	2	2	8	12	1.5
SWAP A	C4	1	1	4	12	3
SJMP rel	80	2	3	12	24	2
SUBB A, R0	98	1	1	4	12	3
SUBB A, R1	99	1	1	4	12	3
SUBB A, R2	9A	1	1	4	12	3
SUBB A, R3	9B	1	1	4	12	3
SUBB A, R4	9C	1	1	4	12	3
SUBB A, R5	9D	1	1	4	12	3
SUBB A, R6	9E	1	1	4	12	3
SUBB A, R7	9F	1	1	4	12	3

W77IC32



Figure 6: Four Cycle Instruction Timing



Figure 7: Five Cycle Instruction Timing



7.1.1 MOVX Instruction

The W77IC32, like the standard 8032, uses the MOVX instruction to access external Data Memory. This Data Memory includes both off-chip memory as well as memory mapped peripherals. While the results of the MOVX instruction are the same as in the standard 8032, the operation and the timing of the strobe signals have been modified in order to give the user much greater flexibility.

The MOVX instruction is of two types, the MOVX @Ri and MOVX @DPTR. In the MOVX @Ri, the address of the external data comes from two sources. The lower 8-bits of the address are stored in the Ri register of the selected working register bank. The upper 8-bits of the address come from the port 2 SFR. In the MOVX @DPTR type, the full 16-bit address is supplied by the Data Pointer.

Since the W77IC32 has two Data Pointers, DPTR and DPTR1, the user has to select between the two by setting or clearing the DPS bit. The Data Pointer Select bit (DPS) is the LSB of the DPS SFR, which exists at location 86h. No other bits in this SFR have any effect, and they are set to 0. When DPS is 0, then DPTR is selected, and when set to 1, DPTR1 is selected. The user can switch between DPTR and DPTR1 by toggling the DPS bit. The quickest way to do this is by the INC instruction. The advantage of having two Data Pointers is most obvious while performing block move operations. The accompanying code shows how the use of two separate Data Pointers speeds up the execution time for code performing the same task.

Block Move with single Data Pointer:

- ; SH and SL are the high and low bytes of Source Address
- ; DH and DL are the high and low bytes of Destination Address
- ; CNT is the number of bytes to be moved

Machine cycles of W77IC32

			m
MOV	R2, #CNT	; Load R2 with the count value	2
MOV	R3, #SL	; Save low byte of Source Address in R3	2
MOV	R4, #SH	; Save high byte of Source address in R4	2
MOV	R5, #DL	; Save low byte of Destination Address in R5	2
MOV	R6, #DH	; Save high byte of Destination address in R6	2
LOOP:			
MOV	DPL, R3	; Load DPL with low byte of Source address	2
MOV	DPH, R4	; Load DPH with high byte of Source address	2
MOVX	A, @DPTR	; Get byte from Source to Accumulator	2
INC	DPTR	; Increment Source Address to next byte	2
MOV	R3, DPL	; Save low byte of Source address in R3	2
MOV	R4, DPH	; Save high byte of Source Address in R4	2
MOV	DPL, R5	; Load low byte of Destination Address in DPL	2
MOV	DPH, R6	; Load high byte of Destination Address in DPH	2
MOVX	@DPTR, A	; Write data to destination	2
INC	DPTR	; Increment Destination Address	2
MOV	DPL, R5	; Save low byte of new destination address in R5	2
MOV	DPH, R6	; Save high byte of new destination address in R6	2
DJNZ	R2, LOOP	; Decrement count and do LOOP again if count <> 0	2



Vinbond

Figure 9: Dada Memory Write with Stretch Value = 1



Figure 10: Dada Memory Write with Stretch Value = 2



Wait State Control Signal

Either with the software using stretch value to change the required machine cycle of MOVX instruction, the W77IC32 provides another hardware signal WAIT to implement the wider duration of external data access timing. This wait state control signal is the alternate function of P4.0 such that it can only be invoked to 44-pin PLCC/QFP package type. The wait state control signal can be enabled by setting WS (ROMMAP.7) bit. When enabled, the setting of stretch value decides the minimum length of MOVX instruction cycle and the device will sample the WAIT pin at each C3 state before the rising edge of read/write strobe signal during MOVX instruction. Once this signal being recongnized, one more machine cycle (wait state cycle) will be inserted into next cycle. The inserted wait state cycles are unlimited, so the MOVX instruction cycle will end in which the wait state control signal is deactivated. Using wait state control signal allows a dynamically access timing to a selected external peripheral. The WS bit is accessed by the Timed Access Protection procedure.



Wait State Control Signal Timing (when Stretch = 1)

Wait State Control Signal Timing (when Stretch = 2)





8. POWER MANAGEMENT

The W77IC32 has several features that help the user to modify the power consumption of the device. The power saving features are basically the POWER DOWN mode, ECONOMY mode and the IDLE mode of operation.

8.1 Idle Mode

The user can put the device into idle mode by writing 1 to the bit PCON.0. The instruction that sets the idle bit is the last instruction that will be executed before the device goes into Idle Mode. In the Idle mode, the clock to the CPU is halted, but not to the Interrupt, Timer, Watchdog timer and Serial port blocks. This forces the CPU state to be frozen; the Program counter, the Stack Pointer, the Program Status Word, the Accumulator and the other registers hold their contents. The ALE and PSEN pins are held high during the Idle state. The port pins hold the logical states they had at the time Idle was activated. The Idle mode can be terminated in two ways. Since the interrupt controller is still active, the activation of any enabled interrupt can wake up the processor. This will automatically clear the Idle bit, terminate the Idle mode, and the Interrupt Service Routine (ISR) will be executed. After the ISR, execution of the program will continue from the instruction which put the device into Idle mode.

The Idle mode can also be exited by activating the reset. The device can be put into reset either by applying a high on the external RST pin, a Power on/fail reset condition or a Watchdog timer reset. The external reset pin has to be held high for at least two machine cycles I.e. 8 clock periods to be recognized as a valid reset. In the reset condition the program counter is reset to 0000h and all the SFRs are set to the reset condition. Since the clock is already running there is no delay and execution starts immediately. In the Idle mode, the Watchdog timer continues to run, and if enabled, a time-out will cause a watchdog timer interrupt which will wake up the device. The software must reset the Watchdog timer in order to preempt the reset which will occur after 512 clock periods of the time-out. When the W77IC32 is exiting from an Idle mode with a reset, the instruction following the one which put the device into Idle mode is not executed. So there is no danger of unexpected writes.

8.2 Economy Mode

The power consumption of microcontroller relates to operating frequency. The W77IC32 offers a Economy mode to reduce the internal clock rate dynamically without external components. By default, one machine cycle needs 4 clocks. In Economy mode, software can select 4, 64 or 1024 clocks per machine cycle. It keeps the CPU operating at a acceptable speed but eliminates the power consumption. In the Idle mode, the clock of the core logic is stopped, b+ut all clocked peripherals such as watchdog timer are still running at a rate of clock/4. In the Economy mode, all clocked peripherals run at the same reduced clocks rate as in core logic. So the Economy mode may provide a lower power consumption than idle mode.

Software invokes the Economy mode by setting the appropriate bits in the SFRs. Setting the bits CD0(PMR.6),CD1(PMR.7) decides the instruction cycle rate as below:

CD1 CD0 CLOCKS/MACHINE CYCLE

- 0 0 Reserved
- 0 1 4 (default)
- 1 0 64
- 1 1 1024



9. RESET CONDITIONS

The user has several hardware related options for placing the W77IC32 into reset condition. In general, most register bits go to their reset value irrespective of the reset condition, but there are a few flags whose state depends on the source of reset. The user can use these flags to determine the cause of reset using software. There are ways of putting the device into reset state, external reset and watchdog reset.

9.1 External Reset

The device continuously samples the RST pin at state C4 of every machine cycle. Therefore the RST pin must be held for at least 2 machine cycles to ensure detection of a valid RST high. The reset circuitry then synchronously applies the internal reset signal. Thus the reset is a synchronous operation and requires the clock to be running to cause an external reset.

Once the device is in reset condition, it will remain so as long as RST is 1. Even after RST is deactivated, the device will continue to be in reset state for up to two machine cycles, and then begin program execution from 0000h. There is no flag associated with the external reset condition. However since the other two reset sources have flags, the external reset can be considered as the default reset if those two flags are cleared.

9.2 Watchdog Timer Reset

The Watchdog timer is a free running timer with programmable time-out intervals. The user can clear the watchdog timer at any time, causing it to restart the count. When the time-out interval is reached an interrupt flag is set. If the Watchdog reset is enabled and the watchdog timer is not cleared, then 512 clocks from the flag being set, the watchdog timer will generate a reset. This places the device into the reset condition. The reset condition is maintained by hardware for two machine cycles. Once the reset is removed the device will begin execution from 0000h.

9.3 Reset State

Most of the SFRs and registers on the device will go to the same condition in the reset state. The Program Counter is forced to 0000h and is held there as long as the reset condition is applied. However, the reset state does not affect the on-chip RAM. The data in the RAM will be preserved during the reset. However, the stack pointer is reset to 07h, and therefore the stack contents will be lost. The RAM contents will be lost if the VDD falls below approximately 2V, as this is the minimum voltage level required for the RAM to operate normally. Therefore after a first time power on reset the RAM contents will be indeterminate. During a power fail condition, if the power falls below 2V, the RAM contents are lost. Hence it should be assumed that after a power fail, the RAM contents are lost.

After a reset most SFRs are cleared. Interrupts and Timers are disabled. The Watchdog timer is disabled if the reset source was a POR. The port SFRs have FFh written into them which puts the port pins in a high state. Port 0 floats as it does not have on-chip pull-ups.



10. INTERRUPTS

The W77IC32 has a two priority level interrupt structure with 12 interrupt sources. Each of the interrupt sources has an individual priority bit, flag, interrupt vector and enable bit. In addition, the interrupts can be globally enabled or disabled.

10.1 Interrupt Sources

The External Interrupts INTO and INT1 can be either edge triggered or level triggered, depending on bits ITO and IT1. The bits IEO and IE1 in the TCON register are the flags which are checked to generate the interrupt. In the edge triggered mode, the INTx inputs are sampled in every machine cycle. If the sample is high in one cycle and low in the next, then a high to low transition is detected and the interrupts request flag IEx in TCON or EXIF is set. The flag bit requests the interrupt. Since the external interrupts are sampled every machine cycle, they have to be held high or low for at least one complete machine cycle. The IEx flag is automatically cleared when the service routine is called. If the level triggered mode is selected, then the requesting source has to hold the pin low till the interrupt is serviced. The IEx flag will not be cleared by the hardware on entering the service routine. If the interrupt continues to be held low even after the service routine is completed, then the processor may acknowledge another interrupt request from the same source. Note that the external interrupts INT2 to

INT5 are edge triggered only. By default, the individual interrupt flag corresponding to external interrupt 2 to 5 must be cleared manually by software. It can be configured with hardware cleared by setting the corresponding bit HCx in the T2MOD register. For instance, if HC2 is set hardware will clear IE2 flag after program enters the interrupt 2 service routine.

The Timer 0 and 1 Interrupts are generated by the TF0 and TF1 flags. These flags are set by the overflow in the Timer 0 and Timer 1. The TF0 and TF1 flags are automatically cleared by the hardware when the timer interrupt is serviced. The Timer 2 interrupt is generated by a logical OR of the TF2 and the EXF2 flags. These flags are set by overflow or capture/reload events in the timer 2 operation. The hardware does not clear these flags when a timer 2 interrupt is executed. Software has to resolve the cause of the interrupt between TF2 and EXF2 and clear the appropriate flag.

The Watchdog timer can be used as a system monitor or a simple timer. In either case, when the time-out count is reached, the Watchdog timer interrupt flag WDIF (WDCON.3) is set. If the interrupt is enabled by the enable bit EIE.4, then an interrupt will occur.

The Serial block can generate interrupts on reception or transmission. There are two interrupt sources from the Serial block, which are obtained by the RI and TI bits in the SCON SFR and RI_1 and TI_1 in the SCON1 SFR. These bits are not automatically cleared by the hardware, and the user will have to clear these bits using software.

All the bits that generate interrupts can be set or reset by hardware, and thereby software initiated interrupts can be generated. Each of the individual interrupts can be enabled or disabled by setting or clearing a bit in the IE SFR. IE also has a global enable/disable bit EA, which can be cleared to disable all the interrupt, at once.

any errant code is executed now, then the reset watchdog timer instructions will not be executed at the required instants and watchdog reset will occur.

The watchdog time-out selection will result in different time-out values depending on the clock speed. The reset, when enabled, will occur 512 clocks after the time-out has occurred.

WD1	WD0	WATCHDOG INTERVAL	NUMBER OF CLOCKS	TIME @1.8432 MHZ	TIME @10 MHZ	TIME @25 MHZ
0	0	2 ¹⁷	131072	71.11 mS	13.11 mS	5.24 mS
0	1	2 ²⁰	1048576	568.89 mS	104.86 mS	41.94 mS
1	0	2 ²³	8388608	4551.11 mS	838.86 mS	335.54 mS
1	1	2 ²⁶	67108864	36408.88 mS	6710.89 mS	2684.35 mS

Table 9. Time-out values for the Watchdog timer

The Watchdog timer will de disabled by a power-on/fail reset. The Watchdog timer reset does not disable the watchdog timer, but will restart it. In general, software should restart the timer to put it into a known state.

The control bits that support the Watchdog timer are discussed below.

WATCHDOG CONTROL

- WDIF: WDCON.3 Watchdog Timer Interrupt flag. This bit is set whenever the time-out occurs in the watchdog timer. If the Watchdog interrupt is enabled (EIE.4), then an interrupt will occur (if the global interrupt enable is set and other interrupt requirements are met). Software or any reset can clear this bit.
- WTRF: WDCON.2 Watchdog Timer Reset flag. This bit is set whenever a watchdog reset occurs. This bit is useful for determined the cause of a reset. Software must read it, and clear it manually. A Power-fail reset will clear this bit. If EWT = 0, then this bit will not be affected by the watchdog timer.
- EWT: WDCON.1 Enable Watchdog timer Reset. This bit when set to 1 will enable the Watchdog timer reset function. Setting this bit to 0 will disable the Watchdog timer reset function, but will leave the timer running
- RWT: WDCON.0 Reset Watchdog Timer. This bit is used to clear the Watchdog timer and to restart it. This bit is self-clearing, so after the software writes 1 to it the hardware will automatically clear it. If the Watchdog timer reset is enabled, then the RWT has to be set by the user within 512 clocks of the time-out. If this is not done then a Watchdog timer reset will occur.

CLOCK CONTROL

WD1, WD0: CKCON.7, CKCON.6 - Watchdog Timer Mode select bits. These two bits select the timeout interval for the watchdog timer. The reset time is 512 clock longer than the interrupt time-out value.

The default Watchdog time-out is 2¹⁷ clocks, which is the shortest time-out period. The EWT, WDIF and RWT bits are protected by the Timed Access procedure. This prevents software from accidentally enabling or disabling the watchdog timer. More importantly, it makes it highly improbable that errant code can enable or disable the watchdog timer.



The TI flag is set high in C1 following the end of transmission of the last bit. The serial port will receive data when REN is 1 and RI is zero. The shift clock (TxD) will be activated and the serial port will latch data on the rising edge of shift clock. The external device should therefore present data on the falling edge on the shift clock. This process continues till all the 8 bits have been received. The RI flag is set in C1 following the last rising edge of the shift clock on TxD. This will stop reception, till the RI is cleared by software.

11.6.2 Mode 1

In Mode 1, the full duplex asynchronous mode is used. Serial communication frames are made up of 10 bits transmitted on TXD and received on RXD. The 10 bits consist of a start bit (0), 8 data bits (LSB first), and a stop bit (1). On receive, the stop bit goes into RB8 in the SFR SCON. The baud rate in this mode is variable. The serial baud can be programmed to be 1/16 or 1/32 of the Timer 1 overflow. Since the Timer 1 can be set to different reload values, a wide variation in baud rates is possible.

Transmission begins with a write to SBUF. The serial data is brought out on to TxD pin at C1 following the first roll-over of divide by 16 counter. The next bit is placed on TxD pin at C1 following the next rollover of the divide by 16 counter. Thus the transmission is synchronized to the divide by 16 counter and not directly to the write to SBUF signal. After all 8 bits of data are transmitted, the stop bit is transmitted. The TI flag is set in the C1 state after the stop bit has been put out on TxD pin. This will be at the 10th rollover of the divide by 16 counter after a write to SBUF.

Reception is enabled only if REN is high. The serial port actually starts the receiving of serial data, with the detection of a falling edge on the RxD pin. The 1-to-0 detector continuously monitors the RxD line, sampling it at the rate of 16 times the selected baud rate. When a falling edge is detected, the divide by 16 counter is immediately reset. This helps to align the bit boundaries with the rollovers of the divide by 16 counter.

The 16 states of the counter effectively divide the bit time into 16 slices. The bit detection is done on a best of three basis. The bit detector samples the RxD pin, at the 8th, 9th and 10th counter states. By using a majority 2 of 3 voting system, the bit value is selected. This is done to improve the noise rejection feature of the serial port. If the first bit detected after the falling edge of RxD pin is not 0, then this indicates an invalid start bit, and the reception is immediately aborted. The serial port again looks for a falling edge in the RxD line. If a valid start bit is detected, then the rest of the bits are also detected and shifted into the SBUF.

After shifting in 8 data bits, there is one more shift to do, after which the SBUF and RB8 are loaded and RI is set. However certain conditions must be met before the loading and setting of RI can be done.

- 1. RI must be 0 and
- 2. Either SM2 = 0, or the received stop bit = 1.

If these conditions are met, then the stop bit goes to RB8, the 8 data bits go into SBUF and RI is set. Otherwise the received frame may be lost. After the middle of the stop bit, the receiver goes back to looking for a 1-to-0 transition on the RxD pin.



11.6.5 Framing Error Detection

A Frame Error occurs when a valid stop bit is not detected. This could indicate incorrect serial data communication. Typically the frame error is due to noise and contention on the serial communication line. The W77IC32 has the facility to detect such framing errors and set a flag which can be checked by software.

The Frame Error FE(FE_1) bit is located in SCON.7(SCON1.7). This bit is normally used as SM0 in the standard 8051 family. However, in the W77IC32 it serves a dual function and is called SM0/FE (SM0_1/FE_1). There are actually two separate flags, one for SM0 and the other for FE. The flag that is actually accessed as SCON.7(SCON1.7) is determined by SMOD0 (PCON.6) bit. When SMOD0 is set to 1, then the FE flag is indicated in SM0/FE. When SMOD0 is set to 0, then the SM0 flag is indicated in SM0/FE.

The FE bit is set to 1 by hardware but must be cleared by software. Note that SMOD0 must be 1 while reading or writing to FE or FE_1. If FE is set, then any following frames received without any error will not clear the FE flag. The clearing has to be done by software.

Multiprocessor Communications

Multiprocessor communications makes use of the 9th data bit in modes 2 and 3. In the W77IC32, the RI flag is set only if the received byte corresponds to the Given or Broadcast address. This hardware feature eliminates the software overhead required in checking every received address, and greatly simplifies the software programmer task.

In the multiprocessor communication mode, the address bytes are distinguished from the data bytes by transmitting the address with the 9th bit set high. When the master processor wants to transmit a block of data to one of the slaves, it first sends out the address of the targeted slave (or slaves). All the slave processors should have their SM2 bit set high when waiting for an address byte. This ensures that they will be interrupted only by the reception of a address byte. The Automatic address recognition feature ensures that only the addressed slave will be interrupted. The address comparison is done in hardware not software.

The addressed slave clears the SM2 bit, thereby clearing the way to receive data bytes. With SM2 = 0, the slave will be interrupted on the reception of every single complete frame of data. The unaddressed slaves will be unaffected, as they will be still waiting for their address. In Mode 1, the 9th bit is the stop bit, which is 1 in case of a valid frame. If SM2 is 1, then RI is set only if a valid frame is received and the received byte matches the Given or Broadcast address.

The Master processor can selectively communicate with groups of slaves by using the Given Address. All the slaves can be addressed together using the Broadcast Address. The addresses for each slave are defined by the SADDR and SADEN SFRs. The slave address is an 8-bit value specified in the SADDR SFR. The SADEN SFR is actually a mask for the byte value in SADDR. If a bit position in SADEN is 0, then the corresponding bit position in SADDR is don't care. Only those bit positions in SADDR whose corresponding bits in SADEN are 1 are used to obtain the Given Address. This gives the user flexibility to address multiple slaves without changing the slave address in SADDR.

The following example shows how the user can define the Given Address to address different slaves.

Slave 1:

SADDR 1010 0100 SADEN 1111 1010 Given 1010 0x0x



14. AC CHARACTERISTICS



14.1 External Clock Characteristics

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Clock High Time	t _{CHCX}	20	-	-	nS	
Clock Low Time	t _{CLCX}	20	-	-	nS	
Clock Rise Time	t _{CLCH}	-	-	10	nS	
Clock Fall Time	t _{CHCL}	-	-	10	nS	

Note: Duty cycle is 50 %.

14.2 AC Specification

PARAMETER	SYM.	VARIABLE CLOCK MIN.	VARIABLE CLOCK MAX.	UNITS
Oscillator Frequency	1/t _{CLCL}	0	25	MHz
ALE Pulse Width	t _{LHLL}	1.5 t _{CLCL} - 5		nS
Address Valid to ALE Low	t _{AVLL}	0.5 t _{CLCL} - 5		nS
Address Hold After ALE Low	t _{LLAX1}	0.5 t _{CLCL} - 5		nS
Address Hold After ALE Low for MOVX Write	t _{LLAX2}	0.5 t _{CLCL} - 5		nS
ALE Low to Valid Instruction In	t _{LLIV}		2.5 t _{CLCL} - 20	nS
ALE Low to PSEN Low	t _{LLPL}	0.5 t _{CLCL} - 5		nS
PSEN Pulse Width	t _{PLPH}	2.0 t _{CLCL} - 5		nS
PSEN Low to Valid Instruction In	t _{PLIV}		2.0 t _{CLCL} - 20	nS
Input Instruction Hold After PSEN	t _{PXIX}	0		nS
Input Instruction Float After PSEN	t _{PXIZ}		t _{CLCL} - 5	nS
Port 0 Address to Valid Instr. In	t _{AVIV1}		3.0 t _{CLCL} - 20	nS
Port 2 Address to Valid Instr. In	t _{AVIV2}		3.5 t _{CLCL} - 20	nS
PSEN Low to Address Float	t _{PLAZ}	0		nS
Data Hold After Read	t _{RHDX}	0		nS
Data Float After Read	t _{RHDZ}		t _{CLCL} - 5	nS
RD Low to Address Float	t _{RLAZ}		0.5 t _{CLCL} - 5	nS



M2	M1	M0	MOVX CYCLES	T _{MCS}
0	0	0	2 machine cycles	0
0	0	1	3 machine cycles	4 t _{CLCL}
0	1	0	4 machine cycles	8 t _{CLCL}
0	1	1	5 machine cycles	12 t _{CLCL}
1	0	0	6 machine cycles	16 t _{CLCL}
1	0	1	7 machine cycles	20 t _{CLCL}
1	1	0	8 machine cycles	24 t _{CLCL}
1	1	1	9 machine cycles	28 t _{CLCL}

Explanation of Logic Symbols

In order to maintain compatibility with the original 8051 family, this device specifies the same parameter for each device, using the same symbols. The explanation of the symbols is as follows.

t	Time	А	Address
С	Clock	D	Input Data
Н	Logic level high	L	Logic level low
I	Instruction	Р	PSEN
Q	Output Data	R	RD signal
V	Valid	W	WR signal
Х	No longer a valid state	Z	Tri-state



Timing Waveforms, continued

15.3 Data Memory Write Cycle





Typical Application Circuits, continued

16.2 Expanded External Data Memory and Oscillator



Figure B



18. VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION	
A1	-	-	Initial Issued	
A2	-	-	-	
A3	April 18, 2005	18	Add Important Notice	
A 4	December 13, 2005 3 Add lead-free(RoHS) parts 8 69 Revise the maximum oscillator frequencies	3	Add lead-free(RoHS) parts	
A4		Revise the maximum oscillator frequency to 25MHz		
A5	October 02, 2006		Remove block diagram	

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