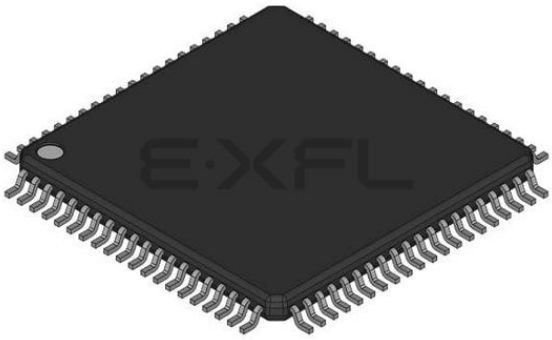

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V1
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, SCI, SPI
Peripherals	LCD, LVD, PWM, WDT
Number of I/O	56
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 12x16b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf51em128clk

1 MCF51EM256 Series Configurations

1.1 Device Comparison

The MCF51EM256 series is summarized in Table 1.

Table 1. MCF51EM256 Series Features by MCU and Package

Feature	MCF51EM256		MCF51EM128	
Flash size (bytes)	262144		131072	
RAM size (bytes)	16384		8192	
Robust flash update supported	Yes			
Pin quantity	100	80	100	80
PRACMP1 inputs	5	3	5	3
PRACMP2 inputs	5			
ADC modules	4		4	
ADC differential channels[1]	4	2	4	2
ADC single-ended channels	16	12	16	12
DBG	Yes			
ICS	Yes			
IIC	Yes			
IRQ	Yes			
IRTC	Yes			
VREF	Yes			
LCD drivers	44	37	44	37
Rapid GPIO[2]	16	16	16	16
Port I/O[3]	47	40	47	40
Keyboard interface 1	8			
Keyboard interface 2	8			
SCI1	Yes			
SCI2	Yes			
SCI3	Yes			
SPI1 (FIFO)	Yes			
SPI2 (standard)	Yes			
SPI3 (standard)	Yes	No	Yes	No

  - 6 μs typical wakeup time from stop3 mode
- Clock source options
  - Two independent oscillators (XOSC1 and XOSC2) — loop-control Pierce oscillator; 32.768 kHz crystal or ceramic resonator. XOSC1 nominally supports the independent real time clock, and can be powered by a separate battery backup. XOSC2 is the primary external clock source for the ICS
  - Internal clock source (ICS) — internal clock source module containing a frequency-locked-loop (FLL) controlled by internal or external reference (XOSC1 or XOSC2); precision trimming of internal reference allowing 0.2% resolution and typical 0.5% to –1% deviation over temperature and voltage; supporting CPU frequencies from 4 kHz to 50 MHz
- System protection
  - Watchdog computer operating properly (COP) reset with option to run from dedicated 1 kHz internal clock source or bus clock
  - Low voltage detection with reset or interrupt; selectable trip points; seperate low voltage warning with optional interrupt; selectable trip points
  - Illegal opcode and illegal address detection with reset
  - Flash block protection for each array to prevent accidental write/erasure
  - Hardware CRC module to support fast cyclic redundancy checks
- Development support
  - Integrated ColdFire DEBUG_Rev_B+ interface with single wire BDM connection supports same electrical interface used by the S08 family debug modules
  - Real-time debug support with six hardware breakpoints (4 PC, 1 address and 1 data)
  - On-chip trace buffer provides programmable start/stop recording conditions
- Peripherals
  - **ADC16** — 4 analog-to-digital converters; the 100 pin version of the device has 1 dedicated differential channel and 1 dedicated single-ended channel per ADC, along with 3 muxed single-ended channels per ADC. The ADCs have 16-bit resolution, range compare function, 1.7 mV/°C temperature sensor, internal bandgap reference channel, operate in stop3 and are fully functional from 3.6 V to 1.8 V
  - **PDB** — Programmable delay block with 16-bit counter and modulus and 3-bit prescaler; 8 trigger outputs for ADC16 modules (2 per ADC); provides periodic coordination of ADC sampling sequence with programmable sequence completion interrupt
  - **IRTC** — Ultra-low power independent real time clock with calendar features (IRTC); runs in all MCU modes; external clock source with trim capabilities (XOSC1); independent voltage source runs IRTC when MCU is powered-down; tamper detection and indicator; battery monitor output to ADC; unaffected by MCU resets
  - **PRACMPx** — Two analog comparators with selectable interrupt on rising, falling, or either edge of comparator output; compare option to programmable internal reference voltage; operation in stop3
  - **LCD** — up to 288 segments (8 × 36); 160 segments (4 × 40); internal charge pump and option to provide internal reference voltage that can be trimmed for contrast control; flexible

1.5.2 Pinout: 100-Pin LQFP

Figure 3 shows the pinout configuration for the 100-pin LQFP. Pins which are blacked out do not have an equivalent pin on the 80-pin LQFP package.

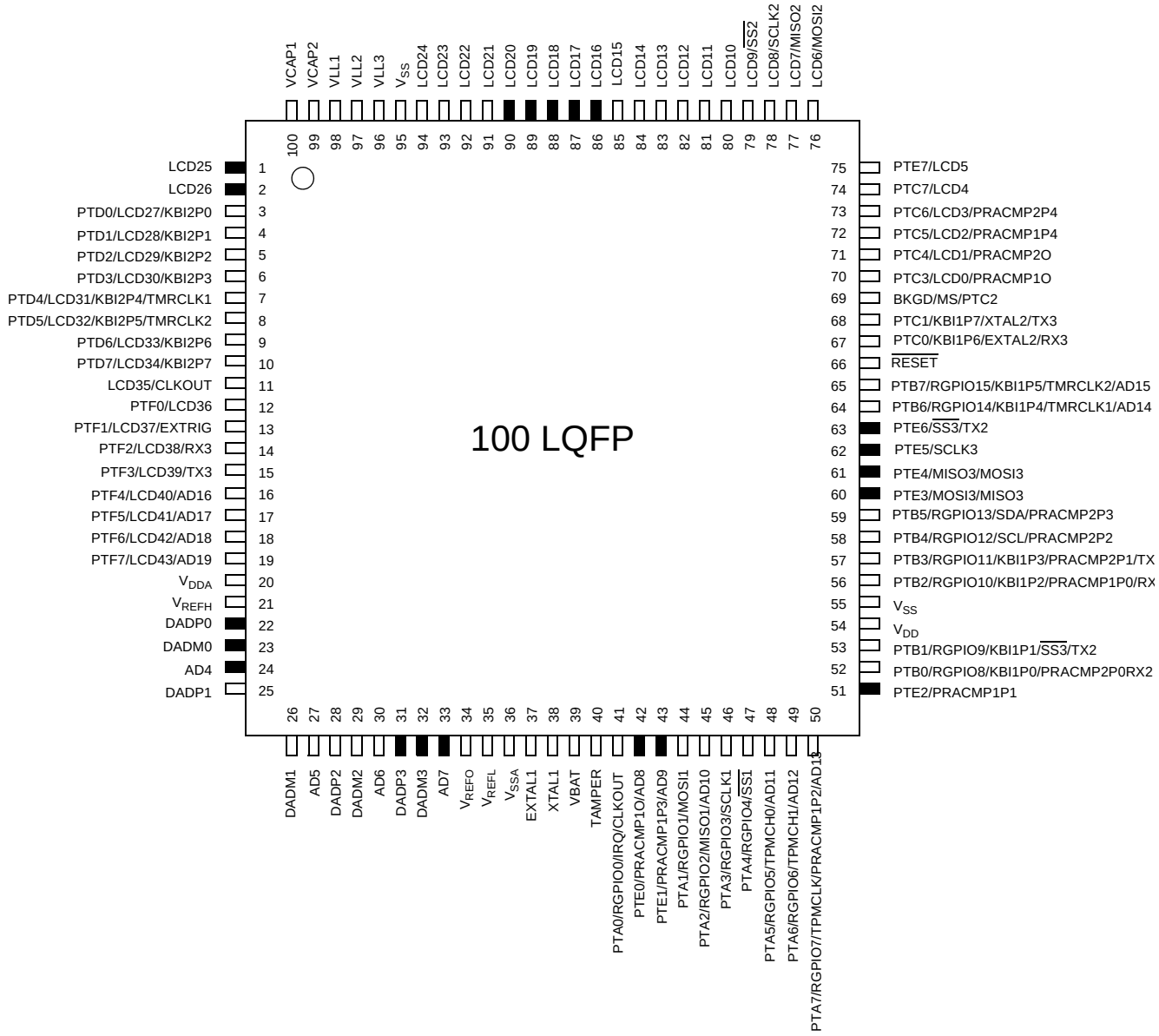


Figure 3. 100-Pin LQFP Pinout

Table 4 shows the package pin assignments.

Table 9. ESD and Latch-Up Protection Characteristics

Num	Rating	Symbol	Min	Max	Unit
1	Human Body Model (HBM)	V_{HBM}	±2000	—	V
2	Machine Model (MM)	V_{MM}	±200	—	V
3	Charge Device Model (CDM)	V_{CDM}	±500	—	V
4	Latch-up Current at T_A = 85 °C	I_{LAT}	±100	—	mA

2.5 DC Characteristics

This section includes information about power supply requirements, I/O pin characteristics, and power supply current in various operating modes.

Table 10. DC Characteristics

Num	C	Parameter		Symbol	Min	Typical[1]	Max	Unit
1	P	Operating voltage	Digital supply — 50 MHz operation	V_{DD}	2.5	—	3.6	V
			Digital supply[2] — 20 MHz maximum operation	V_{DD}	1.8	—	3.6	
2	P	Analog supply		V_{DDA}	1.8	—	3.6	V
3	D	Battery supply		V_{BAT}	2.2	3	3.3	V
4	P	Bandgap voltage reference[3]		V_{BG}	1.15	1.17	1.18	V
5	C	Output high voltage	PTA[7:0], PTB[7:0], PTC[2:0], PTE[6:0], low-drive strength. $V_{DD} \geq 1.8$ V, $I_{Load} = -0.6$ mA	V_{OH}	$V_{DD} - 0.5$	—	—	V
	P		PTA[7:0], PTB[7:0], PTC[2:0], PTE[6:0], high-drive strength. $V_{DD} \geq 2.7$ V, $I_{Load} = -10$ mA					
	C		PTA[7:0], PTB[7:0], PTC[2:0], PTE[6:0], high-drive strength. $V_{DD} \geq 1.8$ V, $I_{Load} = -3$ mA					
6	C	Output high voltage	PTC[7:3], PTD[7:0], PTE7, PTF[7:0], LCD35/CLKOUT, MOSI2, MISO2, SCK2, SS2, low drive strength. VDD ≥ 1.8 V, $I_{Load} = -0.5$ mA	V_{OH}	$V_{DD} - 0.5$	—	—	V
	P		PTC[7:3], PTD[7:0], PTE7, PTF[7:0], LCD35/CLKOUT, MOSI2, MISO2, SCK2, SS2, high-drive strength. $V_{DD} \geq 2.7$ V, $I_{Load} = -3$ mA					
	C		PTC[7:3], PTD[7:0], PTE7, PTF[7:0], LCD35/CLKOUT, MOSI2, MISO2, SCK2, SS2, high-drive strength. $V_{DD} \geq 1.8$ V, $I_{Load} = -1$ mA					
7	D	Output high current	Max total I_{OH} for all ports	I_{OHT}	—	—	100	mA

Table 10. DC Characteristics (continued)

Num	C	Parameter		Symbol	Min	Typical[1]	Max	Unit
8	C	Output low voltage	PTA[7:0], PTB[7:0], PTC[2:0], PTE[6:0], low-drive strength. $V_{DD} \geq 1.8$ V, $I_{Load} = 2$ mA	V_{OL}	—	—	0.50	V
	P		PTA[7:0], PTB[7:0], PTC[2:0], PTE[6:0], high-drive strength. $V_{DD} \geq 2.7$ V, $I_{Load} = 10$ mA					
	C		PTA[7:0], PTB[7:0], PTC[2:0], PTE[6:0], high-drive strength. $V_{DD} \geq 1.8$ V, $I_{Load} = 3$ mA					
9	C	Output low voltage	PTC[7:3], PTD[7:0], PTE7, PTF[7:0], LCD35/CLKOUT, MOSI2, MISO2, SCK2, SS2, low drive strength. VDD ≥ 1.8 V, $I_{Load} = 0.5$ mA	V_{OL}	—	—	0.50	V
	P		PTC[7:3], PTD[7:0], PTE7, PTF[7:0], LCD35/CLKOUT, MOSI2, MISO2, SCK2, SS2, high-drive strength. $V_{DD} \geq 2.7$ V, $I_{Load} = 3$ mA					
	C		PTC[7:3], PTD[7:0], PTE7, PTF[7:0], LCD35/CLKOUT, MOSI2, MISO2, SCK2, SS2, high-drive strength. $V_{DD} \geq 1.8$ V, $I_{Load} = 1$ mA					
10	D	Output low current	Max total I_{OL} for all ports	I_{OLT}	—	—	100	mA
11	P	Input high voltage	All digital inputs except tamper_in, $V_{DD} > 2.7$ V	V_{IH}	$0.70 \times V_{DD}$	—	—	V
			All digital inputs except tamper_in, $2.7 \text{ V} > V_{DD} \geq 1.8$ V		$0.85 \times V_{DD}$	—	—	
			Tamper_in		1.5	—	—	
12	P	Input low voltage	All digital inputs except tamper_in, $V_{DD} > 2.7$ V	V_{IL}	—	—	$0.35 \times V_{DD}$	V
			all digital inputs except tamper_in, $2.7 \text{ V} > V_{DD} \geq 1.8$ V		—	—	$0.3 \times V_{DD}$	
			Tamper_in		—	—	0.5	
13	C	Input hysteresis; all digital inputs		V_{hys}	$0.06 \times V_{DD}$	—	—	mV
14	P	Input leakage current; input only pins[4]		$\lvert I_{In} \rvert$	—	0.1	1	μA
15	P	High Impedance (off-state) leakage current[4]		$\lvert I_{OZ} \rvert$	—	0.1	1	μA
16	P	Internal pullup resistors[5]		R_{PU}	17.5	—	52.5	kΩ
17	P	Internal pulldown resistors[6]		R_{PD}	17.5	—	52.5	kΩ
18	C	Input capacitance; all non-supply pins		C_{In}	—	—	8	pF
19	P	POR rearm voltage		V_{POR}	0.9	1.4	2.0	V
20	D	POR rearm time		t_{POR}	10	—	—	μs
21	P	Low-voltage detection threshold	High range — V_{DD} falling	V_{LVDH}	2.300	2.355	2.410	V
			High range — V_{DD} rising		2.370	2.425	2.480	

Table 10. DC Characteristics (continued)

Num	C	Parameter		Symbol	Min	Typical[1]	Max	Unit
22	C	Low-voltage detection threshold	Low range — V_{DD} falling	V_{LVDL}	1.800	1.845	1.890	V
			Low range — V_{DD} rising		1.870	1.915	1.960	V
23	P	Low-voltage warning threshold	V_{DD} falling, LVWV = 1	V_{LVWH}	2.590	2.655	2.720	V
			V_{DD} rising, LVWV = 1		2.580	2.645	2.710	
24	C	Low-voltage warning	V_{DD} falling, LVWV = 0	V_{LVWL}	2.300	2.355	2.410	V
			V_{DD} rising, LVWV = 0		2.360	2.425	2.490	
25	D	RAM retention voltage		V_{RAM}	—	0.6	1.0	V
26	D	DC injection current[7 8 9 10] (single pin limit), $V_{IN} > V_{DD}$, $V_{IN} < V_{SS}$		I_{IC}	–0.2	—	0.2	mA
		DC injection current (Total MCU limit, includes sum of all stressed pins), $V_{IN} > V_{DD}$, $V_{IN} < V_{SS}$			–5	—	5	mA

1 Typical values are based on characterization data at 25 °C unless otherwise stated.

2 Switch to lower frequency when the low-voltage interrupt asserts (V_{LVDH}).

3 Factory trimmed at V_{DD} = 3.0 V, Temp = 25°C

4 Measured with $V_{In} = V_{DD}$ or V_{SS}.

5 Measured with $V_{In} = V_{SS}$.

6 Measured with $V_{In} = V_{DD}$.

7 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

8 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

9 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

10 The $\overline{\text{RESET}}$ pin does not have a clamp diode to V_{DD}. Do not drive this pin above V_{DD}.

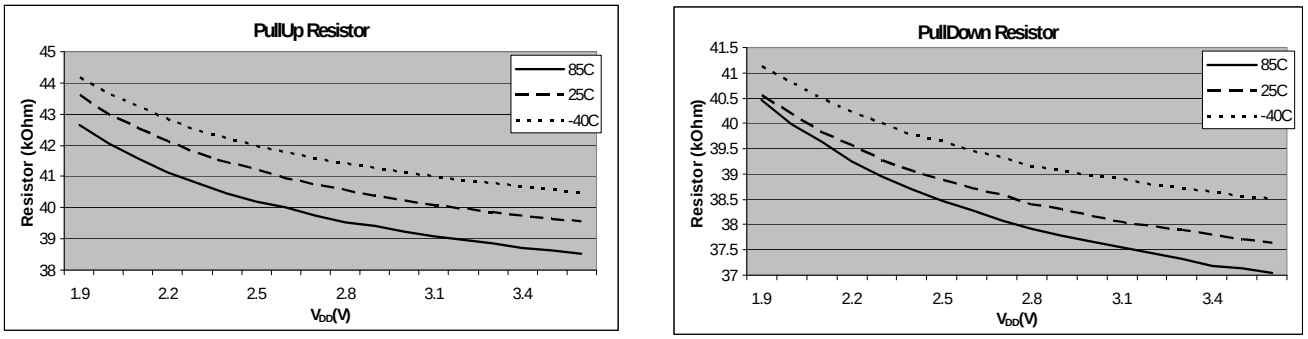
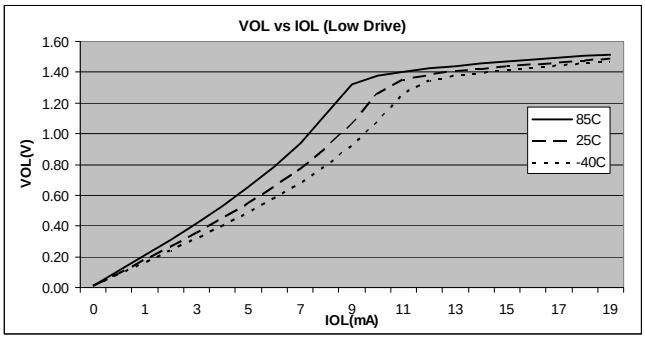


Figure 4. Pullup and Pulldown Typical Resistor Values



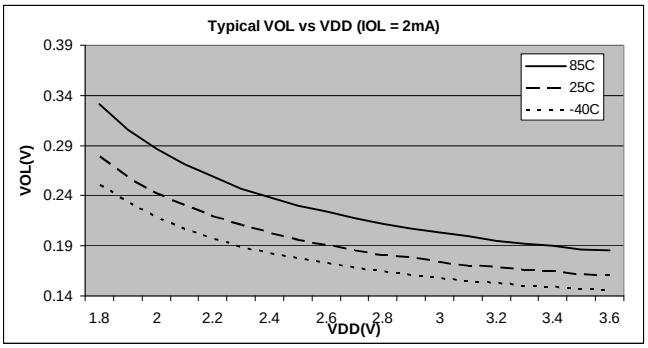
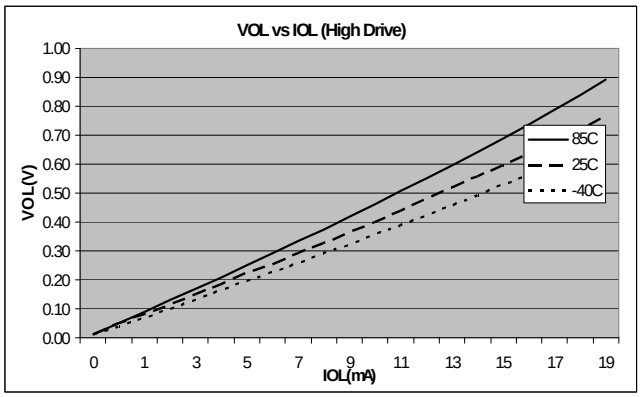


Figure 5. Typical Low-Side Driver (Sink) Characteristics — Low Drive (PTxDSn = 0)



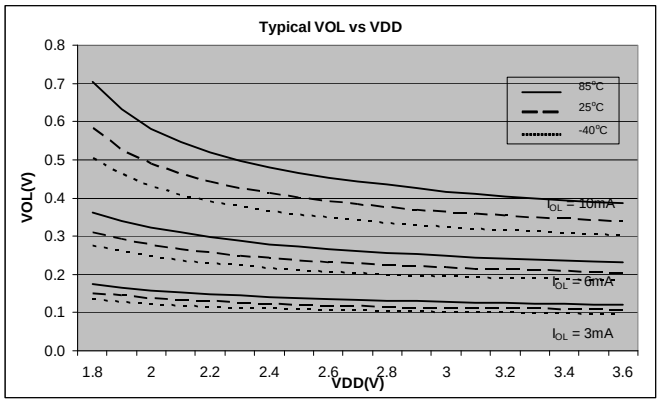
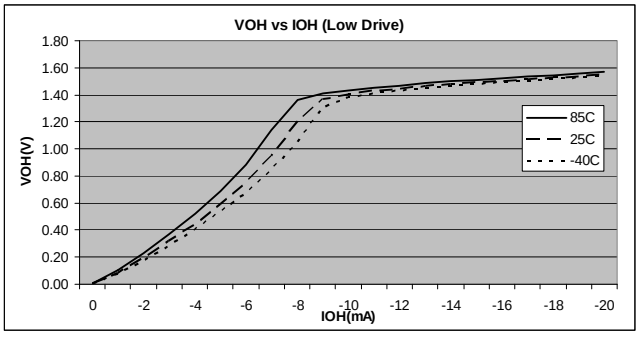


Figure 6. Typical Low-Side Driver (Sink) Characteristics — High Drive (PTxDSn = 1)



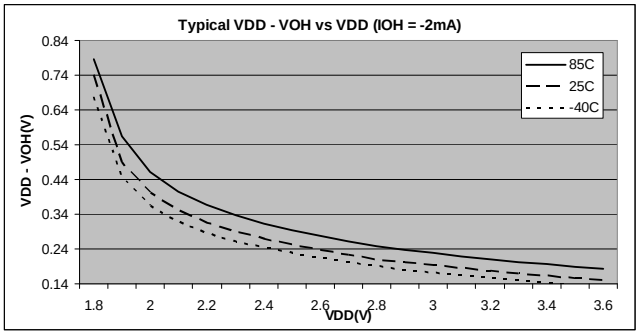


Figure 7. Typical High-Side (Source) Characteristics — Low Drive (PTxDSn = 0)

Table 11. Supply Current Characteristics

Num	C	Parameter		Symbol	V_{DD} (V)	Typical[1]	Max	Unit	Temp (°C)
1	P	Run supply current FEI mode, all modules on	25.165 MHz	RI_{DD}	3	66.2	100	mA	–40 to 85°C
	T		20 MHz			55.3	—		
	T		8 MHz			23.9	—		
	T		1 MHz			4.56	—		
2	C	Run supply current FEI mode, all modules off	25.165 MHz	RI_{DD}	3	55.1	56	mA	–40 to 85°C
	T		20 MHz			46.6	—		
	T		8 MHz			19.9	—		
	T		1 MHz			3.92	—		
3	T	Run supply current LPS=0, all modules off	16 kHz FBILP	RI_{DD}	3	239	—	µA	—
	T		16 kHz FBELP			249	—		
4	T	Run supply current LPS = 1, all modules off, running from flash	16 kHz FBELP	RI_{DD}	3	50	—	µA	—
5	C	Wait mode supply current FEI mode, all modules off	25.165 MHz	WI_{DD}	3	51.1	69	mA	–40 to 85°C
	T		20 MHz			42.6	—		
	T		8 MHz			18.8	—		
	T		1			3.69	—		
6	T	Wait mode supply current LPRS = 1, all mods off		WI_{DD}	3	1	—	µA	—
7	P	Stop2 mode supply current		$S2I_{DD}$	3	0.576	30	µA	–40 to 85°C
	C				2		16		
8	P	Stop3 mode supply current		$S3I_{DD}$	3	1.05	45	µA	–40 to 85°C
	C				2		27		
9	T	LVD adder to stop3, stop2 (LVDE = LVDSE = 1)		$S3I_{DDLVD}$	3	120	—	µA	—
10	T	Voltage reference adder to stop3	Low power mode	$S3I_{DDLVD}$	3	90	—	µA	—
			Tight regulation mode			270			
11	T	PRACMP adder to stop3	PRG disabled	$S3I_{DDLVD}$	3	13	—	µA	—
			PRG enabled			29			
12	T	LCD adder to stop3, stop2, VIREG enabled, 1/4 duty cycle, 4x39 configuration for 156 segments, 32Hz frame rate, no LCD glass connected		$S3I_{DDLVD}$	3	1.3	—	µA	—
13	C	Adder to stop3 for oscillator enabled[2] (ERCLKEN =1 and EREFSTEN = 1)		$S3I_{DDOSC}$	3	5		µA	—

Table 11. Supply Current Characteristics (continued)

Num	C	Parameter	Symbol	V_{DD} (V)	Typical[1]	Max	Unit	Temp (°C)
14	P	IRTC supply current[3,4,5]	I_{DD-BAT}		1.5	5	μA	–40 to 85°C

1 Typicals are measured at 25 °C.

2 Values given under the following conditions: low range operation (RANGE = 0), low power mode (HGO = 0).

3 This is the current consumed when the IRTC is being powered by the V_{BAT}.

4 The IRTC power source depends on the MCU configuration and V_{DD} voltage level. Refer to reference manual for further information.

5 The IRTC current consumption includes the IRTC XOSC1.

2.7 Analog Comparator (PRACMP) Electricals

Table 12. PRACMP Electrical Specifications

N	C	Characteristic	Symbol	Min	Typical	Max	Unit
1	—	Supply voltage	V_{PWR}	1.8	—	3.6	V
2	C	Supply current (active) (PRG enabled)	I_{DDACT1}	—	—	60	μA
3	C	Supply current (active) (PRG disabled)	I_{DDACT2}	—	—	40	μA
4	D	Supply current (ACMP and PRG all disabled)	I_{DDDIS}	—	—	2	nA
5	—	Analog input voltage	VAIN	V_{SS} – 0.3	—	V_{DD}	V
6	T	Analog input offset voltage	VAIO	—	5	40	mV
7	T	Analog comparator hysteresis	V_H	3.0	—	20.0	mV
8	D	Analog input leakage current	I_{ALKG}	—	—	1	nA
9	T	Analog comparator initialization delay	t_{AINIT}	—	—	1.0	μs
10	—	Programmable reference generator input1	$V_{In1}(V_{DD})$	—	V_{DD}	—	V
11	T	Programmable reference generator input2	$V_{In2}(V_{DD25})$	1.8	—	2.75	V
12	D	Programmable reference generator setup delay	t_{PRGST}	—	1	—	μs
13	D	Programmable reference generator step size	Vstep	–0.25	0	0.25	LSB
14	P	Programmable reference generator voltage range	V_{prgout}	$V_{In}/32$	—	V_{in}	V

2.8 ADC Characteristics

These specs all assume seperate V_{DDAD} supply for ADC and isolated pad segment for ADC supplies and differential inputs. Spec's should be de-rated for $V_{REFH} = V_{bg}$ condition.

Table 13. 16-bit ADC Operating Conditions

Num	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
1	Supply voltage	Absolute	V_{DDA}	1.8	—	3.6	V	
2		Delta to V_{DD} (V_{DD}–V_{DDA})[2]	ΔV_{DDA}	–100	0	100	mV	
3	Ground voltage	Delta to V_{SS} (V_{SS}–V_{SSA})[2]	ΔV_{SSA}	–100	0	100	mV	
4	Ref Voltage High		V_{REFH}	1.15	V_{DDA}	V_{DDA}	V	

1 All accuracy numbers assume the ADC is calibrated with $V_{REFH} = V_{DDAD}$

2 Typical values assume V_{DDAD} = 3.0V, Temp = 25°C, f_{ADCK} = 2.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

3 1 LSB = $(V_{REFH} - V_{REFL})/2^N$

Table 15. 16-bit ADC Characteristics($V_{REFH} = V_{DDAD} \geq 2.7V$, $V_{REFL} = V_{SSAD}$, $F_{ADCK} \leq 4MHz$, ADHSC=1)

Characteristic	Conditions[1]	C	Symb	Min	Typ[2]	Max	Unit	Comment
Total Unadjusted Error	16-bit differential mode 16-bit single-ended mode	T	TUE	— —	±16 ±20	+24/-24 +32/-20	LSB[3]	32x Hardware Averaging (AVGE = %1 AVGS = %11)
	13-bit differential mode 12-bit single-ended mode	T		— —	±1.5 ±1.75	±2.0 ±2.5		
	11-bit differential mode 10-bit single-ended mode	T		— —	±0.7 ±0.8	±1.0 ±1.25		
	9-bit differential mode 8-bit single-ended mode	T		— —	±0.5 ±0.5	±1.0 ±1.0		
Differential Non-Linearity	16-bit differential mode 16-bit single-ended mode	T	DNL	— —	±2.5 ±2.5	±3 ±3	LSB[2]	
	13-bit differential mode 12-bit single-ended mode	T		— —	±0.7 ±0.7	±1 ±1		
	11-bit differential mode 10-bit single-ended mode	T		— —	±0.5 ±0.5	±0.75 ±0.75		
	9-bit differential mode 8-bit single-ended mode	T		— —	±0.2 ±0.2	±0.5 ±0.5		
Integral Non-Linearity	16-bit differential mode 16-bit single-ended mode	T	INL	— —	±6.0 ±10.0	±12.0 ±16.0	LSB[2]	
	13-bit differential mode 12-bit single-ended mode	T		— —	±1.0 ±1.0	±2.0 ±2.0		
	11-bit differential mode 10-bit single-ended mode	T		— —	±0.5 ±0.5	±1.0 ±1.0		
	9-bit differential mode 8-bit single-ended mode	T		— —	±0.3 ±0.3	±0.5 ±0.5		
Zero-Scale Error	16-bit differential mode 16-bit single-ended mode	T	E_{ZS}	— —	±4.0 ±4.0	+16/0 +16/-8	LSB[2]	$V_{ADIN} = V_{SSAD}$
	13-bit differential mode 12-bit single-ended mode	T		— —	±0.7 ±0.7	±2.0 ±2.0		
	11-bit differential mode 10-bit single-ended mode	T		— —	±0.4 ±0.4	±1.0 ±1.0		
	9-bit differential mode 8-bit single-ended mode	T		— —	±0.2 ±0.2	±0.5 ±0.5		

2.13 VREF Characteristics

Table 21. VREF Electrical Specifications

Num	C	Characteristic	Symbol	Min	Typical	Max	Unit
1	—	Supply voltage	V_{DDAD}	1.80	—	3.60	V
2	—	Operating temperature range	T_{op}	–40	—	105	°C
3	D	Load capability	I_{load}	—	—	10	mA
4	C P	Voltage reference output untrimmed factory trimmed	V_{REFO}	 1.070 1.04	 — 1.150	 1.202 1.17	 V V
5	D	Load regulation mode = 10, I_{load} = 1 mA		20	—	100	μV/mA
6	T	Line regulation (power supply rejection) DC AC		±0.1 from room temp voltage –60			 mV dB
7	T	Bandgap only (mode = 00)	I_{BG}	—	72	—	μA
8	C	Low power mode (mode = 01)	I_{LP}	—	90	125	μA
9	T	Tight regulation mode (mode =10)	I_{TR}	—	0.27	—	mA

2.14 SPI Characteristics

Table 22 and Figure 19 through Figure 22 describe the timing requirements for the SPI system.

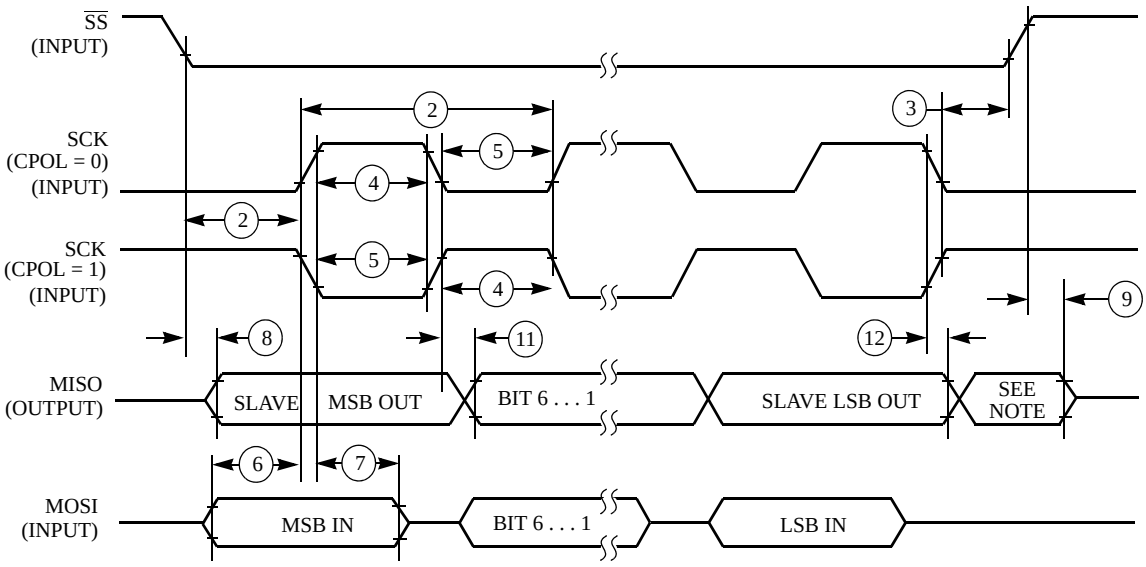
Table 22. SPI Electrical Characteristic[1,2]

Num[3]	C	Characteristic[4]	Symbol	Min	Max	Unit
1	D	Operating frequency Master Slave	f_{op}	$f_{Bus}/2048$ 0	$f_{Bus}/2$ $f_{Bus}/4$	Hz
2	D	SPSCK period Master Slave	t_{SPSCK}	2 4	2048 —	t_{cyc}
3	D	Enable lead time Master Slave	t_{Lead}	1/2 —	— —	t_{SPSCK} t_{cyc}
4	D	Enable lag time Master Slave	t_{Lag}	1/2 —	— —	t_{SPSCK} t_{cyc}
5	D	Clock (SPSCK) high or low time Master Slave	t_{WSPSCK}	$t_{cyc} - 30$	1024 t_{cyc} —	ns
6	D	Data setup time (inputs) Master Slave	t_{SI}	15 15	— —	ns
7	D	Data hold time (inputs) Master Slave	t_{HI}	0 25	— —	ns
8	D	Slave access time[5]	t_a	—	1	t_{cyc}
9	D	Slave MISO disable time[6]	t_{dis}	—	1	t_{cyc}
10	D	Data valid (after SPSCK edge) Master Slave	t_v	— —	25 25	ns
11	D	Data hold time (outputs) Master Slave	t_{HO}	0 0	— —	ns
12	D	Rise time Input Output	t_{RI} t_{RO}	— —	$t_{cyc} - 25$ —25	ns
13	D	Fall time Input Output	t_{FI} t_{FO}	— —	$t_{cyc} - 25$ —25	ns

1 The performance of SPI2 depends on the configuration of power supply of the LCD pins. When the LCD pins are configured with full complementary drive enabled (FCDEN = 1, VSUPPLY = 11 and RVEN = 0), and VLL3 is driven with external VDD, the SPI2 can operate at the max performance as the above table. When the internal LCD charge pump is used to power the LCD pins, the SPI2 is configured with open-drain outputs. Its performance depends on the value of the external pullup resistor implemented, and the max operating frequency must be limited to 1 MHz.

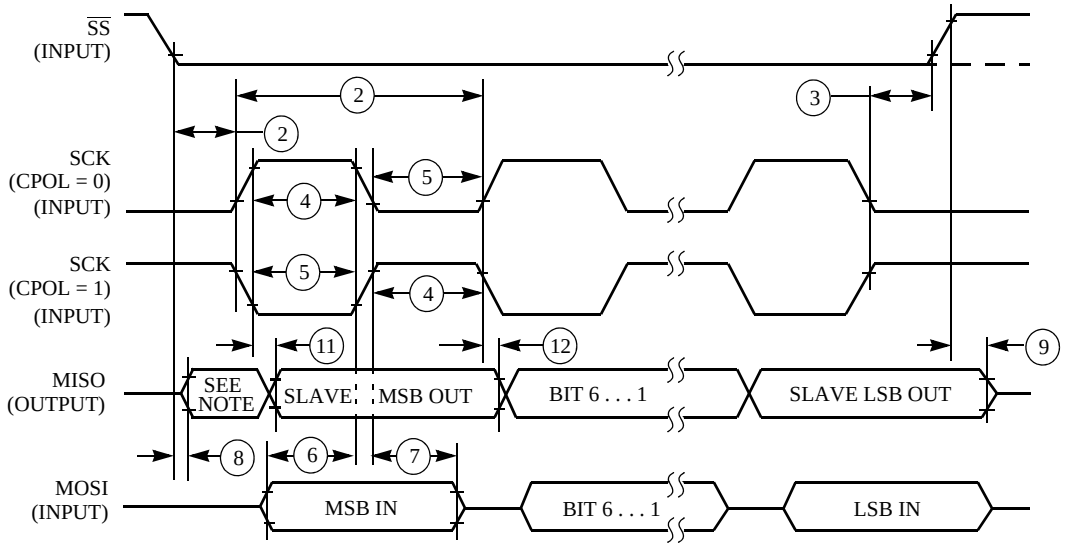
2 SPI3 has open-drain outputs and its performance depends on the value of the external pullup resistor implemented.

3 Refer to Figure 19 through Figure 22.



NOTE:
1. Not defined but normally MSB of character just received

Figure 21. SPI Slave Timing (CPHA = 0)



NOTE:
1. Not defined but normally LSB of character just received

Figure 22. SPI Slave Timing (CPHA = 1)

2.15 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory section of the *MCF51EM256 Series ColdFire Microcontroller Reference Manual*.

Table 23. Flash Characteristics

N	C	Characteristic	Symbol	Min	Typical	Max	Unit
1	D	Supply voltage for program/erase –40 °C to 85 °C	$V_{prog/erase}$	1.8		3.6	V
2	D	Supply voltage for read operation	V_{Read}	1.8		3.6	V
3	D	Internal FCLK frequency[1]	f_{FCLK}	150		200	kHz
4	D	Internal FCLK period ($1/f_{FCLK}$)	t_{Fcyc}	5		6.67	µs
5	P	Longword program time (random location)[2]	t_{prog}	9			t_{Fcyc}
6	P	Longword program time (burst mode)[2]	t_{Burst}	4			t_{Fcyc}
7	P	Page erase time[2]	t_{Page}	4000			t_{Fcyc}
8	P	Mass erase time[2]	t_{Mass}	20,000			t_{Fcyc}
9		Longword program current[3]	R_{IDDBP}	—	9.7	—	mA
10		Page erase current[3]	R_{IDDPE}	—	7.6	—	mA
11	C	Program/erase endurance[4] T_L to T_H = –40 °C to 85 °C T = 25 °C		10,000 —	— 100,000	— —	cycles
12	C	Data retention[5]	t_{D_ret}	15	100	—	years

1 The frequency of this clock is controlled by a software setting.

2 These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

3 The program and erase currents are additional to the standard run I_{DD}. These values are measured at room temperatures with V_{DD} = 3.0 V, bus frequency = 4.0 MHz.

4 **Typical endurance for flash** was evaluated for this product family on the HC9S12Dx64. For additional information on how Freescale defines typical endurance, please refer to Engineering Bulletin EB619, *Typical Endurance for Nonvolatile Memory.*

5 **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale defines typical data retention, please refer to Engineering Bulletin EB618, *Typical Data Retention for Nonvolatile Memory.*

2.16 EMC Performance

Electromagnetic compatibility (EMC) performance is highly dependant on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

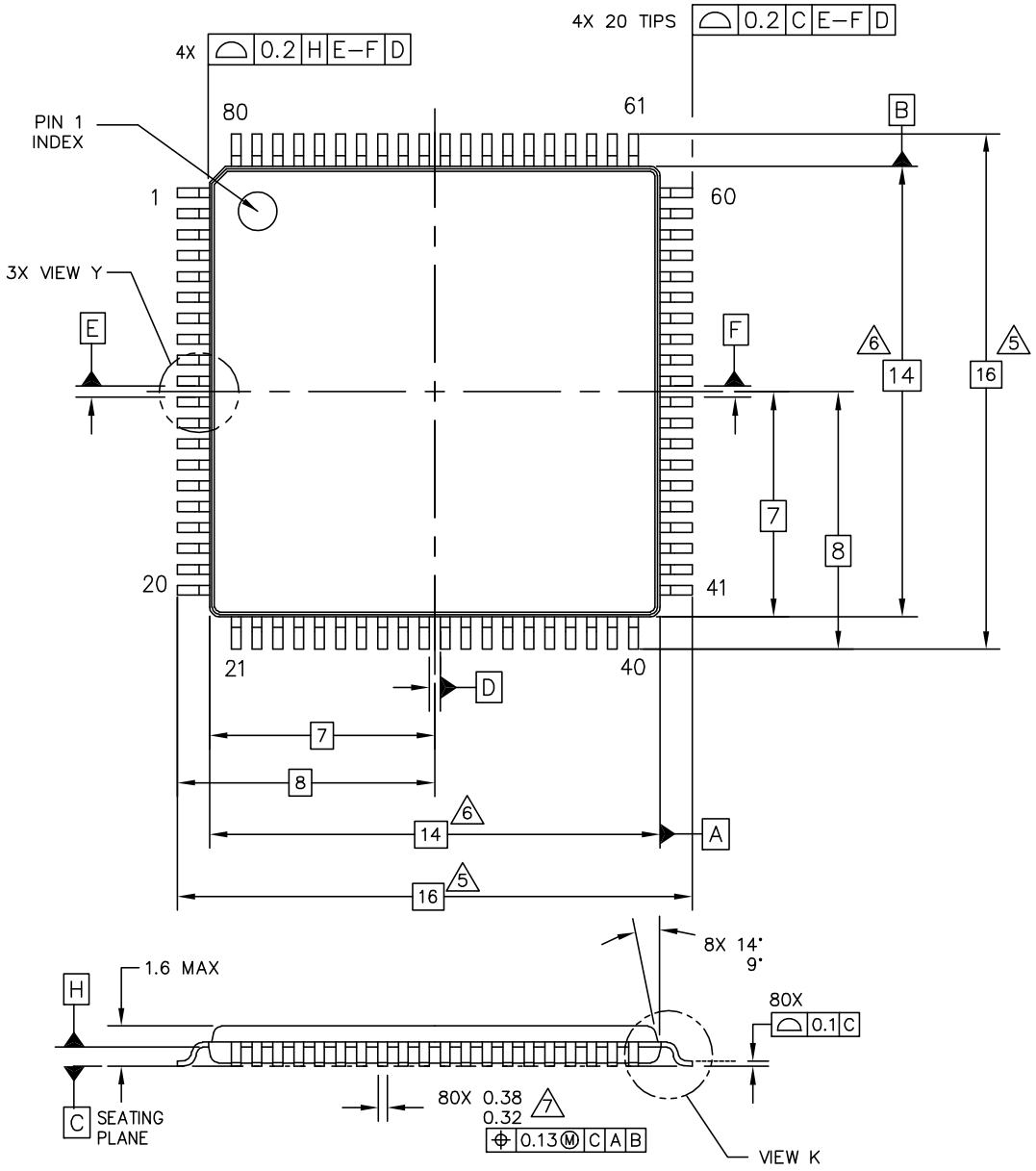
2.16.1 Radiated Emissions

Microcontroller radiated RF emissions are measured from 150 kHz to 1 GHz using the TEM/GTEM Cell method in accordance with the IEC 61967-2 and SAE J1752/3 standards. The measurement is performed with the microcontroller installed on a custom EMC evaluation board while running specialized EMC test software. The radiated emissions from the microcontroller are measured in a TEM cell in two package orientations (North and East). For more detailed information concerning the evaluation results, conditions and setup, please refer to the EMC Evaluation Report for this device.

3 Mechanical Outline Drawings

3.1 80-pin LQFP Package

freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASS23237W
		PAGE: 917A
	DO NOT SCALE THIS DRAWING	REV: E



TITLE: 80 LD LQFP, 14 X 14 PKG, 0.65 MM PITCH, 1.4 THICK	CASE NUMBER: 917A–03	
	STANDARD: FREESCALE	
	PACKAGE CODE: 8258	SHEET: 1 OF 4

freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASS23237W
		PAGE: 917A
	DO NOT SCALE THIS DRAWING	REV: E

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION : MILIMETER.
3. DATUM PLANE H IS LOCATED AT THE BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUM E, F AND D TO BE DETERMINED AT DATUM PLANE H.
5. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
7. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07.

TITLE:	CASE NUMBER: 917A–03	
80 LD LQFP, 14 X 14 PKG, 0.65 MM PITCH, 1.4 THICK	STANDARD: FREESCALE	
	PACKAGE CODE: 8258	SHEET: 3 OF 4

freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASS23308W
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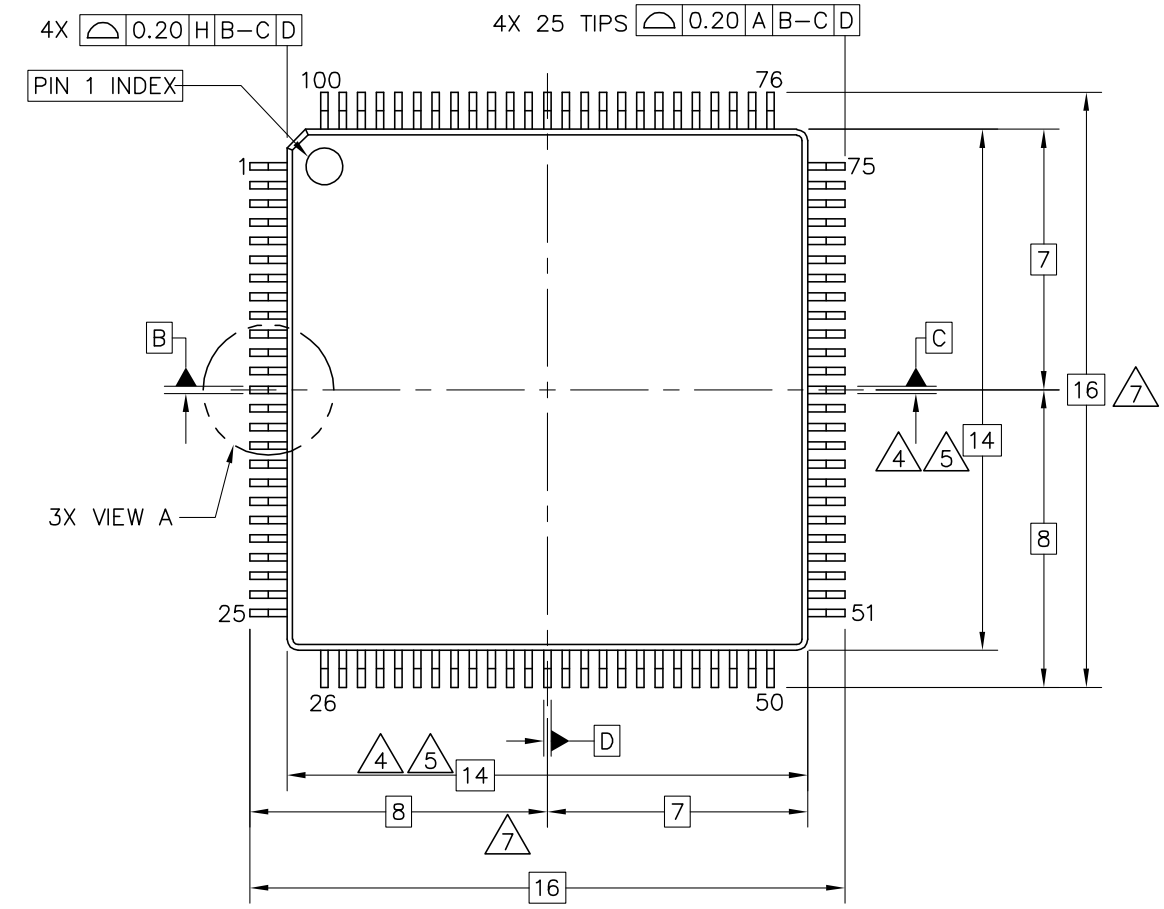

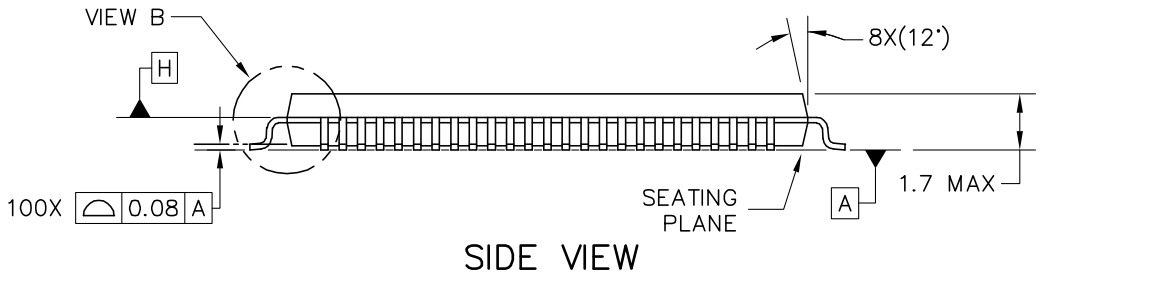

TITLE: 100 LEAD LQFP 14 X 14, 0.5 PITCH, 1.4 THICK	CASE NUMBER: 983–02	
	STANDARD: NON–JEDEC	
	PACKAGE CODE: 8264	SHEET: 1 OF 4

freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASS23308W
		PAGE: 983
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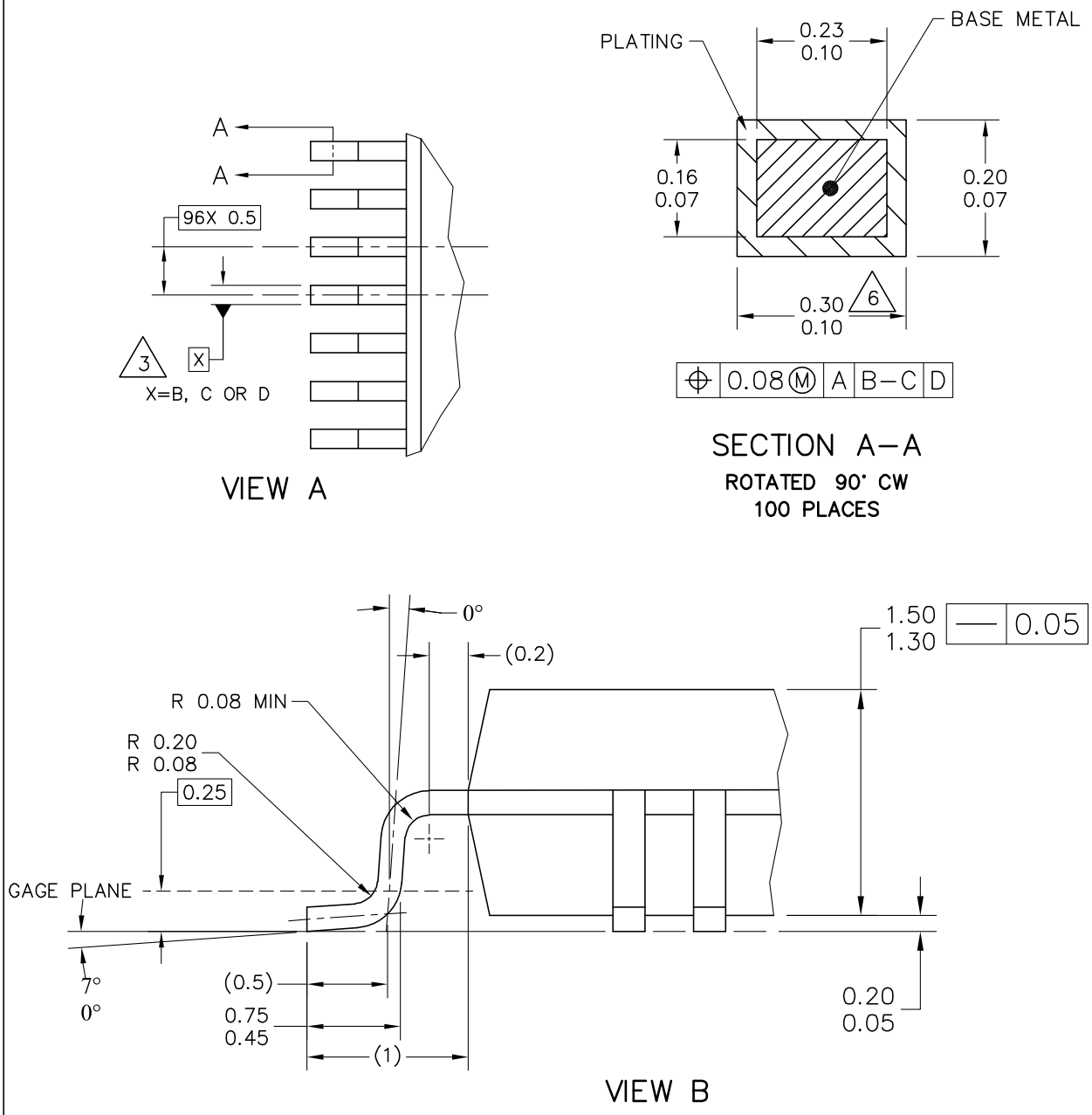

TITLE: 100 LEAD LQFP 14 X 14, 0.5 PITCH, 1.4 THICK	CASE NUMBER: 983–02	
	STANDARD: NON–JEDEC	
	PACKAGE CODE: 8264	SHEET: 2 OF 4