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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V1
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, SCI, SPI
Peripherals	LCD, LVD, PWM, WDT
Number of I/O	63
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf51em128cll

Table of Contents

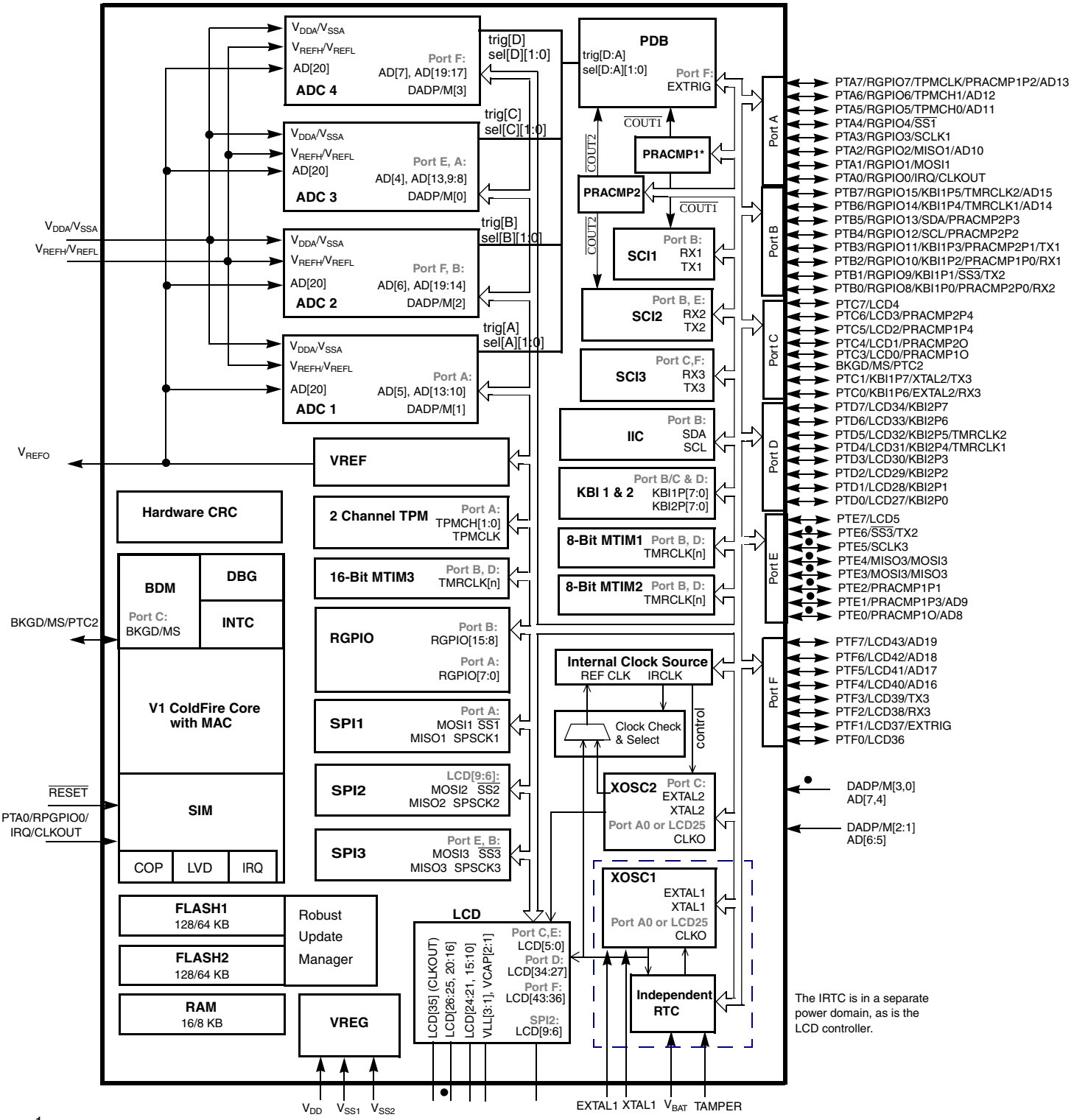
1 MCF51EM256 Series Configurations

1.1 Device Comparison

The MCF51EM256 series is summarized in Table 1.

Table 1. MCF51EM256 Series Features by MCU and Package

Feature	MCF51EM256		MCF51EM128	
Flash size (bytes)	262144		131072	
RAM size (bytes)	16384		8192	
Robust flash update supported	Yes			
Pin quantity	100	80	100	80
PRACMP1 inputs	5	3	5	3
PRACMP2 inputs	5			
ADC modules	4		4	
ADC differential channels[1]	4	2	4	2
ADC single-ended channels	16	12	16	12
DBG	Yes			
ICS	Yes			
IIC	Yes			
IRQ	Yes			
IRTC	Yes			
VREF	Yes			
LCD drivers	44	37	44	37
Rapid GPIO[2]	16	16	16	16
Port I/O[3]	47	40	47	40
Keyboard interface 1	8			
Keyboard interface 2	8			
SCI1	Yes			
SCI2	Yes			
SCI3	Yes			
SPI1 (FIFO)	Yes			
SPI2 (standard)	Yes			
SPI3 (standard)	Yes	No	Yes	No



1 Pins with • are not present on 80-pin devices.

2 PRACMP1 has two less available inputs on the 80-pin devices.

Figure 1. MCF51EM256 Series Block Diagram

1.3 Features

Table 2 describes the functional units of the MCF51EM256 series.

Table 2. MCF51EM256 Series Functional Units

Unit	Function
ADC (analog-to-digital converter)	Measures analog voltages at up to 16 bits of resolution. Each ADC has up to four differential and 24 single-ended inputs.
BDM (background debug module)	Provides single pin debugging interface (part of the V1 ColdFire core)
CF1 CORE (V1 ColdFire core) with MAC unit	Executes programs, handles interrupts and containes multiply-accumulate hardware (MAC).
PRACMP1, PRACMP2 (comparators)	Analog comparators for comparing external analog signals against each other, or a variety of reference levels.
COP (computer operating poperly)	Software watchdog
IRQ (interrupt request)	Single pin high priority interrupt (part of the V1 ColdFire core)
CRC (cyclic Redundancy Check)	High-speed CRC calculation
DBG (debug)	Provides debugging and emulation capabilities (part of the V1 ColdFire core)
FLASH (flash memory)	Provides storage for program code, constants and variables
IIC (inter-integrated circuits)	Supports standard IIC communications protocol and SMBus
INTC (interrupt controller)	Controls and prioritizes all device interrupts
KBI1 & KBI2	Keyboard Interfaces 1 and 2
LCD	Liquid crystal display driver
LVD (low voltage detect)	Provides an interrupt to the CF1CORE in the event that the supply voltage drops below a critical value. The LVD can also be programmed to reset the device upon a low voltage event
ICS (internal clock source)	Provides clocking options for the device, including a three frequency-locked loops (FLLs) for multiplying slower reference clock sources
IRTC (independent real-time clock)	The independent real time clock provides an independent time-base with optional interrupt, battery backup and tamper protection
VREF (voltage reference)	The voltage reference output is available for both on and off-chip use
MTIM1, MTIM2 (modulo timers)	8-bit modulo timers with configurable clock inputs and interrupt generation on overflow
MTIM3 (modulo timer)	16-bit modulo timer with configurable clock inputs and interrupt generation on overflow
PDB (programmable delay block)	This timer is optimized for scheduling ADC conversions
RAM (random-access memory)	Provides stack and variable storage
RGPIO (rapid general-purpose input/output)	Allows for I/O port access at CPU clock speeds and is used to implement GPIO functionality for PTA and PTB.

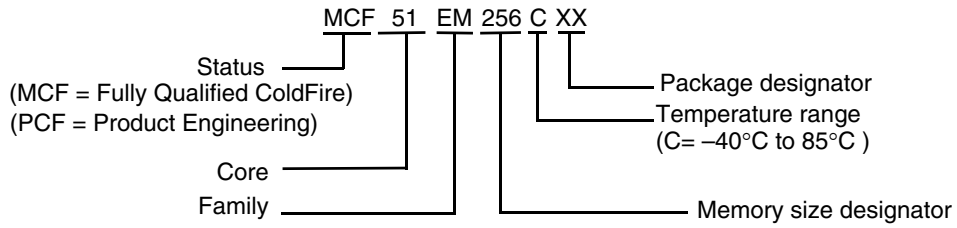
  - 6 µs typical wakeup time from stop3 mode
- Clock source options
  - Two independent oscillators (XOSC1 and XOSC2) — loop-control Pierce oscillator; 32.768 kHz crystal or ceramic resonator. XOSC1 nominally supports the independent real time clock, and can be powered by a separate battery backup. XOSC2 is the primary external clock source for the ICS
  - Internal clock source (ICS) — internal clock source module containing a frequency-locked-loop (FLL) controlled by internal or external reference (XOSC1 or XOSC2); precision trimming of internal reference allowing 0.2% resolution and typical 0.5% to –1% deviation over temperature and voltage; supporting CPU frequencies from 4 kHz to 50 MHz
- System protection
  - Watchdog computer operating properly (COP) reset with option to run from dedicated 1 kHz internal clock source or bus clock
  - Low voltage detection with reset or interrupt; selectable trip points; seperate low voltage warning with optional interrupt; selectable trip points
  - Illegal opcode and illegal address detection with reset
  - Flash block protection for each array to prevent accidental write/erasure
  - Hardware CRC module to support fast cyclic redundancy checks
- Development support
  - Integrated ColdFire DEBUG_Rev_B+ interface with single wire BDM connection supports same electrical interface used by the S08 family debug modules
  - Real-time debug support with six hardware breakpoints (4 PC, 1 address and 1 data)
  - On-chip trace buffer provides programmable start/stop recording conditions
- Peripherals
  - **ADC16** — 4 analog-to-digital converters; the 100 pin version of the device has 1 dedicated differential channel and 1 dedicated single-ended channel per ADC, along with 3 muxed single-ended channels per ADC. The ADCs have 16-bit resolution, range compare function, 1.7 mV/°C temperature sensor, internal bandgap reference channel, operate in stop3 and are fully functional from 3.6 V to 1.8 V
  - **PDB** — Programmable delay block with 16-bit counter and modulus and 3-bit prescaler; 8 trigger outputs for ADC16 modules (2 per ADC); provides periodic coordination of ADC sampling sequence with programmable sequence completion interrupt
  - **IRTC** — Ultra-low power independent real time clock with calendar features (IRTC); runs in all MCU modes; external clock source with trim capabilities (XOSC1); independent voltage source runs IRTC when MCU is powered-down; tamper detection and indicator; battery monitor output to ADC; unaffected by MCU resets
  - **PRACMPx** — Two analog comparators with selectable interrupt on rising, falling, or either edge of comparator output; compare option to programmable internal reference voltage; operation in stop3
  - **LCD** — up to 288 segments (8 × 36); 160 segments (4 × 40); internal charge pump and option to provide internal reference voltage that can be trimmed for contrast control; flexible

front-plane/backplane pin assignments; operation in all low power modes with blink functionality

- **SCIx** — Three serial communications interface modules with optional 13-bit break; option to connect Rx input to PRACMP output on SCI1 and SCI2; high current drive on Tx on SCI1 and SCI2; wakeup from stop3 on Rx edge. SCI1 and SCI2 Tx pins can be modulated with timer outputs for use with IR interfaces
- **SPIx—** Two serial peripheral interfaces (SPI2, SPI3) with full-duplex or single-wire bidirectional; double-buffered transmit and receive; master or slave mode; MSB-first or LSB-first shifting
- **SPI16**— Serial peripheral interface (SPI1) with 32-bit FIFO buffer; 16-bit or 8-bit data transfers; full-duplex or single-wire bidirectional; double-buffered transmit and receive; master or slave mode; MSB-first or LSB-first shifting
- **IIC** — Up to 100 kbps with maximum bus loading; multi-master operation; programmable slave address; interrupt driven byte-by-byte data transfer; supports broadcast mode and 10 bit addressing
- **MTIMx** — Two 8-bit and one 16-bit modulo timers with 4-bit prescaler; overflow interrupt; external clock input/pulse accumulator
- **TPM** — 2-channel Timer/PWM module; selectable input capture, output compare, or buffered edge- or center-aligned PWM on each channel; external clock input/pulse accumulator; can be used modulate SCI1 and SCI2 TX pins

- Input/output
  - up to 16 rapid GPIO and 48 standard GPIOs, including 1 output-only pin and 3 open-drain pins.
  - up to 16 keyboard interrupts with selectable polarity
  - Hysteresis and configurable pullup device on all input pins; configurable slew rate and drive strength on all output pins
- Package options
  - 100-pin LQFP, 80-pin LQFP

1.4 Part Numbers



1.5 Pinouts and Packaging

1.5.1 Pinout: 80-Pin LQFP

Pins not available on the 80-pin LQFP are automatically disabled for reduced current consumption. No user interaction is needed. Software access to the functions on these pins will be ignored

Figure 2 shows the pinout of the 80-pin LQFP.

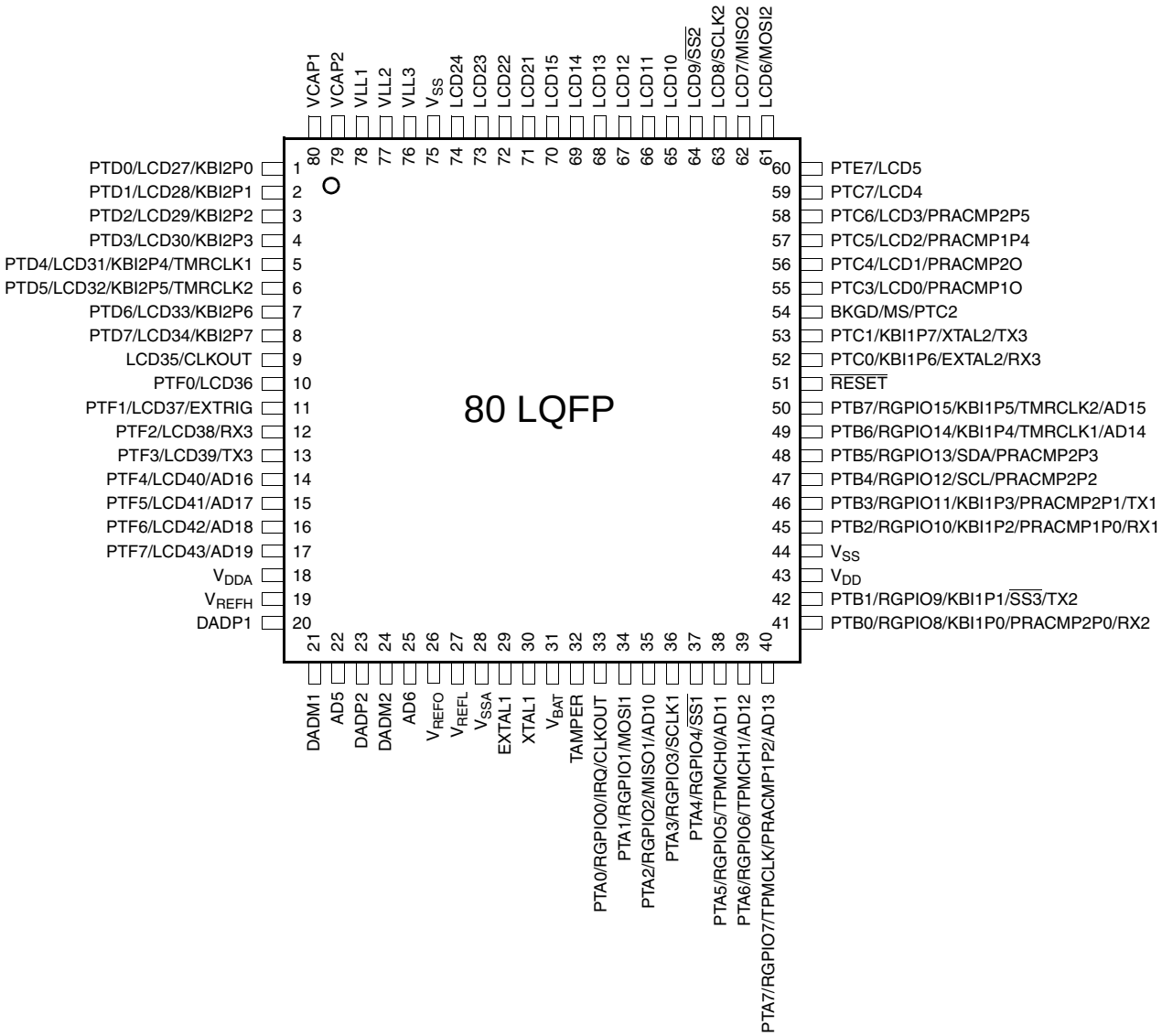


Figure 2. 80-Pin LQFP Pinout

Table 4. MCF51EM256 Series Package Pin Assignments (continued)

100 LQFP	80 LQFP	Default Function	ALT1	ALT2	ALT3	Comment
33	—	AD7				
34	26	V_{REFO}				
35	27	V_{REFL}				
36	28	V_{SSA}				
37	29	EXTAL1				
38	30	XTAL1				
39	31	V_{BAT}				
40	32	TAMPER				
41	33	PTA0/RGPIO0	IRQ	CLKOUT		
42	—	PTE0		PRACMP1O	AD8	
43	—	PTE1		PRACMP1P3	AD9	
44	34	PTA1/RGPIO1	MOSI1			RGPIO_ENB is used to select between standard GPIO and RGPIO
45	35	PTA2/RGPIO2	MISO1		AD10	
46	36	PTA3/RGPIO3	SCLK1			
47	37	PTA4/RGPIO4	$\overline{SS1}$			
48	38	PTA5/RGPIO5	TPMCH0		AD11	
49	39	PTA6/RGPIO6	TPMCH1		AD12	
50	40	PTA7/RGPIO7	TPMCLK	PRACMP1P2	AD13	
51	—	PTE2		PRACMP1P1		
52	41	PTB0/RGPIO8	KBI1P0	PRACMP2P0	RX2	RGPIO_ENB is used to select between standard GPIO and RGPIO
53	42	PTB1/RGPIO9	KBI1P1	$\overline{SS3}$	TX2	2X Drive Output RGPIO_ENB is used to select between standard GPIO and RGPIO
54	43	V_{DD}				
55	44	V_{SS}				
56	45	PTB2/RGPIO10	KBI1P2	PRACMP1P0	RX1	RGPIO_ENB is used to select between standard GPIO and RGPIO
57	46	PTB3/RGPIO11	KBI1P3	PRACMP2P1	TX1	2X drive output RGPIO_ENB is used to select between standard GPIO and RGPIO

Table 4. MCF51EM256 Series Package Pin Assignments (continued)

100 LQFP	80 LQFP	Default Function	ALT1	ALT2	ALT3	Comment
58	47	PTB4/RGPIO12	SCL	PRACMP2P2		RGPIO_ENB is used to select between standard GPIO and RGPIO
59	48	PTB5/RGPIO13	SDA	PRACMP2P3		
60	—	PTE3	MOSI3	MISO3		
61	—	PTE4	MISO3	MOSI3		Open Drain
62	—	PTE5	SCLK3			Open Drain
63	—	PTE6	$\overline{SS3}$	TX2		Open Drain
64	49	PTB6/RGPIO14	KBI1P4	TMRCLK1	AD14	RGPIO_ENB is used to select between standard GPIO and RGPIO
65	50	PTB7/RGPIO15	KBI1P5	TMRCLK2	AD15	
66	51	$\overline{RESET}$				This pin is an open drain device and has an internal pullup. There is no clamp diode to V_{DD}.
67	52	PTC0	KBI1P6	EXTAL2	RX3	
68	53	PTC1	KBI1P7	XTAL2	TX3	
69	54	BKGD/MS	PTC2			This pin has an internal pullup. PTC2 can only be programmed as an output.
70[1]	55[1]	PTC3	LCD0	PRACMP1O		
71[1]	56[1]	PTC4	LCD1	PRACMP2O		
72[1]	57[1]	PTC5	LCD2		PRACMP1P4	
73[1]	58[1]	PTC6	LCD3		PRACMP2P4	
74[1]	59[1]	PTC7	LCD4			
75[1]	60[1]	PTE7	LCD5			
76[1]	61[1]	LCD6	MOSI2			
77[1]	62[1]	LCD7	MISO2			
78[1]	63[1]	LCD8	SCLK2			
79[1]	64[1]	LCD9	$\overline{SS2}$			
80	65	LCD10				
81	66	LCD11				
82	67	LCD12				
83	68	LCD13				
84	69	LCD14				
85	70	LCD15				
86	—	LCD16				

$$T_J = T_A + (P_D \times \theta_{JA}) \quad \textit{Eqn. 1}$$

where:

T_A = Ambient temperature, °C
θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W
$P_D = P_{int} + P_{I/O}$
$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power
$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad \textit{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (P_D)^2 \quad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

2.4 Electrostatic Discharge (ESD) Protection Characteristics

Although damage from static discharge is much less common on these devices than on early CMOS circuits, normal handling precautions should be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with CDF-AEC-Q00 Stress Test Qualification for Automotive Grade Integrated Circuits. (http://www.aecouncil.com/) This device was qualified to AEC-Q100 Rev E.

A device is considered to have failed if, after exposure to ESD pulses, the device no longer meets the device specification requirements. Complete dc parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 8. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series Resistance	R1	1500	Ω
	Storage Capacitance	C	100	pF
	Number of Pulse per pin	—	3	
Machine	Series Resistance	R1	0	Ω
	Storage Capacitance	C	200	pF
	Number of Pulse per pin	—	3	
Latch-up	Minimum input voltage limit		–2.5	V
	Maximum input voltage limit		7.5	V

Table 9. ESD and Latch-Up Protection Characteristics

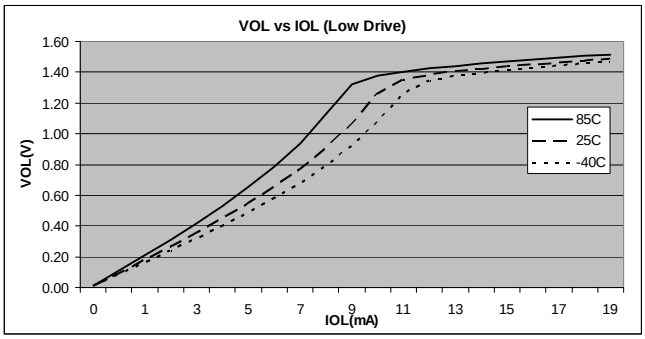
Num	Rating	Symbol	Min	Max	Unit
1	Human Body Model (HBM)	V_{HBM}	±2000	—	V
2	Machine Model (MM)	V_{MM}	±200	—	V
3	Charge Device Model (CDM)	V_{CDM}	±500	—	V
4	Latch-up Current at T_A = 85 °C	I_{LAT}	±100	—	mA

2.5 DC Characteristics

This section includes information about power supply requirements, I/O pin characteristics, and power supply current in various operating modes.

Table 10. DC Characteristics

Num	C	Parameter		Symbol	Min	Typical[1]	Max	Unit
1	P	Operating voltage	Digital supply — 50 MHz operation	V_{DD}	2.5	—	3.6	V
			Digital supply[2] — 20 MHz maximum operation	V_{DD}	1.8	—	3.6	
2	P	Analog supply		V_{DDA}	1.8	—	3.6	V
3	D	Battery supply		V_{BAT}	2.2	3	3.3	V
4	P	Bandgap voltage reference[3]		V_{BG}	1.15	1.17	1.18	V
5	C	Output high voltage	PTA[7:0], PTB[7:0], PTC[2:0], PTE[6:0], low-drive strength. $V_{DD} \geq 1.8$ V, $I_{Load} = -0.6$ mA	V_{OH}	$V_{DD} - 0.5$	—	—	V
	P		PTA[7:0], PTB[7:0], PTC[2:0], PTE[6:0], high-drive strength. $V_{DD} \geq 2.7$ V, $I_{Load} = -10$ mA					
	C		PTA[7:0], PTB[7:0], PTC[2:0], PTE[6:0], high-drive strength. $V_{DD} \geq 1.8$ V, $I_{Load} = -3$ mA					
6	C	Output high voltage	PTC[7:3], PTD[7:0], PTE7, PTF[7:0], LCD35/CLKOUT, MOSI2, MISO2, SCK2, SS2, low drive strength. VDD ≥ 1.8 V, $I_{Load} = -0.5$ mA	V_{OH}	$V_{DD} - 0.5$	—	—	V
	P		PTC[7:3], PTD[7:0], PTE7, PTF[7:0], LCD35/CLKOUT, MOSI2, MISO2, SCK2, SS2, high-drive strength. $V_{DD} \geq 2.7$ V, $I_{Load} = -3$ mA					
	C		PTC[7:3], PTD[7:0], PTE7, PTF[7:0], LCD35/CLKOUT, MOSI2, MISO2, SCK2, SS2, high-drive strength. $V_{DD} \geq 1.8$ V, $I_{Load} = -1$ mA					
7	D	Output high current	Max total I_{OH} for all ports	I_{OHT}	—	—	100	mA



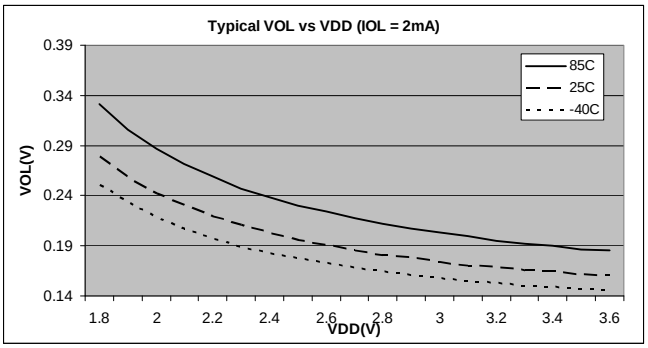
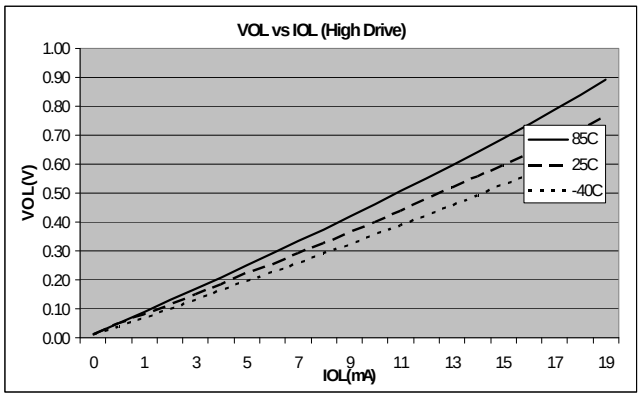


Figure 5. Typical Low-Side Driver (Sink) Characteristics — Low Drive (PTxDSn = 0)



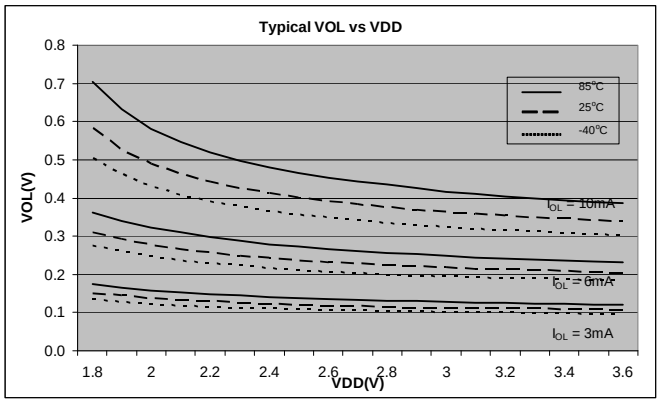
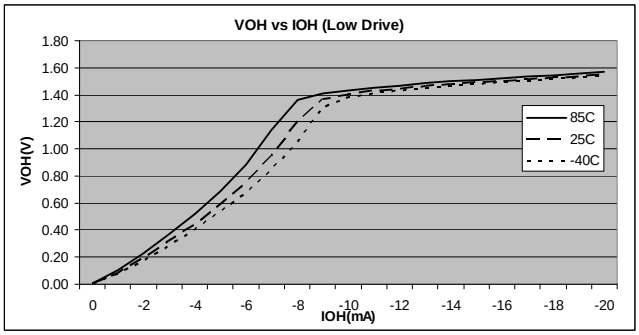


Figure 6. Typical Low-Side Driver (Sink) Characteristics — High Drive (PTxDSn = 1)



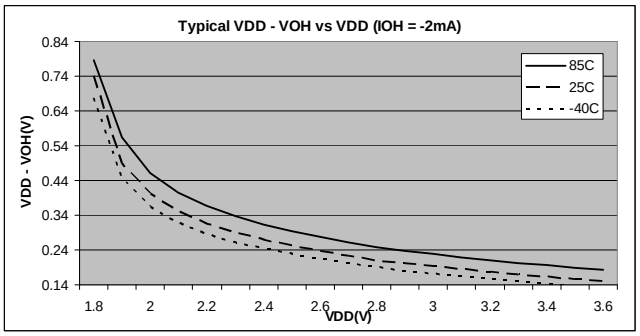


Figure 7. Typical High-Side (Source) Characteristics — Low Drive (PTxDSn = 0)

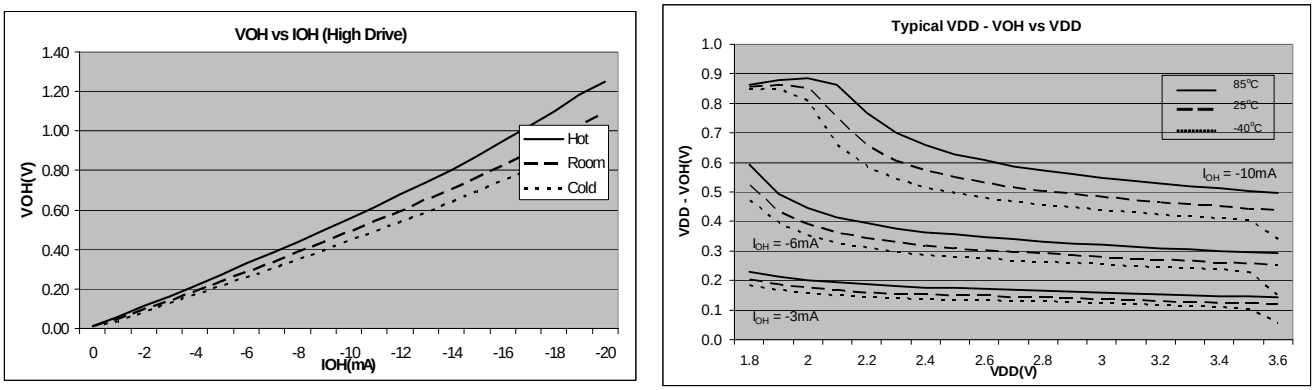


Figure 8. Typical High-Side (Source) Characteristics — High Drive (PTxDSn = 1)

2.6 Supply Current Characteristics

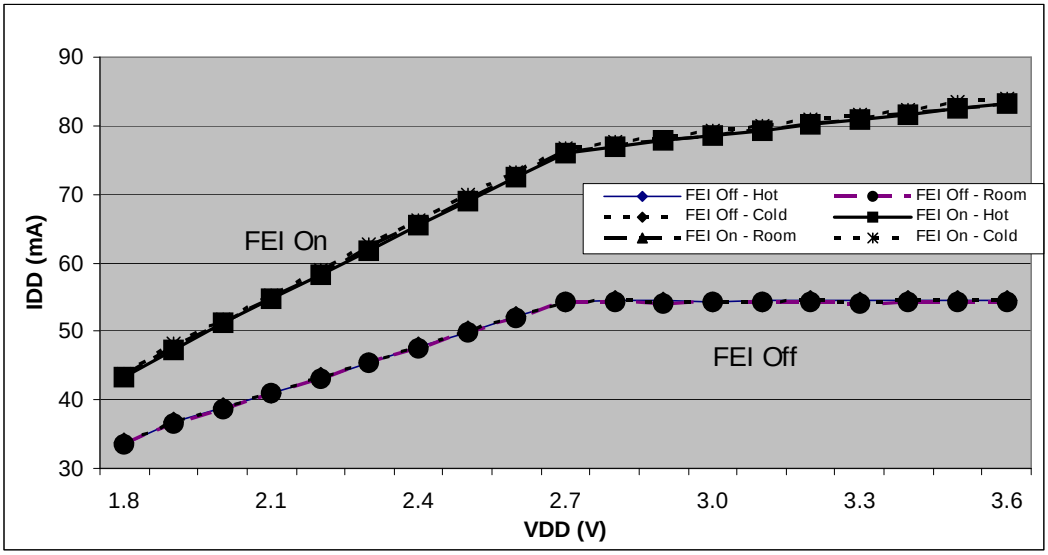


Figure 9. Typical Run I_{DD} for FBE and FEI, I_{DD} vs. V_{DD} (All Modules Enabled)

Table 11. Supply Current Characteristics

Num	C	Parameter		Symbol	V_{DD} (V)	Typical[1]	Max	Unit	Temp (°C)
1	P	Run supply current FEI mode, all modules on	25.165 MHz	RI_{DD}	3	66.2	100	mA	–40 to 85°C
	T		20 MHz			55.3	—		
	T		8 MHz			23.9	—		
	T		1 MHz			4.56	—		
2	C	Run supply current FEI mode, all modules off	25.165 MHz	RI_{DD}	3	55.1	56	mA	–40 to 85°C
	T		20 MHz			46.6	—		
	T		8 MHz			19.9	—		
	T		1 MHz			3.92	—		
3	T	Run supply current LPS=0, all modules off	16 kHz FBILP	RI_{DD}	3	239	—	µA	—
	T		16 kHz FBELP			249	—		
4	T	Run supply current LPS = 1, all modules off, running from flash	16 kHz FBELP	RI_{DD}	3	50	—	µA	—
5	C	Wait mode supply current FEI mode, all modules off	25.165 MHz	WI_{DD}	3	51.1	69	mA	–40 to 85°C
	T		20 MHz			42.6	—		
	T		8 MHz			18.8	—		
	T		1			3.69	—		
6	T	Wait mode supply current LPRS = 1, all mods off		WI_{DD}	3	1	—	µA	—
7	P	Stop2 mode supply current		$S2I_{DD}$	3	0.576	30	µA	–40 to 85°C
	C				2		16		
8	P	Stop3 mode supply current		$S3I_{DD}$	3	1.05	45	µA	–40 to 85°C
	C				2		27		
9	T	LVD adder to stop3, stop2 (LVDE = LVDSE = 1)		$S3I_{DDLVD}$	3	120	—	µA	—
10	T	Voltage reference adder to stop3	Low power mode	$S3I_{DDLVD}$	3	90	—	µA	—
			Tight regulation mode			270			
11	T	PRACMP adder to stop3	PRG disabled	$S3I_{DDLVD}$	3	13	—	µA	—
			PRG enabled			29			
12	T	LCD adder to stop3, stop2, VIREG enabled, 1/4 duty cycle, 4x39 configuration for 156 segments, 32Hz frame rate, no LCD glass connected		$S3I_{DDLVD}$	3	1.3	—	µA	—
13	C	Adder to stop3 for oscillator enabled[2] (ERCLKEN =1 and EREFSTEN = 1)		$S3I_{DDOSC}$	3	5		µA	—

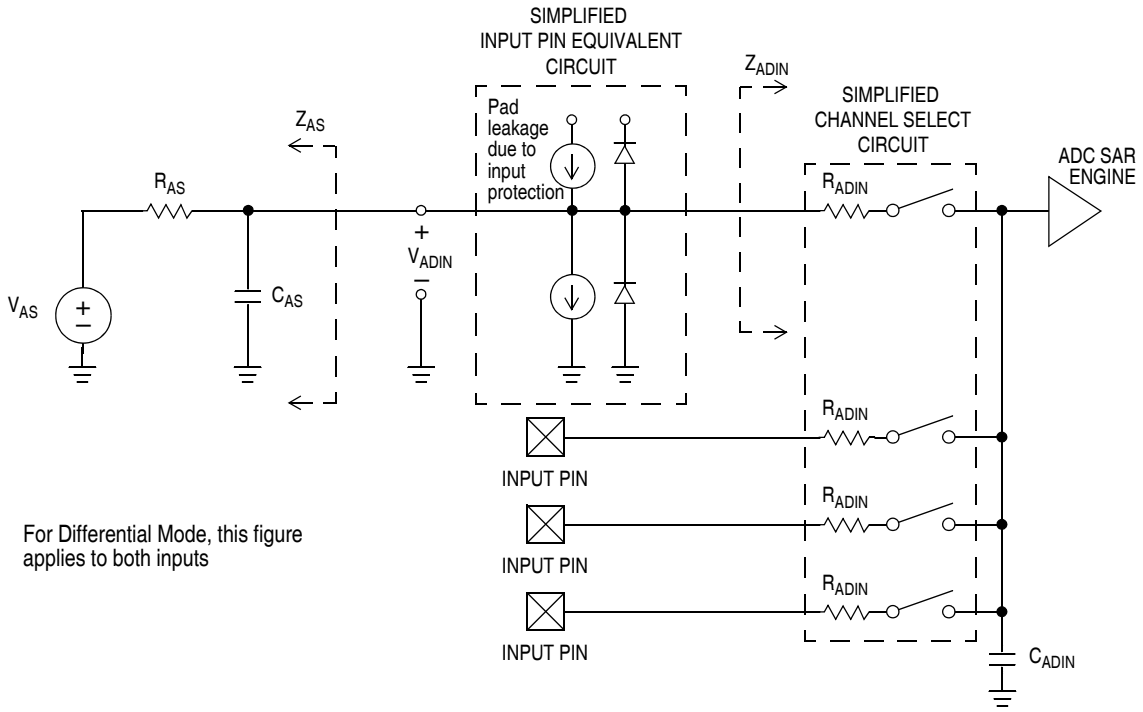


Figure 10. ADC Input Impedance Equivalency Diagram

Table 14. 16-bit ADC Characteristics full operating range($V_{REFH} = V_{DDAD} > 1.8$, $V_{REFL} = V_{SSAD}$, $F_{ADCK} \leq 8$MHz)

Characteristic	Conditions[1]	C	Symb	Min	Typ[2]	Max	Unit	Comment
Supply Current	ADLPC = 1, ADHSC = 0	T	I_{DDA}	—	215	—	μA	ADLSMP = 0 ADCO = 1
	ADLPC = 0, ADHSC = 0			—	470	—		
	ADLPC=0, ADHSC=1			—	610	—		
Supply Current	Stop, Reset, Module Off	C	I_{DDA}	—	0.01	—	μA	
ADC Asynchronous Clock Source	ADLPC = 1, ADHSC = 0	P	f_{ADACK}	—	2.4	—	MHz	$t_{ADACK} = 1/f_{ADACK}$
	ADLPC = 0, ADHSC = 0			—	5.2	—		
	ADLPC = 0, ADHSC = 1			—	6.2	—		
Sample Time	See reference manual for sample times							
Conversion Time	See reference manual for conversion times							

Table 15. 16-bit ADC Characteristics(V_{REFH} = V_{DDAD} ≥ 2.7V, V_{REFL} = V_{SSAD}, F_{ADCK} ≤ 4MHz, ADHSC=1)

Characteristic	Conditions[1]	C	Symb	Min	Typ[2]	Max	Unit	Comment
Full-Scale Error	16-bit differential mode 16-bit single-ended mode	T	E_{FS}	— —	+8/0 +12/0	+24/0 +24/0	LSB^2	V_{ADIN} = V_{DDAD}
	13-bit differential mode 12-bit single-ended mode	T		— —	±0.7 ±0.7	±2.0 ±2.5		
	11-bit differential mode 10-bit single-ended mode	T		— —	±0.4 ±0.4	±1.0 ±1.0		
	9-bit differential mode 8-bit single-ended mode	T		— —	±0.2 ±0.2	±0.5 ±0.5		
Quantization Error	16 bit modes	D	E_Q	—	-1 to 0	—	LSB^2	
	≤13 bit modes			—	—	±0.5		
Effective Number of Bits	16 bit differential mode Avg = 32 Avg = 16 Avg = 8 Avg = 4 Avg = 1	C	ENOB	 14.3 13.8 13.4 13.1 12.4	 14.5 14.0 13.7 13.4 12.6	 — — — — —	Bits	F_{in} = F_{sample}/100
Signal to Noise plus Distortion	See ENOB		SINAD	$SINAD = 6.02 \cdot ENOB + 1.76$			dB	
Total Harmonic Distortion	16–bit differential mode Avg = 32	C	THD	—	-95.8	-90.4	dB	F_{in} = F_{sample}/100
	16–bit single-ended mode Avg = 32	D		—	—	—		
Spurious Free Dynamic Range	16–bit differential mode Avg = 32	C	SFDR	 91.0	 96.5	 —	dB	F_{in} = F_{sample}/100
	16–bit single-ended mode Avg = 32	D		—	—	—		
Input Leakage Error	all modes	D	E_{IL}	I_{In} * R_{AS}			mV	I_{In} = leakage current (refer to DC characteristics)
Temp Sensor Slope	–40°C–25°C	D	m	—	1.646	—	mV/°C	
	25°C–125°C			—	1.769	—		
Temp Sensor Voltage	25°C	D	V_{TEMP25}	—	701.2	—	mV	

1 All accuracy numbers assume the ADC is calibrated with V_{REFH}=V_{DDAD}

2 Typical values assume V_{DDAD} = 3.0 V, Temp = 25 °C, f_{ADCK}=2.0MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

3 1 LSB = (V_{REFH}–V_{REFL})/2^N

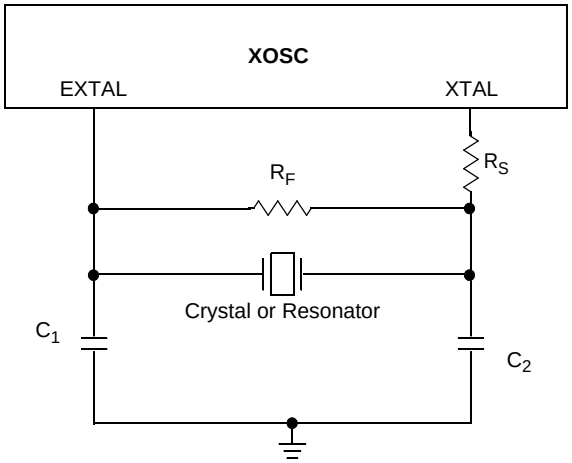


Figure 11. Typical Crystal or Resonator Circuit: High Range and Low Range/High Gain

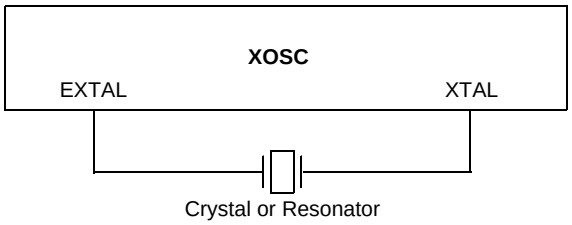


Figure 12. Typical Crystal or Resonator Circuit: Low Range/Low Gain

2.10 Internal Clock Source (ICS) Characteristics

Table 17. ICS Frequency Specifications (Temperature Range = –40 to 85 °C Ambient)

Num	C	Characteristic		Symbol	Min	Typical[1]	Max	Unit
1	P	Average internal reference frequency — factory trimmed at V_{DD} = 3.6 V and temperature = 25 °C		f_{int_ft}	—	32.768	—	kHz
2	P	Internal reference frequency — user trimmed		f_{int_ut}	31.25	—	39.06	kHz
3	T	Internal reference start-up time		t_{IRST}	—	60	100	µs
4	P	DCO output frequency range — trimmed[2]	Low range (DRS = 00)	f_{dco_u}	16	—	20	MHz
	C		Mid range (DRS = 01)		32	—	40	
	P		High range (DRS = 10)		48	—	60	
5	P	DCO output frequency[2] Reference = 32768 Hz and DMX32 = 1	Low range (DRS = 00)	f_{dco_DMX32}	—	19.92	—	MHz
	P		Mid range (DRS = 01)		—	39.85	—	
	P		High range (DRS = 10)		—	59.77	—	
6	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)		$\Delta f_{dco\_res\_t}$	—	±0.1	±0.2	$\%f_{dco}$
7	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)		$\Delta f_{dco\_res\_t}$	—	±0.2	±0.4	$\%f_{dco}$

2.13 VREF Characteristics

Table 21. VREF Electrical Specifications

Num	C	Characteristic	Symbol	Min	Typical	Max	Unit
1	—	Supply voltage	V_{DDAD}	1.80	—	3.60	V
2	—	Operating temperature range	T_{op}	–40	—	105	°C
3	D	Load capability	I_{load}	—	—	10	mA
4	C P	Voltage reference output untrimmed factory trimmed	V_{REFO}	 1.070 1.04	 — 1.150	 1.202 1.17	 V V
5	D	Load regulation mode = 10, I_{load} = 1 mA		20	—	100	µV/mA
6	T	Line regulation (power supply rejection) DC AC		±0.1 from room temp voltage –60			 mV dB
7	T	Bandgap only (mode = 00)	I_{BG}	—	72	—	µA
8	C	Low power mode (mode = 01)	I_{LP}	—	90	125	µA
9	T	Tight regulation mode (mode =10)	I_{TR}	—	0.27	—	mA

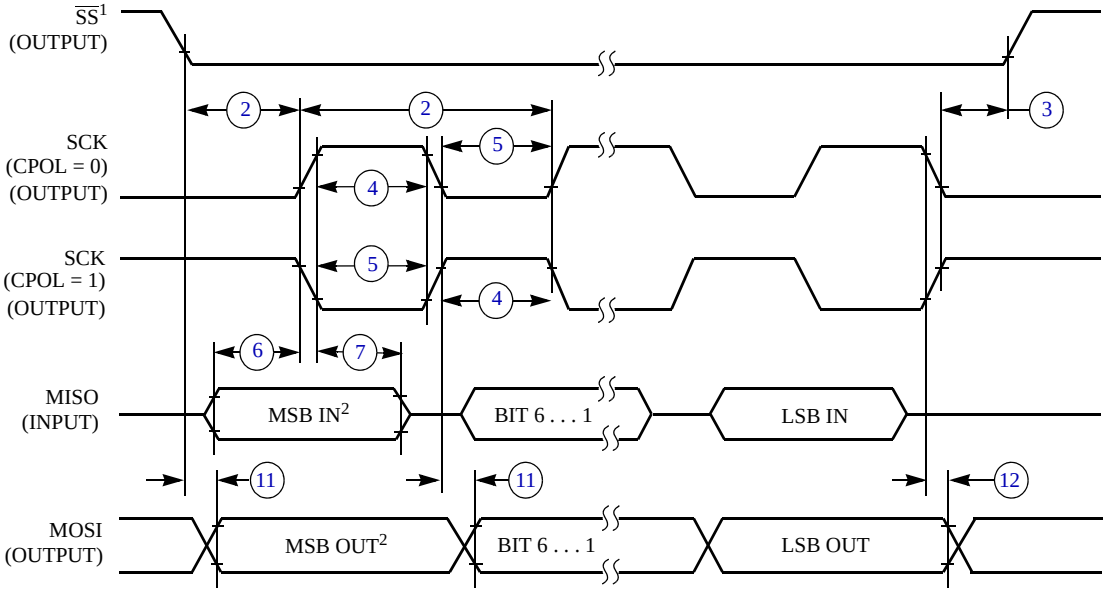
2.14 SPI Characteristics

Table 22 and Figure 19 through Figure 22 describe the timing requirements for the SPI system.

4 All timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless noted; 100 pF load on all SPI pins. All timing assumes slew rate control disabled and high drive strength enabled for SPI output pins.

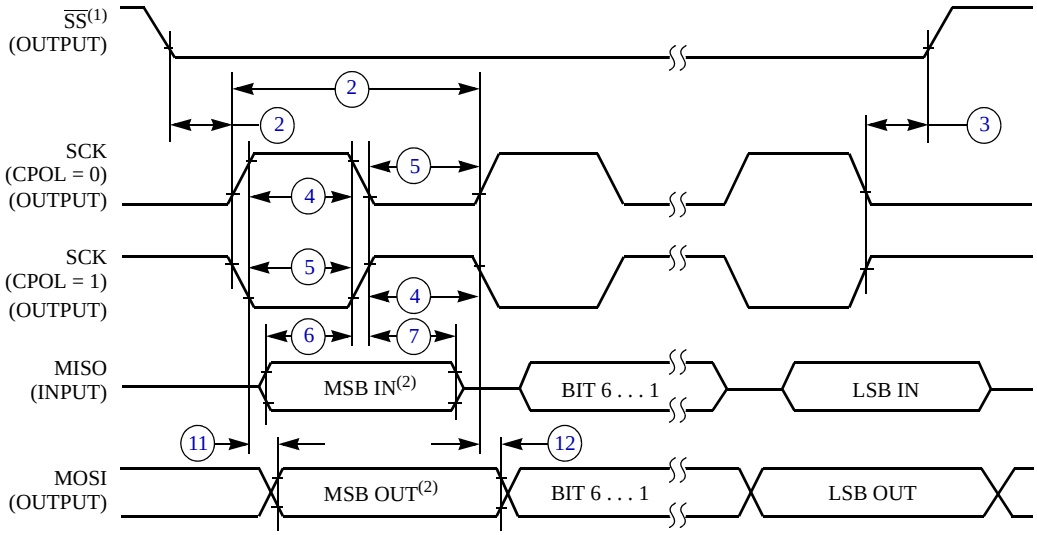
5 Time to data active from high-impedance state.

6 Hold time to high-impedance state.



NOTES:
1. $\overline{SS}$ output mode (MODFEN = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 19. SPI Master Timing (CPHA = 0)



NOTES:
1. $\overline{SS}$ output mode (MODFEN = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 20. SPI Master Timing (CPHA = 1)

freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASS23308W
		PAGE: 983
	DO NOT SCALE THIS DRAWING	REV: H

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DATUMS B, C AND D TO BE DETERMINED AT DATUM PLANE H.
4. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE SIZE BY A MAXIMUM OF 0.1 MM.
5. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSIONS. THE MAXIMUM ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THE DIMENSIONS ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
6. DIMENSION DOES NOT INCLUDE DAM BAR PROTRUSION. PROTRUSIONS SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.35. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL BE 0.07 MM.
7. DIMENSIONS ARE DETERMINED AT THE SEATING PLANE, DATUM A.

TITLE: 100 LEAD LQFP 14 X 14, 0.5 PITCH, 1.4 THICK	CASE NUMBER: 983–02	
	STANDARD: NON–JEDEC	
	PACKAGE CODE: 8264	SHEET: 3 OF 4