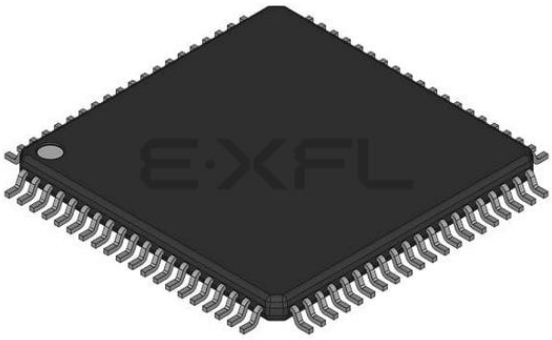

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V1
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, SCI, SPI
Peripherals	LCD, LVD, PWM, WDT
Number of I/O	56
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 12x16b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf51em256clk

1 MCF51EM256 Series Configurations

1.1 Device Comparison

The MCF51EM256 series is summarized in Table 1.

Table 1. MCF51EM256 Series Features by MCU and Package

Feature	MCF51EM256		MCF51EM128	
Flash size (bytes)	262144		131072	
RAM size (bytes)	16384		8192	
Robust flash update supported	Yes			
Pin quantity	100	80	100	80
PRACMP1 inputs	5	3	5	3
PRACMP2 inputs	5			
ADC modules	4		4	
ADC differential channels[1]	4	2	4	2
ADC single-ended channels	16	12	16	12
DBG	Yes			
ICS	Yes			
IIC	Yes			
IRQ	Yes			
IRTC	Yes			
VREF	Yes			
LCD drivers	44	37	44	37
Rapid GPIO[2]	16	16	16	16
Port I/O[3]	47	40	47	40
Keyboard interface 1	8			
Keyboard interface 2	8			
SCI1	Yes			
SCI2	Yes			
SCI3	Yes			
SPI1 (FIFO)	Yes			
SPI2 (standard)	Yes			
SPI3 (standard)	Yes	No	Yes	No

Table 1. MCF51EM256 Series Features by MCU and Package (continued)

Feature	MCF51EM256	MCF51EM128
MTIM1 (8-bit)	Yes	
MTIM2 (8-bit)	Yes	
MTIM3 (16-it)	Yes	
TPM channels	2	
PDB	Yes	
XOSC1[4]	Yes	
XOSC2[5]	Yes	

1 Each differential channel is comprised of 2 pin inputs

2 RGPIO is muxed with standard Port I/O

3 Port I/O count does not include the ouput only PTC2/BKGD/MS.

4 IRTC crystal input and possible crystal input to the ICS module

5 Main external crystal input for the ICS module

1.2 Block Diagram

Figure 1 shows the connections between the MCF51EM256 series pins and modules.

1.3 Features

Table 2 describes the functional units of the MCF51EM256 series.

Table 2. MCF51EM256 Series Functional Units

Unit	Function
ADC (analog-to-digital converter)	Measures analog voltages at up to 16 bits of resolution. Each ADC has up to four differential and 24 single-ended inputs.
BDM (background debug module)	Provides single pin debugging interface (part of the V1 ColdFire core)
CF1 CORE (V1 ColdFire core) with MAC unit	Executes programs, handles interrupts and containes multiply-accumulate hardware (MAC).
PRACMP1, PRACMP2 (comparators)	Analog comparators for comparing external analog signals against each other, or a variety of reference levels.
COP (computer operating poperly)	Software watchdog
IRQ (interrupt request)	Single pin high priority interrupt (part of the V1 ColdFire core)
CRC (cyclic Redundancy Check)	High-speed CRC calculation
DBG (debug)	Provides debugging and emulation capabilities (part of the V1 ColdFire core)
FLASH (flash memory)	Provides storage for program code, constants and variables
IIC (inter-integrated circuits)	Supports standard IIC communications protocol and SMBus
INTC (interrupt controller)	Controls and prioritizes all device interrupts
KBI1 & KBI2	Keyboard Interfaces 1 and 2
LCD	Liquid crystal display driver
LVD (low voltage detect)	Provides an interrupt to the CF1CORE in the event that the supply voltage drops below a critical value. The LVD can also be programmed to reset the device upon a low voltage event
ICS (internal clock source)	Provides clocking options for the device, including a three frequency-locked loops (FLLs) for multiplying slower reference clock sources
IRTC (independent real-time clock)	The independent real time clock provides an independent time-base with optional interrupt, battery backup and tamper protection
VREF (voltage reference)	The voltage reference output is available for both on and off-chip use
MTIM1, MTIM2 (modulo timers)	8-bit modulo timers with configurable clock inputs and interrupt generation on overflow
MTIM3 (modulo timer)	16-bit modulo timer with configurable clock inputs and interrupt generation on overflow
PDB (programmable delay block)	This timer is optimized for scheduling ADC conversions
RAM (random-access memory)	Provides stack and variable storage
RGPIO (rapid general-purpose input/output)	Allows for I/O port access at CPU clock speeds and is used to implement GPIO functionality for PTA and PTB.

Table 2. MCF51EM256 Series Functional Units (continued)

Unit	Function
SCI1, SCI2, SCI3(serial communications interfaces)	Serial communications UARTs capable of supporting RS-232 and LIN protocols
SIM (system integration unit)	
SPI1 (FIFO), SPI2, SPI3 (serial peripheral interfaces)	SPI1 has full-complementary drive outputs. SPI2 may be configured with full-complementary drive output via LCD control registers. SPI3 has open drain outputs on SCLK and (MISO or MOSI). These coupled with off-chip pull-up resistors, allow interface to an external 5 V SPI.
TPM (Timer/PWM Module)	Timer/PWM module can be used for a variety of generic timer operations as well as pulse-width modulation
VREG (voltage regulator)	Controls power management across the device
XOSC1 and XOSC2 (crystal oscillators)	These devices incorporate redundant crystal oscillators in separate power domains.One is intended primarily for use by the IRTC, and the other by the CPU and other peripherals.

1.3.1 Feature List

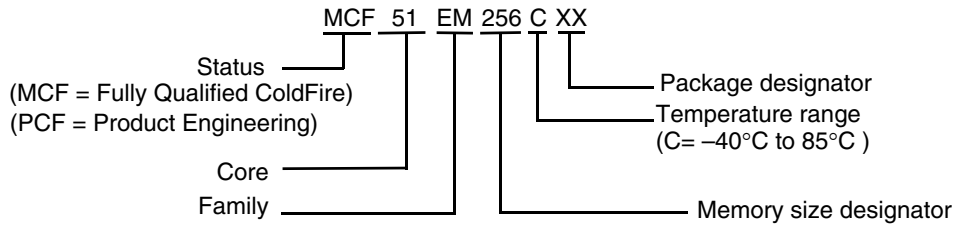
- 32-bit ColdFire V1 central processor unit (CPU)
  - Up to 50.33 MHz ColdFire CPU from 3.6 V to 2.5 V and 20 MHz CPU at 3.6 V to 1.8 V across temperature range of –40 °C to 85 °C
  - ColdFire instruction set revision C (ISA_C) plus MAC
  - 32-bit multiply and accumulate (MAC) optimized for 16×16±32 operations; supports signed or unsigned integer or signed fractional inputs
- On-chip memory
  - MCF51EM256/128 series support two independent flash arrays; read/program/erase over full operating voltage and temperature; allows interrupt processing while programming for robust program updates
  - Random-access memory (RAM)
  - Security circuitry to prevent unathorized access to RAM and Flash contents
- Power-saving modes
  - Two ultra-low power stop modes
  - New low-power run and low-power wait modes
  - Reduced power wait mode
  - Peripheral clock enable register can disable clocks to unused modules, thereby reducing currents
  - Ultra-low power independent real time clock with calendar features (IRTC); runs in all MCU modes; external clock source with trim capabilities; independent voltage source runs IRTC when MCU is powered-down; tamper detection and indicator; battery monitor output to ADC; unaffected by MCU resets
  - Ultra-low power external oscillator that can be used in stop modes to provide accurate clock source to IRTC, ICS and LCD

front-plane/backplane pin assignments; operation in all low power modes with blink functionality

- **SCIx** — Three serial communications interface modules with optional 13-bit break; option to connect Rx input to PRACMP output on SCI1 and SCI2; high current drive on Tx on SCI1 and SCI2; wakeup from stop3 on Rx edge. SCI1 and SCI2 Tx pins can be modulated with timer outputs for use with IR interfaces
- **SPIx—** Two serial peripheral interfaces (SPI2, SPI3) with full-duplex or single-wire bidirectional; double-buffered transmit and receive; master or slave mode; MSB-first or LSB-first shifting
- **SPI16**— Serial peripheral interface (SPI1) with 32-bit FIFO buffer; 16-bit or 8-bit data transfers; full-duplex or single-wire bidirectional; double-buffered transmit and receive; master or slave mode; MSB-first or LSB-first shifting
- **IIC** — Up to 100 kbps with maximum bus loading; multi-master operation; programmable slave address; interrupt driven byte-by-byte data transfer; supports broadcast mode and 10 bit addressing
- **MTIMx** — Two 8-bit and one 16-bit modulo timers with 4-bit prescaler; overflow interrupt; external clock input/pulse accumulator
- **TPM** — 2-channel Timer/PWM module; selectable input capture, output compare, or buffered edge- or center-aligned PWM on each channel; external clock input/pulse accumulator; can be used modulate SCI1 and SCI2 TX pins

- Input/output
  - up to 16 rapid GPIO and 48 standard GPIOs, including 1 output-only pin and 3 open-drain pins.
  - up to 16 keyboard interrupts with selectable polarity
  - Hysteresis and configurable pullup device on all input pins; configurable slew rate and drive strength on all output pins
- Package options
  - 100-pin LQFP, 80-pin LQFP

1.4 Part Numbers



1.5.2 Pinout: 100-Pin LQFP

Figure 3 shows the pinout configuration for the 100-pin LQFP. Pins which are blacked out do not have an equivalent pin on the 80-pin LQFP package.

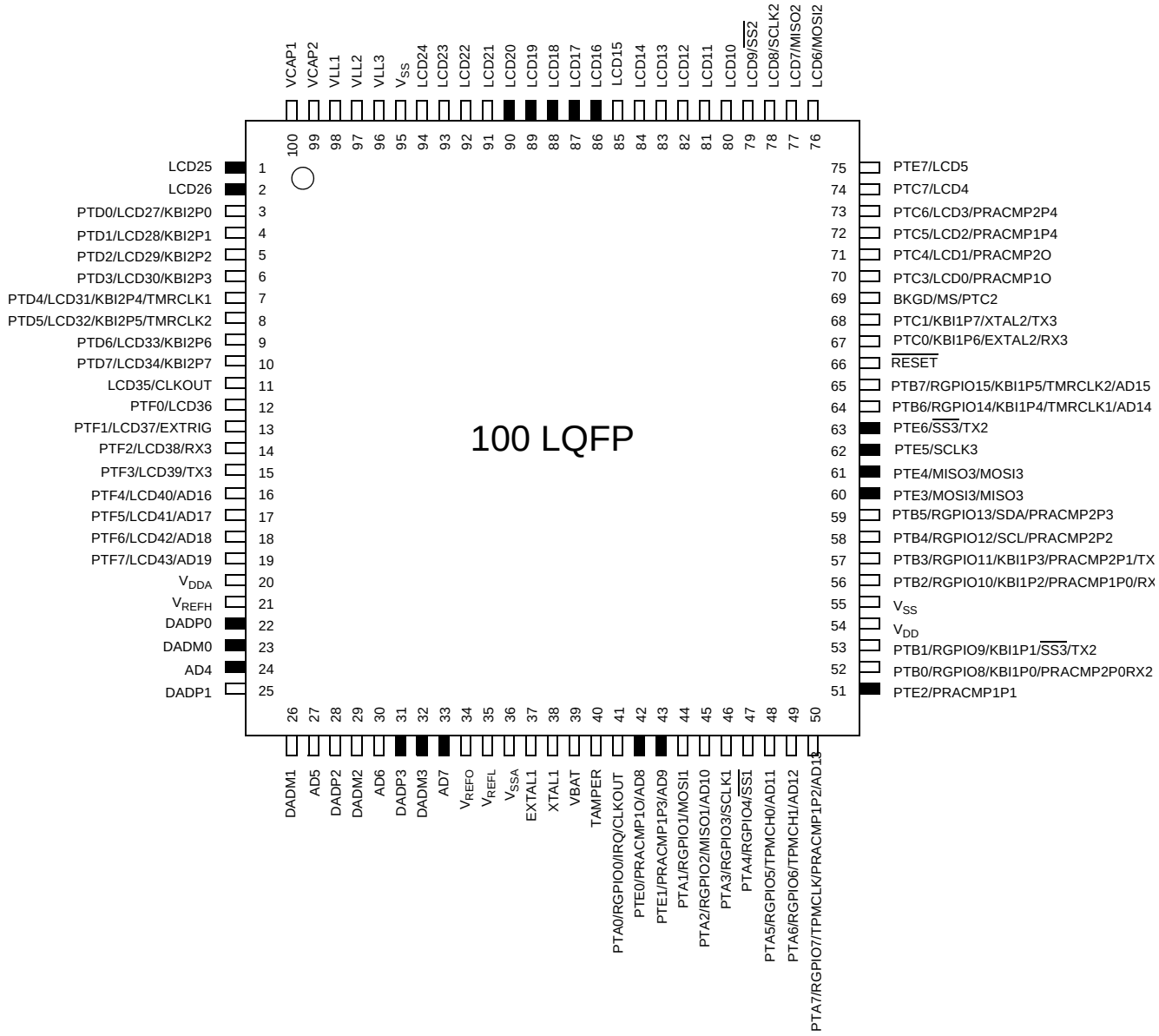


Figure 3. 100-Pin LQFP Pinout

Table 4 shows the package pin assignments.

Table 4. MCF51EM256 Series Package Pin Assignments (continued)

100 LQFP	80 LQFP	Default Function	ALT1	ALT2	ALT3	Comment
58	47	PTB4/RGPIO12	SCL	PRACMP2P2		RGPIO_ENB is used to select between standard GPIO and RGPIO
59	48	PTB5/RGPIO13	SDA	PRACMP2P3		
60	—	PTE3	MOSI3	MISO3		
61	—	PTE4	MISO3	MOSI3		Open Drain
62	—	PTE5	SCLK3			Open Drain
63	—	PTE6	$\overline{SS3}$	TX2		Open Drain
64	49	PTB6/RGPIO14	KBI1P4	TMRCLK1	AD14	RGPIO_ENB is used to select between standard GPIO and RGPIO
65	50	PTB7/RGPIO15	KBI1P5	TMRCLK2	AD15	
66	51	$\overline{RESET}$				This pin is an open drain device and has an internal pullup. There is no clamp diode to V_{DD}.
67	52	PTC0	KBI1P6	EXTAL2	RX3	
68	53	PTC1	KBI1P7	XTAL2	TX3	
69	54	BKGD/MS	PTC2			This pin has an internal pullup. PTC2 can only be programmed as an output.
70[1]	55[1]	PTC3	LCD0	PRACMP1O		
71[1]	56[1]	PTC4	LCD1	PRACMP2O		
72[1]	57[1]	PTC5	LCD2		PRACMP1P4	
73[1]	58[1]	PTC6	LCD3		PRACMP2P4	
74[1]	59[1]	PTC7	LCD4			
75[1]	60[1]	PTE7	LCD5			
76[1]	61[1]	LCD6	MOSI2			
77[1]	62[1]	LCD7	MISO2			
78[1]	63[1]	LCD8	SCLK2			
79[1]	64[1]	LCD9	$\overline{SS2}$			
80	65	LCD10				
81	66	LCD11				
82	67	LCD12				
83	68	LCD13				
84	69	LCD14				
85	70	LCD15				
86	—	LCD16				

$$T_J = T_A + (P_D \times \theta_{JA}) \quad \textit{Eqn. 1}$$

where:

T_A = Ambient temperature, °C
θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W
$P_D = P_{int} + P_{I/O}$
$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power
$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad \textit{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (P_D)^2 \quad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

2.4 Electrostatic Discharge (ESD) Protection Characteristics

Although damage from static discharge is much less common on these devices than on early CMOS circuits, normal handling precautions should be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with CDF-AEC-Q00 Stress Test Qualification for Automotive Grade Integrated Circuits. (http://www.aecouncil.com/) This device was qualified to AEC-Q100 Rev E.

A device is considered to have failed if, after exposure to ESD pulses, the device no longer meets the device specification requirements. Complete dc parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 8. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series Resistance	R1	1500	Ω
	Storage Capacitance	C	100	pF
	Number of Pulse per pin	—	3	
Machine	Series Resistance	R1	0	Ω
	Storage Capacitance	C	200	pF
	Number of Pulse per pin	—	3	
Latch-up	Minimum input voltage limit		–2.5	V
	Maximum input voltage limit		7.5	V

Table 10. DC Characteristics (continued)

Num	C	Parameter		Symbol	Min	Typical[1]	Max	Unit
8	C	Output low voltage	PTA[7:0], PTB[7:0], PTC[2:0], PTE[6:0], low-drive strength. $V_{DD} \geq 1.8$ V, $I_{Load} = 2$ mA	V_{OL}	—	—	0.50	V
	P		PTA[7:0], PTB[7:0], PTC[2:0], PTE[6:0], high-drive strength. $V_{DD} \geq 2.7$ V, $I_{Load} = 10$ mA					
	C		PTA[7:0], PTB[7:0], PTC[2:0], PTE[6:0], high-drive strength. $V_{DD} \geq 1.8$ V, $I_{Load} = 3$ mA					
9	C	Output low voltage	PTC[7:3], PTD[7:0], PTE7, PTF[7:0], LCD35/CLKOUT, MOSI2, MISO2, SCK2, SS2, low drive strength. VDD ≥ 1.8 V, $I_{Load} = 0.5$ mA	V_{OL}	—	—	0.50	V
	P		PTC[7:3], PTD[7:0], PTE7, PTF[7:0], LCD35/CLKOUT, MOSI2, MISO2, SCK2, SS2, high-drive strength. $V_{DD} \geq 2.7$ V, $I_{Load} = 3$ mA					
	C		PTC[7:3], PTD[7:0], PTE7, PTF[7:0], LCD35/CLKOUT, MOSI2, MISO2, SCK2, SS2, high-drive strength. $V_{DD} \geq 1.8$ V, $I_{Load} = 1$ mA					
10	D	Output low current	Max total I_{OL} for all ports	I_{OLT}	—	—	100	mA
11	P	Input high voltage	All digital inputs except tamper_in, $V_{DD} > 2.7$ V	V_{IH}	$0.70 \times V_{DD}$	—	—	V
			All digital inputs except tamper_in, $2.7 \text{ V} > V_{DD} \geq 1.8$ V		$0.85 \times V_{DD}$	—	—	
			Tamper_in		1.5	—	—	
12	P	Input low voltage	All digital inputs except tamper_in, $V_{DD} > 2.7$ V	V_{IL}	—	—	$0.35 \times V_{DD}$	V
			all digital inputs except tamper_in, $2.7 \text{ V} > V_{DD} \geq 1.8$ V		—	—	$0.3 \times V_{DD}$	
			Tamper_in		—	—	0.5	
13	C	Input hysteresis; all digital inputs		V_{hys}	$0.06 \times V_{DD}$	—	—	mV
14	P	Input leakage current; input only pins[4]		$\lvert I_{In} \rvert$	—	0.1	1	μA
15	P	High Impedance (off-state) leakage current[4]		$\lvert I_{OZ} \rvert$	—	0.1	1	μA
16	P	Internal pullup resistors[5]		R_{PU}	17.5	—	52.5	kΩ
17	P	Internal pulldown resistors[6]		R_{PD}	17.5	—	52.5	kΩ
18	C	Input capacitance; all non-supply pins		C_{In}	—	—	8	pF
19	P	POR rearm voltage		V_{POR}	0.9	1.4	2.0	V
20	D	POR rearm time		t_{POR}	10	—	—	μs
21	P	Low-voltage detection threshold	High range — V_{DD} falling	V_{LVDH}	2.300	2.355	2.410	V
			High range — V_{DD} rising		2.370	2.425	2.480	

Table 11. Supply Current Characteristics

Num	C	Parameter		Symbol	V_{DD} (V)	Typical[1]	Max	Unit	Temp (°C)
1	P	Run supply current FEI mode, all modules on	25.165 MHz	RI_{DD}	3	66.2	100	mA	–40 to 85°C
	T		20 MHz			55.3	—		
	T		8 MHz			23.9	—		
	T		1 MHz			4.56	—		
2	C	Run supply current FEI mode, all modules off	25.165 MHz	RI_{DD}	3	55.1	56	mA	–40 to 85°C
	T		20 MHz			46.6	—		
	T		8 MHz			19.9	—		
	T		1 MHz			3.92	—		
3	T	Run supply current LPS=0, all modules off	16 kHz FBILP	RI_{DD}	3	239	—	µA	—
	T		16 kHz FBELP			249	—		
4	T	Run supply current LPS = 1, all modules off, running from flash	16 kHz FBELP	RI_{DD}	3	50	—	µA	—
5	C	Wait mode supply current FEI mode, all modules off	25.165 MHz	WI_{DD}	3	51.1	69	mA	–40 to 85°C
	T		20 MHz			42.6	—		
	T		8 MHz			18.8	—		
	T		1			3.69	—		
6	T	Wait mode supply current LPRS = 1, all mods off		WI_{DD}	3	1	—	µA	—
7	P	Stop2 mode supply current		$S2I_{DD}$	3	0.576	30	µA	–40 to 85°C
	C				2		16		
8	P	Stop3 mode supply current		$S3I_{DD}$	3	1.05	45	µA	–40 to 85°C
	C				2		27		
9	T	LVD adder to stop3, stop2 (LVDE = LVDSE = 1)		$S3I_{DDLVD}$	3	120	—	µA	—
10	T	Voltage reference adder to stop3	Low power mode	$S3I_{DDLVD}$	3	90	—	µA	—
			Tight regulation mode			270			
11	T	PRACMP adder to stop3	PRG disabled	$S3I_{DDLVD}$	3	13	—	µA	—
			PRG enabled			29			
12	T	LCD adder to stop3, stop2, VIREG enabled, 1/4 duty cycle, 4x39 configuration for 156 segments, 32Hz frame rate, no LCD glass connected		$S3I_{DDLVD}$	3	1.3	—	µA	—
13	C	Adder to stop3 for oscillator enabled[2] (ERCLKEN =1 and EREFSTEN = 1)		$S3I_{DDOSC}$	3	5		µA	—

2.7 Analog Comparator (PRACMP) Electricals

Table 12. PRACMP Electrical Specifications

N	C	Characteristic	Symbol	Min	Typical	Max	Unit
1	—	Supply voltage	V_{PWR}	1.8	—	3.6	V
2	C	Supply current (active) (PRG enabled)	I_{DDACT1}	—	—	60	μA
3	C	Supply current (active) (PRG disabled)	I_{DDACT2}	—	—	40	μA
4	D	Supply current (ACMP and PRG all disabled)	I_{DDDIS}	—	—	2	nA
5	—	Analog input voltage	VAIN	V_{SS} – 0.3	—	V_{DD}	V
6	T	Analog input offset voltage	VAIO	—	5	40	mV
7	T	Analog comparator hysteresis	V_H	3.0	—	20.0	mV
8	D	Analog input leakage current	I_{ALKG}	—	—	1	nA
9	T	Analog comparator initialization delay	t_{AINIT}	—	—	1.0	μs
10	—	Programmable reference generator input1	$V_{In1}(V_{DD})$	—	V_{DD}	—	V
11	T	Programmable reference generator input2	$V_{In2}(V_{DD25})$	1.8	—	2.75	V
12	D	Programmable reference generator setup delay	t_{PRGST}	—	1	—	μs
13	D	Programmable reference generator step size	Vstep	–0.25	0	0.25	LSB
14	P	Programmable reference generator voltage range	V_{prgout}	$V_{In}/32$	—	V_{in}	V

2.8 ADC Characteristics

These specs all assume seperate V_{DDAD} supply for ADC and isolated pad segment for ADC supplies and differential inputs. Spec's should be de-rated for $V_{REFH} = V_{bg}$ condition.

Table 13. 16-bit ADC Operating Conditions

Num	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
1	Supply voltage	Absolute	V_{DDA}	1.8	—	3.6	V	
2		Delta to V_{DD} (V_{DD}–V_{DDA})[2]	ΔV_{DDA}	–100	0	100	mV	
3	Ground voltage	Delta to V_{SS} (V_{SS}–V_{SSA})[2]	ΔV_{SSA}	–100	0	100	mV	
4	Ref Voltage High		V_{REFH}	1.15	V_{DDA}	V_{DDA}	V	

Table 13. 16-bit ADC Operating Conditions

Num	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
5	Ref Voltage Low		V_{REFL}	V_{SSA}	V_{SSA}	V_{SSA}	V	
6	Input Voltage		V_{ADIN}	V_{REFL}	—	V_{REFH}	V	
7	Input Capacitance	16-bit modes 8/10/12-bit modes	C_{ADIN}	—	8 4	10 5	pF	
8	Input Resistance		R_{ADIN}	—	2	5	kΩ	
9	Analog Source Resistance	16 bit modes f_{ADCK} > 8MHz 4MHz < f_{ADCK} < 8MHz f_{ADCK} < 4MHz	R_{AS}	— — —	— — —	0.5 1 2	kΩ	External to MCU Assumes ADLSMP=0
10		13/12 bit modes f_{ADCK} > 8MHz 4MHz < f_{ADCK} < 8MHz f_{ADCK} < 4MHz		— — —	— — —	1 2 5		
11		11/10 bit modes f_{ADCK} > 8MHz 4MHz < f_{ADCK} < 8MHz f_{ADCK} < 4MHz		— — —	— — —	2 5 10		
12		9/8 bit modes f_{ADCK} > 8MHz f_{ADCK} < 8MHz		— —	— —	5 10		
13	ADC Conversion Clock Freq.	ADLPC = 0, ADHSC = 1	f_{ADCK}	1.0	—	8	MHz	
14		ADLPC = 0, ADHSC = 0		1.0	—	5		
15		ADLPC = 1, ADHSC = 0		1.0	—	2.5		

1 Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 DC potential difference.

Table 14. 16-bit ADC Characteristics full operating range($V_{REFH} = V_{DDAD} > 1.8$, $V_{REFL} = V_{SSAD}$, $F_{ADCK} \leq 8MHz$)

Characteristic	Conditions[1]	C	Symb	Min	Typ[2]	Max	Unit	Comment
Full-Scale Error	16-bit differential mode 16-bit single-ended mode	T	E_{FS}	— —	+10/0 +14/0	+42/-2 +46/-2	LSB[2]	$V_{ADIN} = V_{DDAD}$
	13-bit differential mode 12-bit single-ended mode	T		— —	±1.0 ±1.0	±3.5 ±3.5		
	11-bit differential mode 10-bit single-ended mode	T		— —	±0.4 ±0.4	±1.5 ±1.5		
	9-bit differential mode 8-bit single-ended mode	T		— —	±0.2 ±0.2	±0.5 ±0.5		
Quantization Error	16 bit modes	D	E_Q	—	-1 to 0	—	LSB[2]	
	≤13 bit modes			—	—	±0.5		
Effective Number of Bits	16 bit differential mode Avg=32 Avg=16 Avg=8 Avg=4 Avg=1	C	ENOB	 12.8 12.7 12.6 12.5 11.9	 14.2 13.8 13.6 13.3 12.5	 — — — — —	Bits	$F_{in} = F_{sample}/100$
	16 bit single-ended mode Avg=32 Avg=16 Avg=8 Avg=4 Avg=1	C		 — — — — —	 TBD TBD TBD TBD TBD	 — — — — —		
Signal to Noise plus Distortion	See ENOB		SINAD	$SINAD = 6.02 \cdot ENOB + 1.76$			dB	
Total Harmonic Distortion	16-bit differential mode Avg = 32	C	THD	—	-91.5	-74.3	dB	$F_{in} = F_{sample}/100$
	16-bit single-ended mode Avg = 32	D		—	-85.5	—		
Spurious Free Dynamic Range	16-bit differential mode Avg = 32	C	SFDR	75.0	92.2	—	dB	$F_{in} = F_{sample}/100$
	16-bit single-ended mode Avg = 32	D		—	86.2	—		
Input Leakage Error	all modes	D	E_{IL}	$I_{In} * R_{AS}$			mV	I_{In} = leakage current (refer to DC characteristics)
Temp Sensor Slope	-40°C– 25°C	C	m	—	1.646	—	mV/°C	
	25°C– 125°C			—	1.769	—		
Temp Sensor Voltage	25°C	C	V_{TEMP25}	—	701.2	—	mV	

2.9 External Oscillator (XOSC) Characteristics

Reference Figure 11 and Figure 12 for crystal or resonator circuits. XOSC1 operates only in low power low range mode. XOSC2 operates in all the power and range modes.

Table 16. XOSC Specifications (Temperature Range = –40 to 85 °C Ambient)

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) Low range (RANGE = 0) High range (RANGE = 1), high gain (HGO = 1) High range (RANGE = 1), low power (HGO = 0)	 f_{lo} f_{hi} f_{hi}	 32 1 1	 — — —	 38.4 16 8	 kHz MHz MHz
2	D	Load capacitors Low range (RANGE=0), low power (HGO = 0) Other oscillator settings	C_1,C_2	See Note[2] See Note[3]			
3	D	Feedback resistor Low range, low power (RANGE = 0, HGO = 0)[2] Low range, high gain (RANGE = 0, HGO = 1) High range (RANGE = 1, HGO = X)	R_F	 — — —	 — 10 1	 — — —	MΩ
4	D	Series resistor — Low range, low power (RANGE = 0, HGO = 0)[2] Low range, high gain (RANGE = 0, HGO = 1) High range, low power (RANGE = 1, HGO = 0) High range, high gain (RANGE = 1, HGO = 1) ≥ 8 MHz 4 MHz 1 MHz	R_S	 — — — — — —	 — 0 100 0 0 0	 — — — 0 10 20	kΩ
5	T	Crystal start-up time [4] Low range, low power Low range, high power High range, low power High range, high power	 t_{CSTL} t_{CSTH} 	 — — — —	 600 400 5 15	 — — — —	ms
6	D	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) FEE mode FBE or FBELP mode	f_{extal}	0.03125 0	— —	50.33 50.33	MHz MHz

1 Data in Typical column was characterized at 3.0 V, 25 °C or is typical recommended value.

2 Load capacitors (C_1,C_2), feedback resistor (R_F) and series resistor (R_S) are incorporated internally when RANGE = HGO = 0.

3 See crystal or resonator manufacturer's recommendation.

4 Proper PC board layout procedures must be followed to achieve specifications.

Table 17. ICS Frequency Specifications (Temperature Range = –40 to 85 °C Ambient) (continued)

Num	C	Characteristic	Symbol	Min	Typical[1]	Max	Unit
8	C	Total deviation of trimmed DCO output frequency over voltage and temperature	Δf_{dco_t}	—	0.5 –1.0	±2	$\%f_{dco}$
9	C	Total deviation of trimmed DCO output frequency over fixed voltage and temperature range of 0 °C to 70 °C	Δf_{dco_t}	—	±0.5	±1	$\%f_{dco}$
10	C	FLL acquisition time [3]	$t_{Acquire}$	—	—	1	ms
11	C	Long term jitter of DCO output clock (averaged over 2 ms interval)[4]	C_{Jitter}	—	0.02	0.2	$\%f_{dco}$

1 Data in Typical column was characterized at 3.0 V, 25 °C or is typical recommended value.

2 The resulting bus clock frequency should not exceed the maximum specified bus clock frequency of the device.

3 This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

4 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{Bus}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

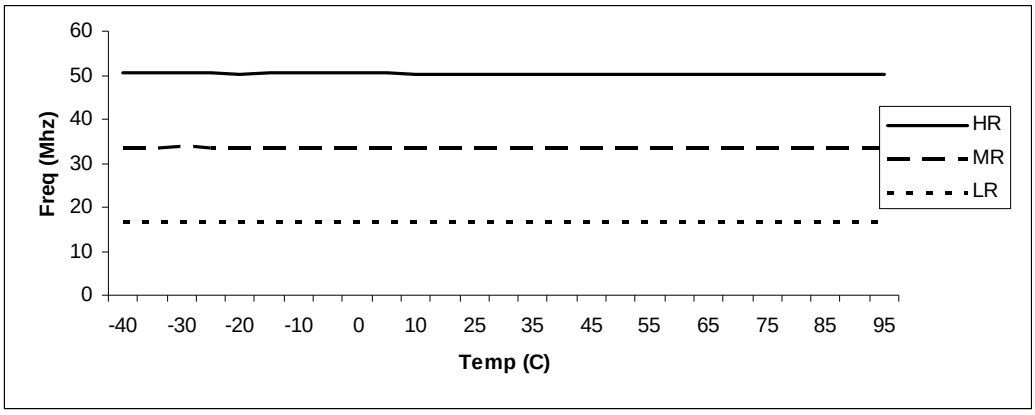
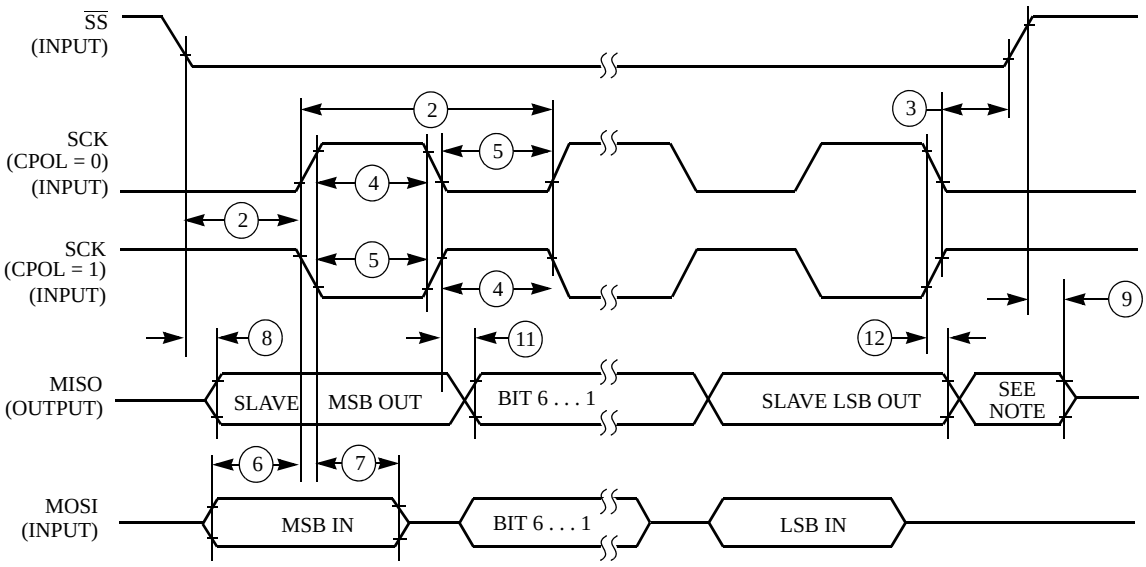
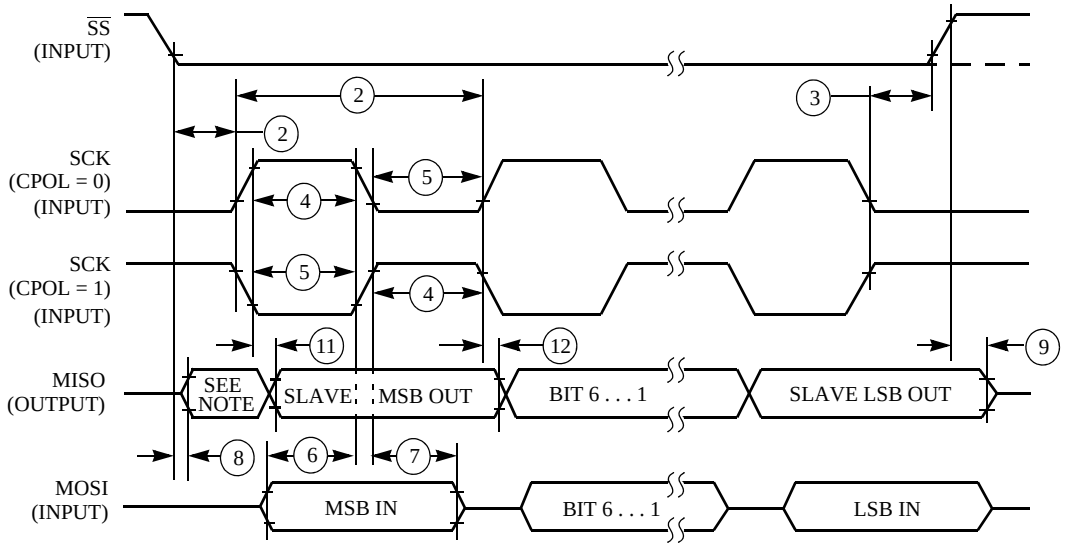


Figure 13. Deviation of DCO Output from Trimmed Frequency (50.33 MHz, 3.0 V)



NOTE:
1. Not defined but normally MSB of character just received

Figure 21. SPI Slave Timing (CPHA = 0)



NOTE:
1. Not defined but normally LSB of character just received

Figure 22. SPI Slave Timing (CPHA = 1)

2.15 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory section of the *MCF51EM256 Series ColdFire Microcontroller Reference Manual*.

freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASS23237W
		PAGE: 917A
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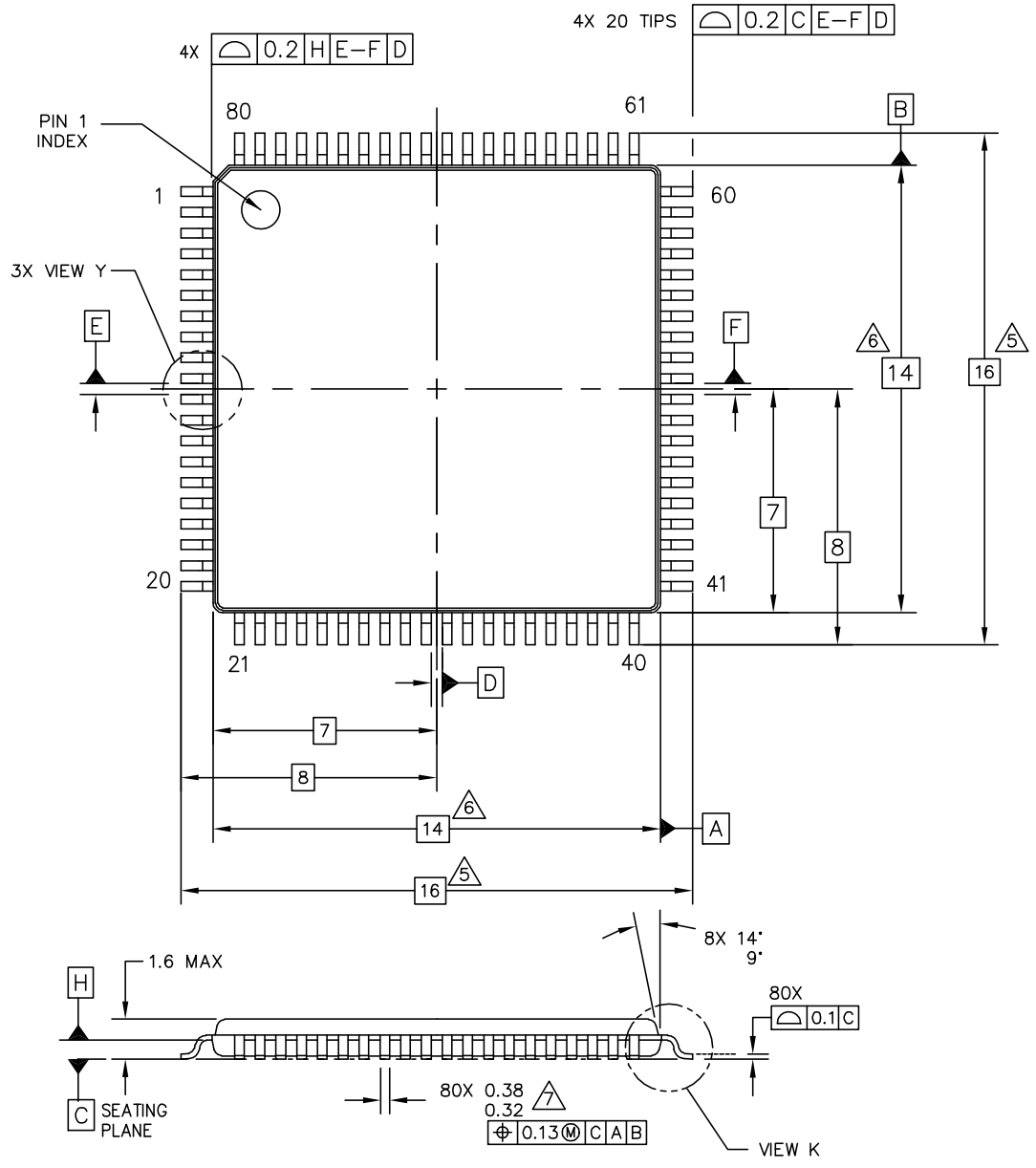
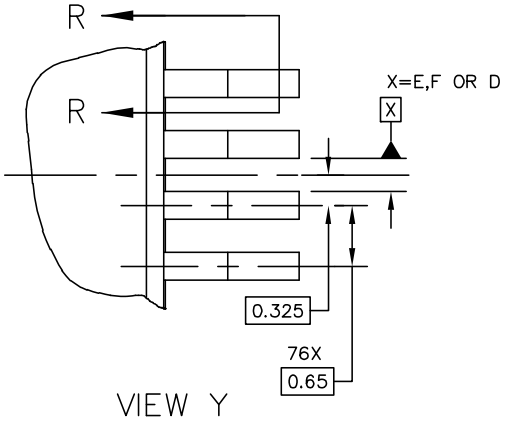


TITLE: 80 LD LQFP, 14 X 14 PKG, 0.65 MM PITCH, 1.4 THICK	CASE NUMBER: 917A–03	
	STANDARD: FREESCALE	
	PACKAGE CODE: 8258	SHEET: 1 OF 4

freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASS23237W
		PAGE: 917A
	DO NOT SCALE THIS DRAWING	REV: E



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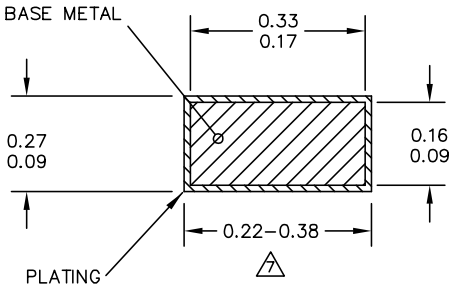
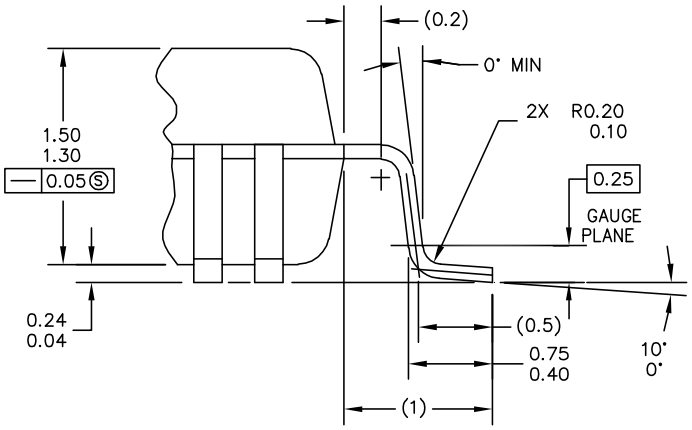


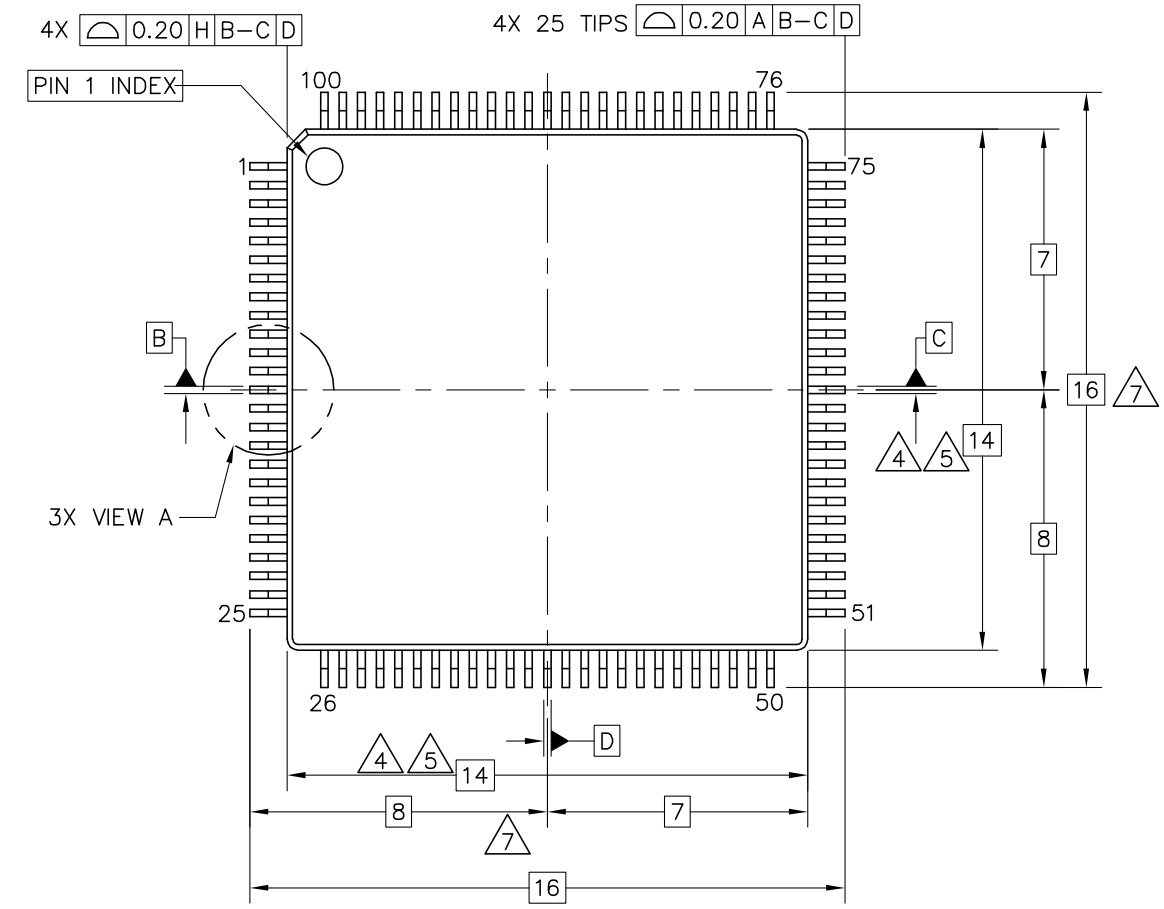
SECTION R–R
ROTATED 90° CW

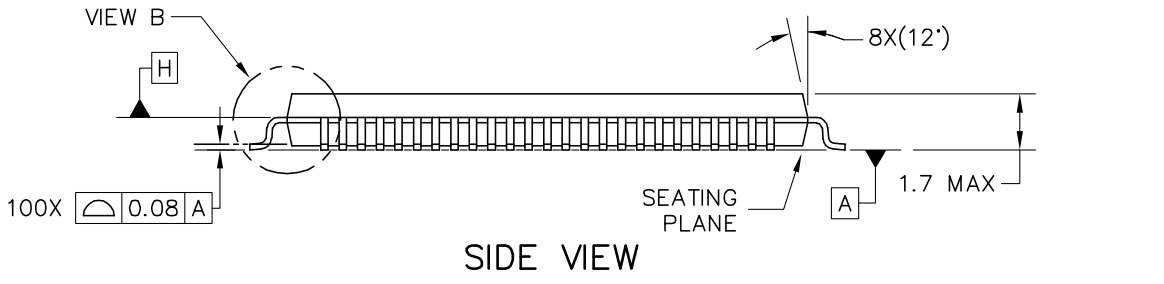


VIEW K

TITLE: 80 LD LQFP, 14 X 14 PKG, 0.65 MM PITCH, 1.4 THICK	CASE NUMBER: 917A–03	
	STANDARD: FREESCALE	
	PACKAGE CODE: 8258	SHEET: 2 OF 4

freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASS23308W
		PAGE: 983
	DO NOT SCALE THIS DRAWING	REV: H





TITLE: 100 LEAD LQFP 14 X 14, 0.5 PITCH, 1.4 THICK	CASE NUMBER: 983–02	
	STANDARD: NON–JEDEC	
	PACKAGE CODE: 8264	SHEET: 1 OF 4

freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASS23308W
		PAGE: 983
	DO NOT SCALE THIS DRAWING	REV: H

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DATUMS B, C AND D TO BE DETERMINED AT DATUM PLANE H.
4. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE SIZE BY A MAXIMUM OF 0.1 MM.
5. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSIONS. THE MAXIMUM ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THE DIMENSIONS ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
6. DIMENSION DOES NOT INCLUDE DAM BAR PROTRUSION. PROTRUSIONS SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.35. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL BE 0.07 MM.
7. DIMENSIONS ARE DETERMINED AT THE SEATING PLANE, DATUM A.

TITLE: 100 LEAD LQFP 14 X 14, 0.5 PITCH, 1.4 THICK	CASE NUMBER: 983–02	
	STANDARD: NON–JEDEC	
	PACKAGE CODE: 8264	SHEET: 3 OF 4