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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V1
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, SCI, SPI
Peripherals	LCD, LVD, PWM, WDT
Number of I/O	63
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf51em256cll

Table of Contents

Table 1. MCF51EM256 Series Features by MCU and Package (continued)

Feature	MCF51EM256	MCF51EM128
MTIM1 (8-bit)	Yes	
MTIM2 (8-bit)	Yes	
MTIM3 (16-it)	Yes	
TPM channels	2	
PDB	Yes	
XOSC1[4]	Yes	
XOSC2[5]	Yes	

1 Each differential channel is comprised of 2 pin inputs
2 RGPIO is muxed with standard Port I/O
3 Port I/O count does not include the ouput only PTC2/BKGD/MS.
4 IRTC crystal input and possible crystal input to the ICS module
5 Main external crystal input for the ICS module

1.2 Block Diagram

Figure 1 shows the connections between the MCF51EM256 series pins and modules.

front-plane/backplane pin assignments; operation in all low power modes with blink functionality

- **SCIx** — Three serial communications interface modules with optional 13-bit break; option to connect Rx input to PRACMP output on SCI1 and SCI2; high current drive on Tx on SCI1 and SCI2; wakeup from stop3 on Rx edge. SCI1 and SCI2 Tx pins can be modulated with timer outputs for use with IR interfaces
- **SPIx—** Two serial peripheral interfaces (SPI2, SPI3) with full-duplex or single-wire bidirectional; double-buffered transmit and receive; master or slave mode; MSB-first or LSB-first shifting
- **SPI16**— Serial peripheral interface (SPI1) with 32-bit FIFO buffer; 16-bit or 8-bit data transfers; full-duplex or single-wire bidirectional; double-buffered transmit and receive; master or slave mode; MSB-first or LSB-first shifting
- **IIC** — Up to 100 kbps with maximum bus loading; multi-master operation; programmable slave address; interrupt driven byte-by-byte data transfer; supports broadcast mode and 10 bit addressing
- **MTIMx** — Two 8-bit and one 16-bit modulo timers with 4-bit prescaler; overflow interrupt; external clock input/pulse accumulator
- **TPM** — 2-channel Timer/PWM module; selectable input capture, output compare, or buffered edge- or center-aligned PWM on each channel; external clock input/pulse accumulator; can be used modulate SCI1 and SCI2 TX pins

- Input/output
  - up to 16 rapid GPIO and 48 standard GPIOs, including 1 output-only pin and 3 open-drain pins.
  - up to 16 keyboard interrupts with selectable polarity
  - Hysteresis and configurable pullup device on all input pins; configurable slew rate and drive strength on all output pins
- Package options
  - 100-pin LQFP, 80-pin LQFP

1.4 Part Numbers

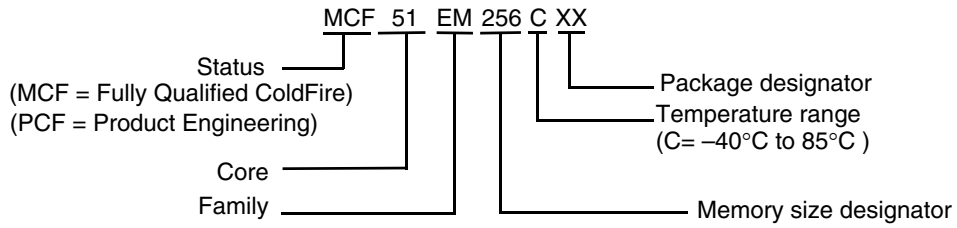


Table 3. Orderable Part Number Summary

Freescale Part Number	Flash / SRAM (KB)	Package	Temperature
MCF51EM256CLL	256/16	100-Pin LQFP	–40°C to 85°C
MCF51EM256CLK	256/16	80-Pin LQFP	–40°C to 85°C
MCF51EM128CLL	128/16	100-Pin LQFP	–40°C to 85°C
MCF51EM128CLK	128/16	80-Pin LQFP	–40°C to 85°C

1.5 Pinouts and Packaging

1.5.1 Pinout: 80-Pin LQFP

Pins not available on the 80-pin LQFP are automatically disabled for reduced current consumption. No user interaction is needed. Software access to the functions on these pins will be ignored

Figure 2 shows the pinout of the 80-pin LQFP.

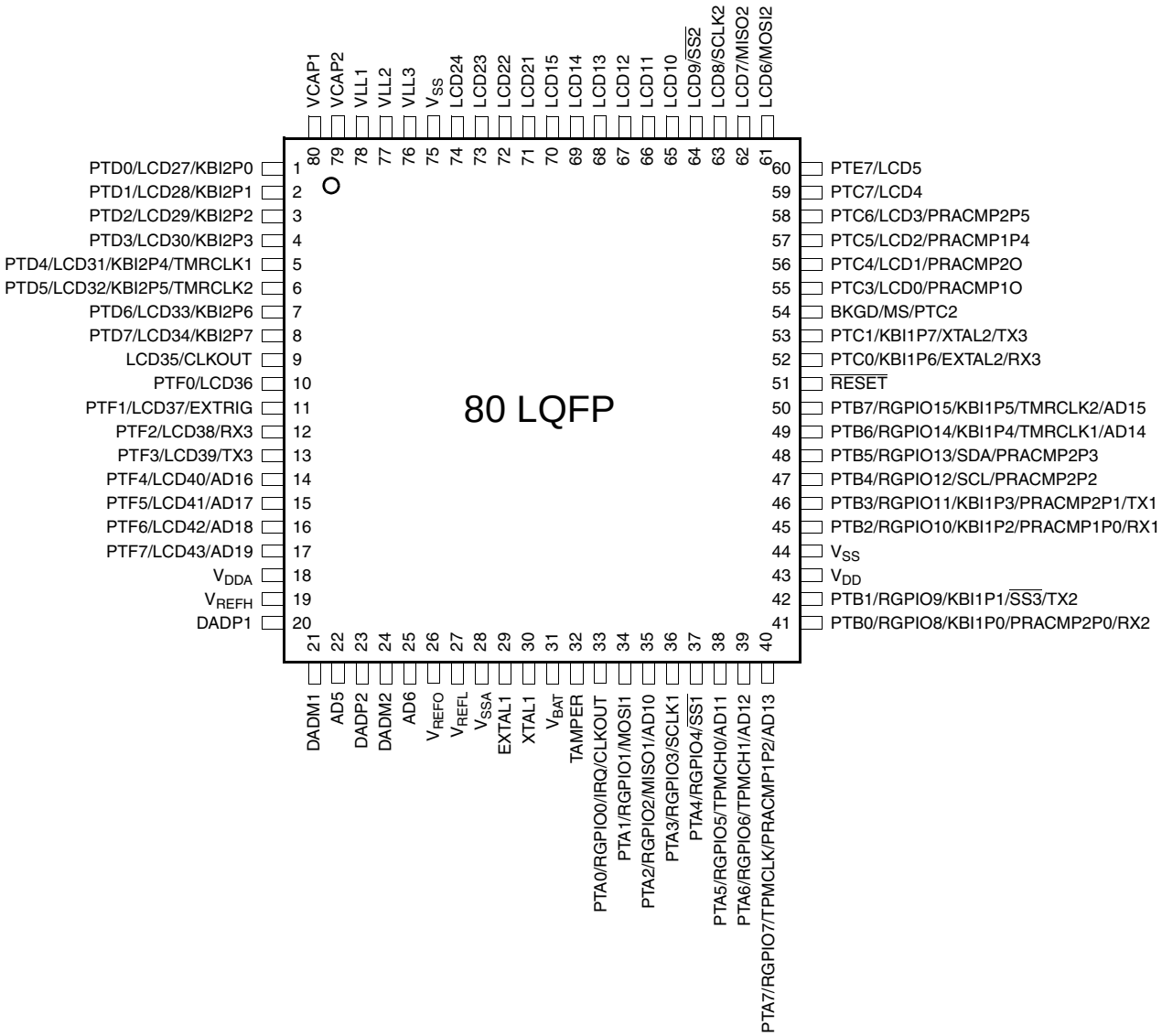


Figure 2. 80-Pin LQFP Pinout

1.5.2 Pinout: 100-Pin LQFP

Figure 3 shows the pinout configuration for the 100-pin LQFP. Pins which are blacked out do not have an equivalent pin on the 80-pin LQFP package.

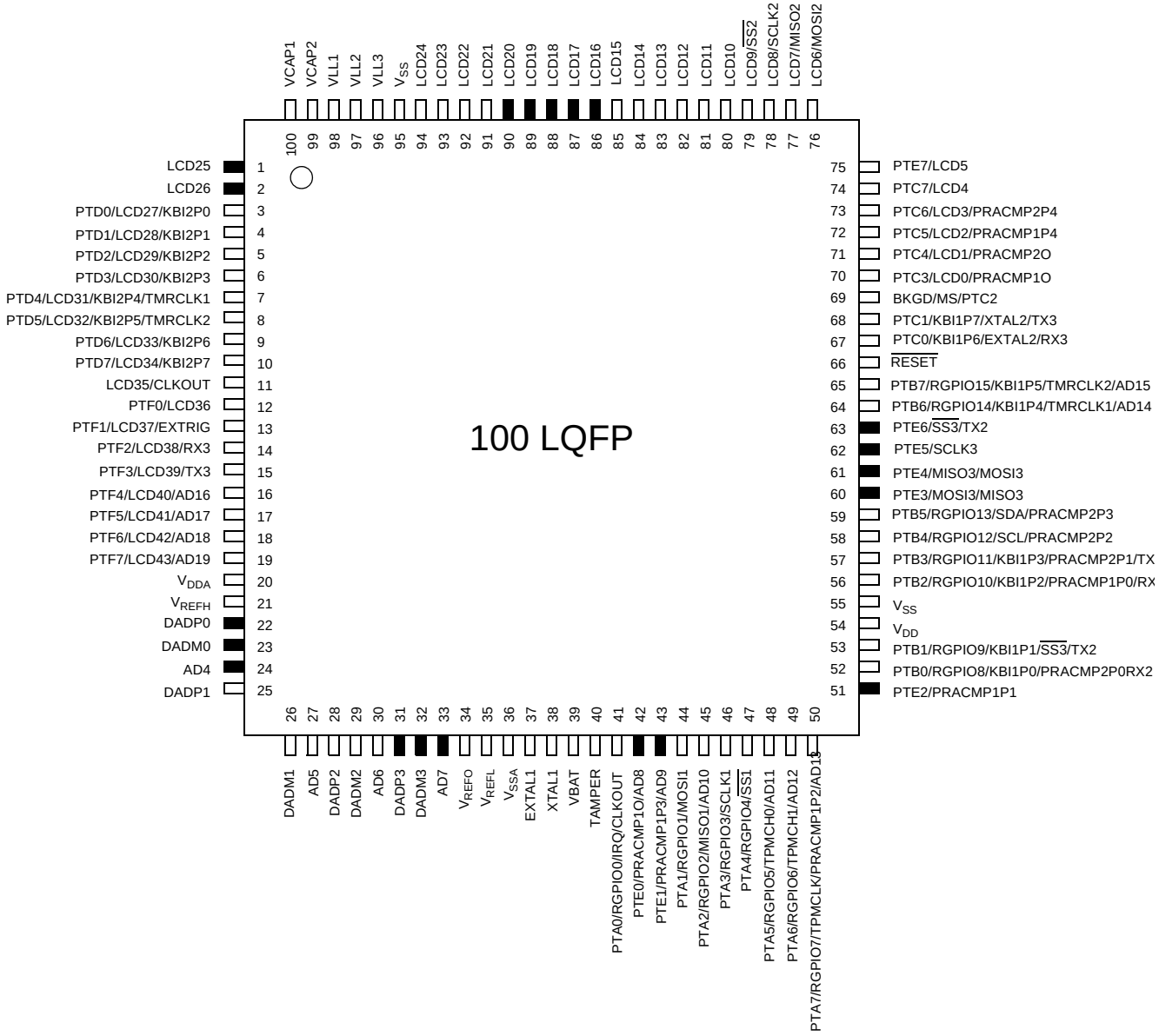


Figure 3. 100-Pin LQFP Pinout

Table 4 shows the package pin assignments.

Table 4. MCF51EM256 Series Package Pin Assignments (continued)

100 LQFP	80 LQFP	Default Function	ALT1	ALT2	ALT3	Comment
87	—	LCD17				
88	—	LCD18				
89	—	LCD19				
90	—	LCD20				
91	71	LCD21				
92	72	LCD22				
93	73	LCD23				
94	74	LCD24				
95	75	V_{SS}				
96	76	VLL3				
97	77	VLL2				
98	78	VLL1				
99	79	VCAP2				
100	80	VCAP1				

[1] These pins that are shared with the LCD are open-drain by default if not used as LCD pins. To configure this pins as full complementary drive outputs, you must have the LCD modules bits configured as follow: FCDEN =1, VSUPPLY = 11 and RVEN = 0. The Input levels and internal pullup resistors are referenced to VLL3. Referer to the LCD chapter for further information.

2 Electrical Characteristics

This section contains electrical specification tables and reference timing diagrams for the MCF51EM256/128 series microcontrollers, including detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications.

The electrical specifications are preliminary and are from previous designs or design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. These specifications will, however, be met for production silicon. Finalized specifications will be published after complete characterization and device qualifications have been completed.

NOTE

The parameters specified in this data sheet supersede any values found in the module specifications.

2.1 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 10. DC Characteristics (continued)

Num	C	Parameter		Symbol	Min	Typical[1]	Max	Unit
22	C	Low-voltage detection threshold	Low range — V_{DD} falling	V_{LVDL}	1.800	1.845	1.890	V
			Low range — V_{DD} rising		1.870	1.915	1.960	V
23	P	Low-voltage warning threshold	V_{DD} falling, LVWV = 1	V_{LVWH}	2.590	2.655	2.720	V
			V_{DD} rising, LVWV = 1		2.580	2.645	2.710	
24	C	Low-voltage warning	V_{DD} falling, LVWV = 0	V_{LVWL}	2.300	2.355	2.410	V
			V_{DD} rising, LVWV = 0		2.360	2.425	2.490	
25	D	RAM retention voltage		V_{RAM}	—	0.6	1.0	V
26	D	DC injection current[7 8 9 10] (single pin limit), $V_{IN} > V_{DD}$, $V_{IN} < V_{SS}$		I_{IC}	–0.2	—	0.2	mA
		DC injection current (Total MCU limit, includes sum of all stressed pins), $V_{IN} > V_{DD}$, $V_{IN} < V_{SS}$			–5	—	5	mA

1 Typical values are based on characterization data at 25 °C unless otherwise stated.

2 Switch to lower frequency when the low-voltage interrupt asserts (V_{LVDH}).

3 Factory trimmed at V_{DD} = 3.0 V, Temp = 25°C

4 Measured with $V_{In} = V_{DD}$ or V_{SS}.

5 Measured with $V_{In} = V_{SS}$.

6 Measured with $V_{In} = V_{DD}$.

7 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

8 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

9 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

10 The $\overline{\text{RESET}}$ pin does not have a clamp diode to V_{DD}. Do not drive this pin above V_{DD}.

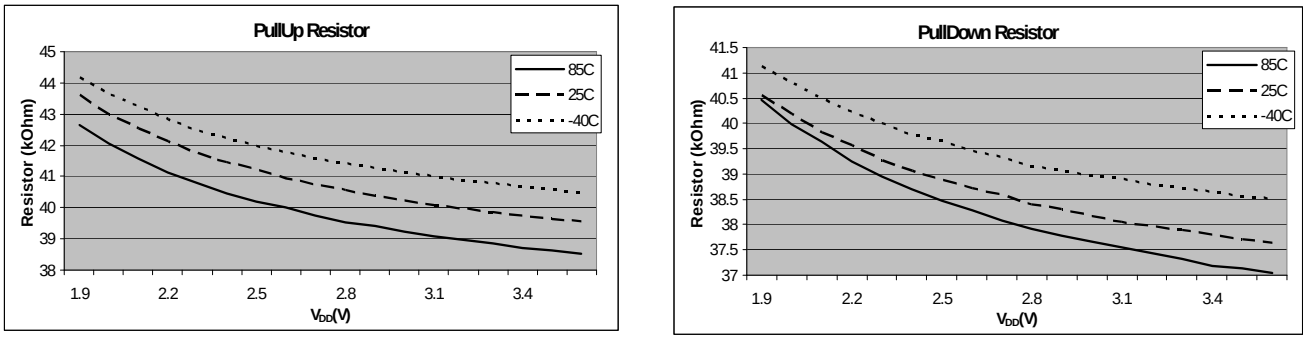


Figure 4. Pullup and Pulldown Typical Resistor Values

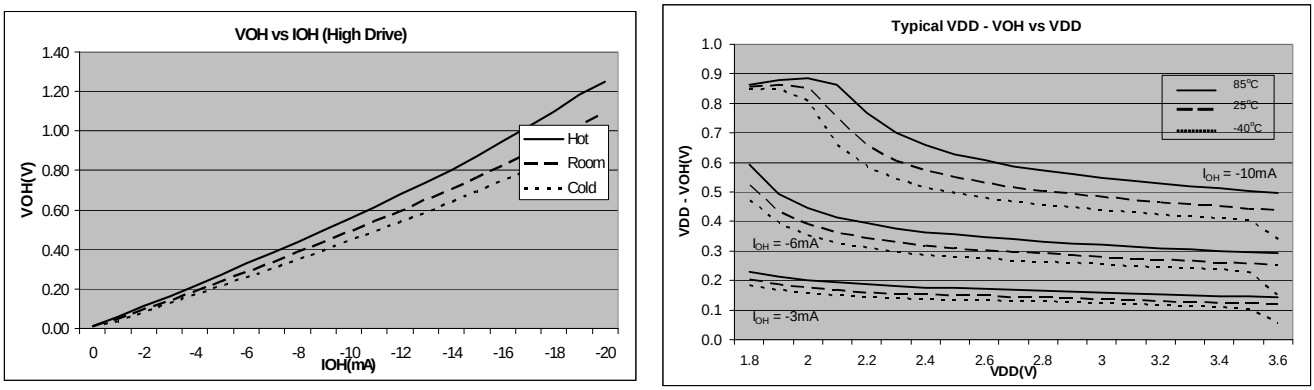


Figure 8. Typical High-Side (Source) Characteristics — High Drive (PTxDSn = 1)

2.6 Supply Current Characteristics

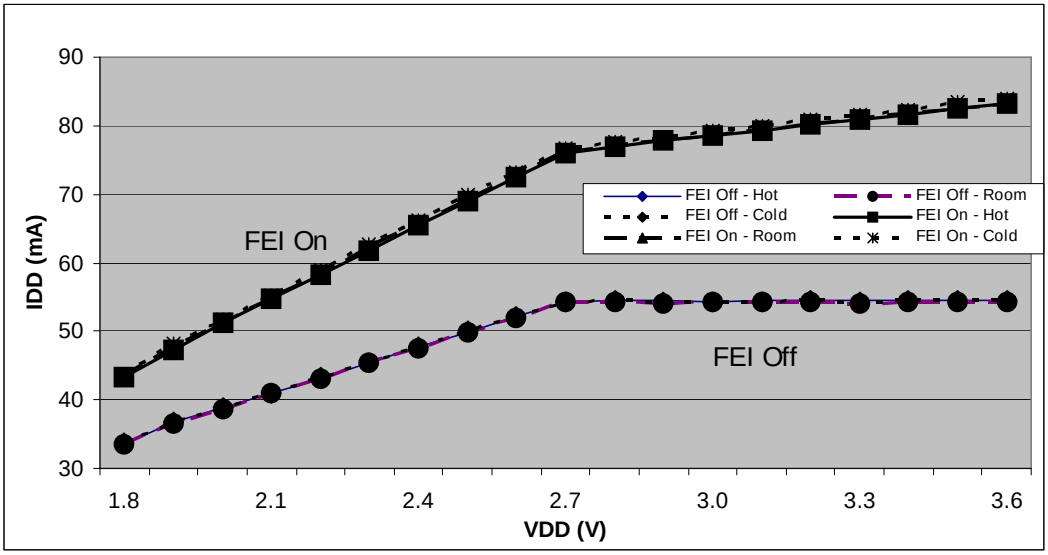


Figure 9. Typical Run I_{DD} for FBE and FEI, I_{DD} vs. V_{DD} (All Modules Enabled)

Table 11. Supply Current Characteristics (continued)

Num	C	Parameter	Symbol	V_{DD} (V)	Typical[1]	Max	Unit	Temp (°C)
14	P	IRTC supply current[3,4,5]	I_{DD-BAT}		1.5	5	µA	–40 to 85°C

1 Typicals are measured at 25 °C.

2 Values given under the following conditions: low range operation (RANGE = 0), low power mode (HGO = 0).

3 This is the current consumed when the IRTC is being powered by the V_{BAT}.

4 The IRTC power source depends on the MCU configuration and V_{DD} voltage level. Refer to reference manual for further information.

5 The IRTC current consumption includes the IRTC XOSC1.

2.7 Analog Comparator (PRACMP) Electricals

Table 12. PRACMP Electrical Specifications

N	C	Characteristic	Symbol	Min	Typical	Max	Unit
1	—	Supply voltage	V_{PWR}	1.8	—	3.6	V
2	C	Supply current (active) (PRG enabled)	I_{DDACT1}	—	—	60	µA
3	C	Supply current (active) (PRG disabled)	I_{DDACT2}	—	—	40	µA
4	D	Supply current (ACMP and PRG all disabled)	I_{DDDIS}	—	—	2	nA
5	—	Analog input voltage	VAIN	V_{SS} – 0.3	—	V_{DD}	V
6	T	Analog input offset voltage	VAIO	—	5	40	mV
7	T	Analog comparator hysteresis	V_H	3.0	—	20.0	mV
8	D	Analog input leakage current	I_{ALKG}	—	—	1	nA
9	T	Analog comparator initialization delay	t_{AINIT}	—	—	1.0	µs
10	—	Programmable reference generator input1	$V_{In1}(V_{DD})$	—	V_{DD}	—	V
11	T	Programmable reference generator input2	$V_{In2}(V_{DD25})$	1.8	—	2.75	V
12	D	Programmable reference generator setup delay	t_{PRGST}	—	1	—	µs
13	D	Programmable reference generator step size	Vstep	–0.25	0	0.25	LSB
14	P	Programmable reference generator voltage range	V_{prgout}	$V_{In}/32$	—	V_{in}	V

2.8 ADC Characteristics

These specs all assume seperate V_{DDAD} supply for ADC and isolated pad segment for ADC supplies and differential inputs. Spec's should be de-rated for $V_{REFH} = V_{bg}$ condition.

Table 13. 16-bit ADC Operating Conditions

Num	Charact eristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
1	Supply voltage	Absolute	V_{DDA}	1.8	—	3.6	V	
2		Delta to V_{DD} (V_{DD}–V_{DDA})[2]	ΔV_{DDA}	–100	0	100	mV	
3	Ground voltage	Delta to V_{SS} (V_{SS}–V_{SSA})[2]	ΔV_{SSA}	–100	0	100	mV	
4	Ref Voltage High		V_{REFH}	1.15	V_{DDA}	V_{DDA}	V	

Table 14. 16-bit ADC Characteristics full operating range($V_{REFH} = V_{DDAD} > 1.8$, $V_{REFL} = V_{SSAD}$, $F_{ADCK} \leq 8MHz$)

Characteristic	Conditions[1]	C	Symb	Min	Typ[2]	Max	Unit	Comment
Full-Scale Error	16-bit differential mode 16-bit single-ended mode	T	E_{FS}	— —	+10/0 +14/0	+42/-2 +46/-2	LSB[2]	$V_{ADIN} = V_{DDAD}$
	13-bit differential mode 12-bit single-ended mode	T		— —	±1.0 ±1.0	±3.5 ±3.5		
	11-bit differential mode 10-bit single-ended mode	T		— —	±0.4 ±0.4	±1.5 ±1.5		
	9-bit differential mode 8-bit single-ended mode	T		— —	±0.2 ±0.2	±0.5 ±0.5		
Quantization Error	16 bit modes	D	E_Q	—	-1 to 0	—	LSB[2]	
	≤13 bit modes			—	—	±0.5		
Effective Number of Bits	16 bit differential mode Avg=32 Avg=16 Avg=8 Avg=4 Avg=1	C	ENOB	 12.8 12.7 12.6 12.5 11.9	 14.2 13.8 13.6 13.3 12.5	 — — — — —	Bits	$F_{in} = F_{sample}/100$
	16 bit single-ended mode Avg=32 Avg=16 Avg=8 Avg=4 Avg=1	C		 — — — — —	 TBD TBD TBD TBD TBD	 — — — — —		
Signal to Noise plus Distortion	See ENOB		SINAD	$SINAD = 6.02 \cdot ENOB + 1.76$			dB	
Total Harmonic Distortion	16-bit differential mode Avg = 32	C	THD	—	-91.5	-74.3	dB	$F_{in} = F_{sample}/100$
	16-bit single-ended mode Avg = 32	D		—	-85.5	—		
Spurious Free Dynamic Range	16-bit differential mode Avg = 32	C	SFDR	75.0	92.2	—	dB	$F_{in} = F_{sample}/100$
	16-bit single-ended mode Avg = 32	D		—	86.2	—		
Input Leakage Error	all modes	D	E_{IL}	$I_{In} * R_{AS}$			mV	I_{In} = leakage current (refer to DC characteristics)
Temp Sensor Slope	-40°C– 25°C	C	m	—	1.646	—	mV/°C	
	25°C– 125°C			—	1.769	—		
Temp Sensor Voltage	25°C	C	V_{TEMP25}	—	701.2	—	mV	

2.13 VREF Characteristics

Table 21. VREF Electrical Specifications

Num	C	Characteristic	Symbol	Min	Typical	Max	Unit
1	—	Supply voltage	V_{DDAD}	1.80	—	3.60	V
2	—	Operating temperature range	T_{op}	–40	—	105	°C
3	D	Load capability	I_{load}	—	—	10	mA
4	C P	Voltage reference output untrimmed factory trimmed	V_{REFO}	 1.070 1.04	 — 1.150	 1.202 1.17	 V V
5	D	Load regulation mode = 10, I_{load} = 1 mA		20	—	100	µV/mA
6	T	Line regulation (power supply rejection) DC AC		±0.1 from room temp voltage –60			 mV dB
7	T	Bandgap only (mode = 00)	I_{BG}	—	72	—	µA
8	C	Low power mode (mode = 01)	I_{LP}	—	90	125	µA
9	T	Tight regulation mode (mode =10)	I_{TR}	—	0.27	—	mA

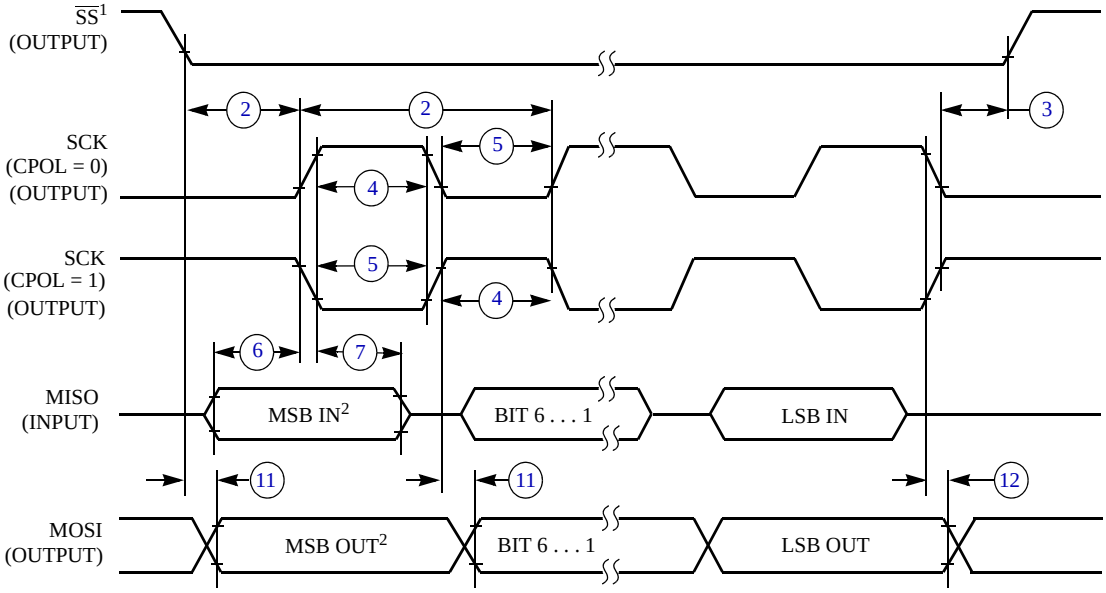
2.14 SPI Characteristics

Table 22 and Figure 19 through Figure 22 describe the timing requirements for the SPI system.

4 All timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless noted; 100 pF load on all SPI pins. All timing assumes slew rate control disabled and high drive strength enabled for SPI output pins.

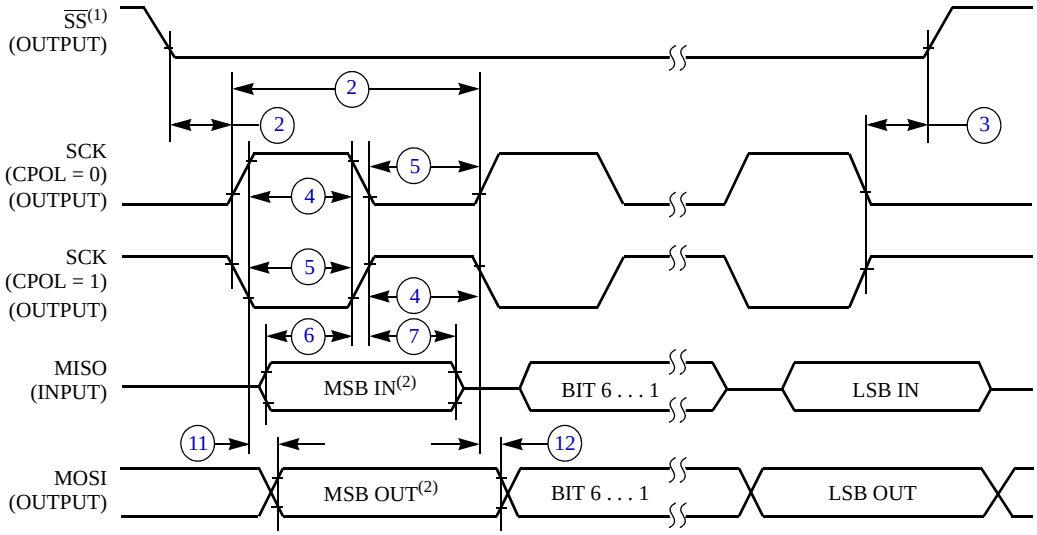
5 Time to data active from high-impedance state.

6 Hold time to high-impedance state.



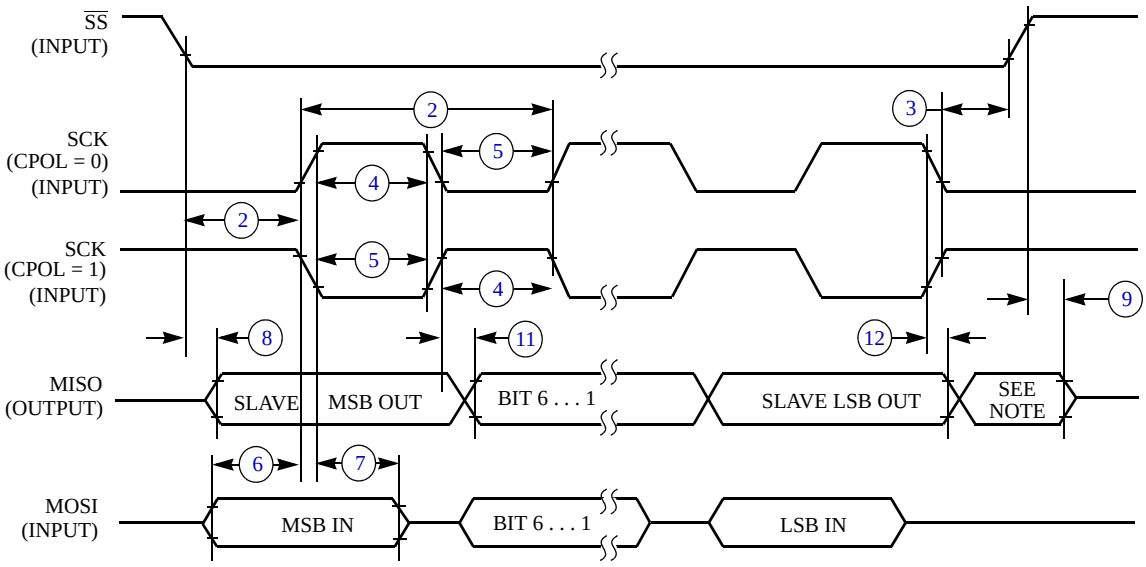
NOTES:
1. $\overline{SS}$ output mode (MODFEN = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 19. SPI Master Timing (CPHA = 0)



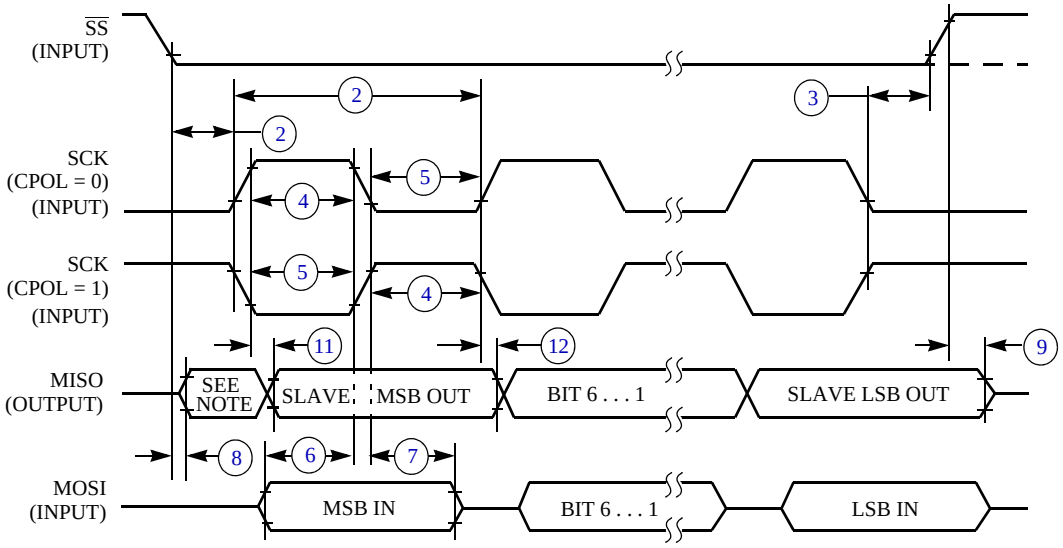
NOTES:
1. $\overline{SS}$ output mode (MODFEN = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 20. SPI Master Timing (CPHA = 1)



NOTE:
1. Not defined but normally MSB of character just received

Figure 21. SPI Slave Timing (CPHA = 0)



NOTE:
1. Not defined but normally LSB of character just received

Figure 22. SPI Slave Timing (CPHA = 1)

2.15 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory section of the *MCF51EM256 Series ColdFire Microcontroller Reference Manual*.

Table 23. Flash Characteristics

N	C	Characteristic	Symbol	Min	Typical	Max	Unit
1	D	Supply voltage for program/erase –40 °C to 85 °C	$V_{prog/erase}$	1.8		3.6	V
2	D	Supply voltage for read operation	V_{Read}	1.8		3.6	V
3	D	Internal FCLK frequency[1]	f_{FCLK}	150		200	kHz
4	D	Internal FCLK period ($1/f_{FCLK}$)	t_{Fcyc}	5		6.67	µs
5	P	Longword program time (random location)[2]	t_{prog}	9			t_{Fcyc}
6	P	Longword program time (burst mode)[2]	t_{Burst}	4			t_{Fcyc}
7	P	Page erase time[2]	t_{Page}	4000			t_{Fcyc}
8	P	Mass erase time[2]	t_{Mass}	20,000			t_{Fcyc}
9		Longword program current[3]	R_{IDDBP}	—	9.7	—	mA
10		Page erase current[3]	R_{IDDPE}	—	7.6	—	mA
11	C	Program/erase endurance[4] T_L to T_H = –40 °C to 85 °C T = 25 °C		10,000 —	— 100,000	— —	cycles
12	C	Data retention[5]	t_{D_ret}	15	100	—	years

1 The frequency of this clock is controlled by a software setting.

2 These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

3 The program and erase currents are additional to the standard run I_{DD}. These values are measured at room temperatures with V_{DD} = 3.0 V, bus frequency = 4.0 MHz.

4 **Typical endurance for flash** was evaluated for this product family on the HC9S12Dx64. For additional information on how Freescale defines typical endurance, please refer to Engineering Bulletin EB619, *Typical Endurance for Nonvolatile Memory.*

5 **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale defines typical data retention, please refer to Engineering Bulletin EB618, *Typical Data Retention for Nonvolatile Memory.*

2.16 EMC Performance

Electromagnetic compatibility (EMC) performance is highly dependant on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

2.16.1 Radiated Emissions

Microcontroller radiated RF emissions are measured from 150 kHz to 1 GHz using the TEM/GTEM Cell method in accordance with the IEC 61967-2 and SAE J1752/3 standards. The measurement is performed with the microcontroller installed on a custom EMC evaluation board while running specialized EMC test software. The radiated emissions from the microcontroller are measured in a TEM cell in two package orientations (North and East). For more detailed information concerning the evaluation results, conditions and setup, please refer to the EMC Evaluation Report for this device.

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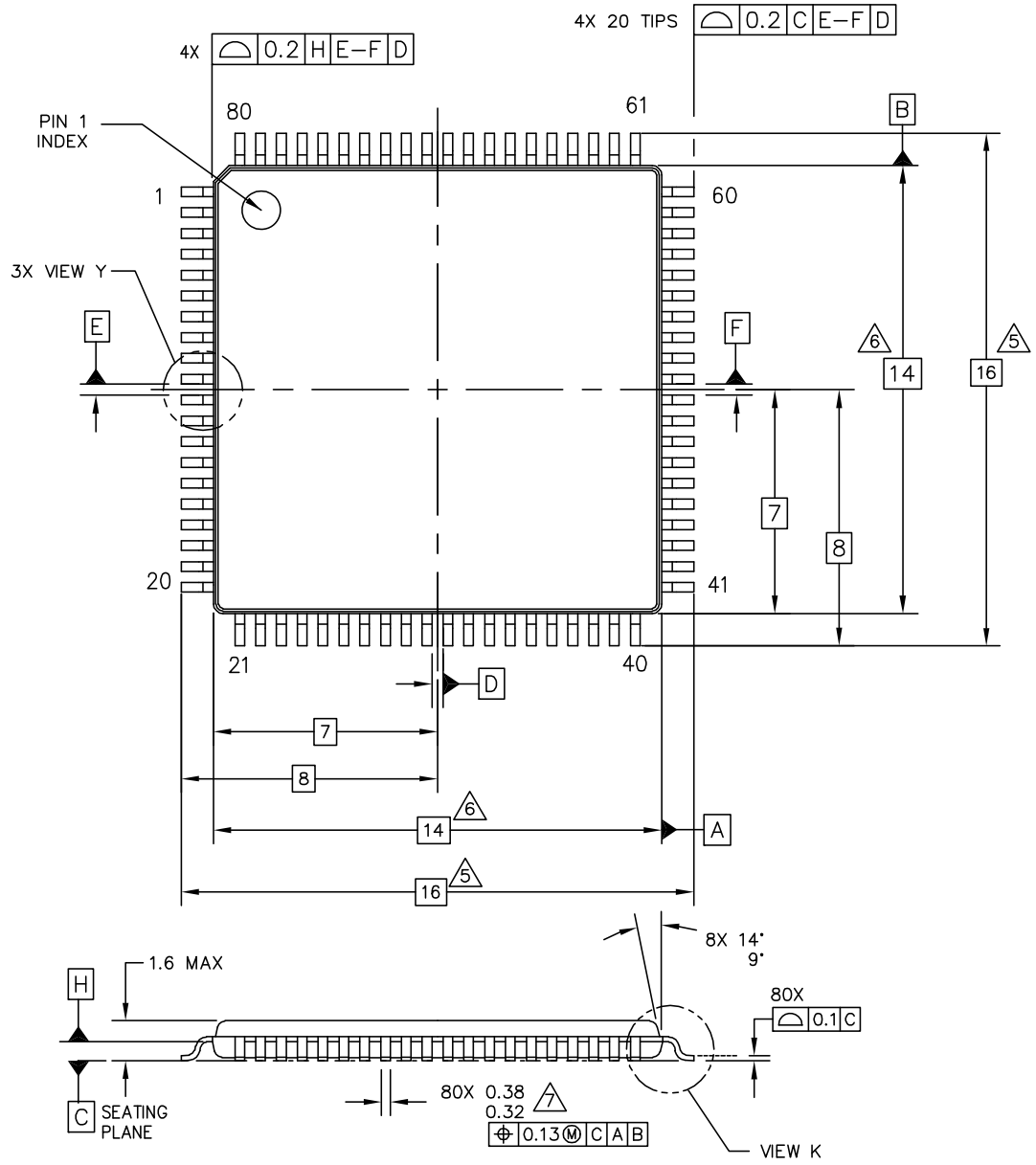

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	STANDARD: FREESCALE	
	PACKAGE CODE: 8258	SHEET: 1 OF 4

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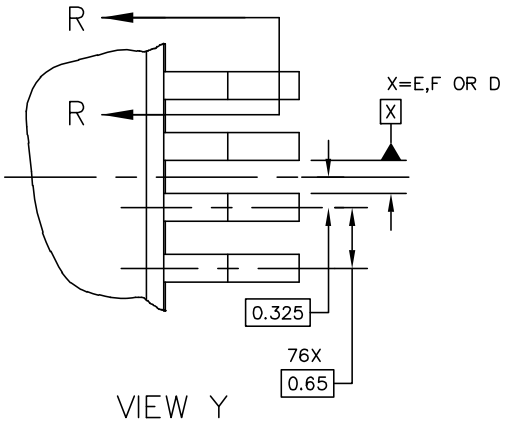

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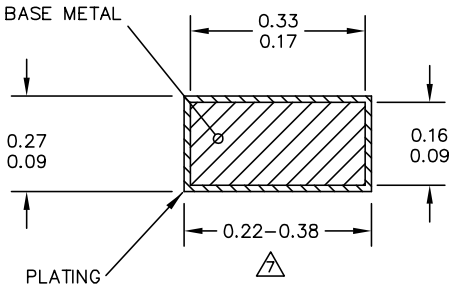

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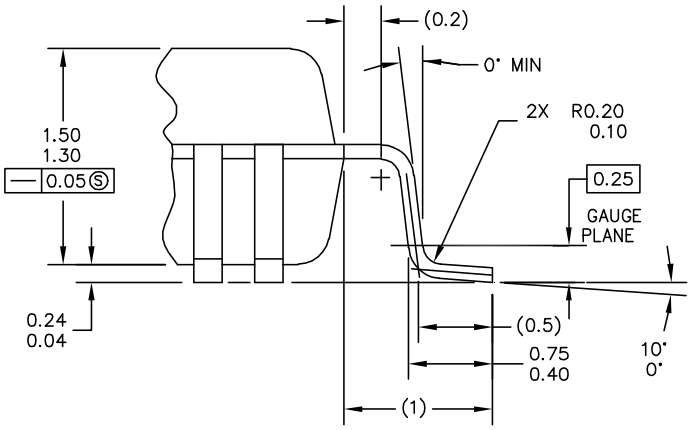
ROTATED 90° CW



VIEW K

TITLE: 80 LD LQFP, 14 X 14 PKG, 0.65 MM PITCH, 1.4 THICK	CASE NUMBER: 917A–03	
	STANDARD: FREESCALE	
	PACKAGE CODE: 8258	SHEET: 2 OF 4

freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASS23237W
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	DO NOT SCALE THIS DRAWING	REV: E

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION : MILIMETER.
3. DATUM PLANE H IS LOCATED AT THE BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUM E, F AND D TO BE DETERMINED AT DATUM PLANE H.
5. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
7. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07.

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4 Revision History

Table 24. Revision History

Revision	Date	Description
1	10/15/2009	Initial public release.
2	4/29/2010	Updated teh descriptions of SPI in the Table 2. Changed the FSPIx to SPI16 to keep the term in accordance. Updated Figure 4 to Figure 8. Updated WI_{DD}, $S2I_{DD}$, $S3I_{DD}$ in the Table 11. Updated the ADC characteristics in the Table 13 to Table 15. Updated description of XOSC in the Section 2.9, “External Oscillator (XOSC) Characteristics.” Updated t_{CSTL} in the Table 16. Updated the the classification of IBG and ITR to T and added Voltage reference output (factory trimmed) in the Table 21. Update SPI data in the Table 22.
3	8/9/2010	Updated the V_{DD} at 20 MHz maximum operation to 3.6 V. Updated the RI_{DD} (at Run supply current FEI mode, all module on), $S2I_{DD}$ and $S3I_{DD}$ at 3 V, $S3I_{DDLVD}$ in the Table 11. Updated ENOB at 16 bit single-ended mode in the Table 14.