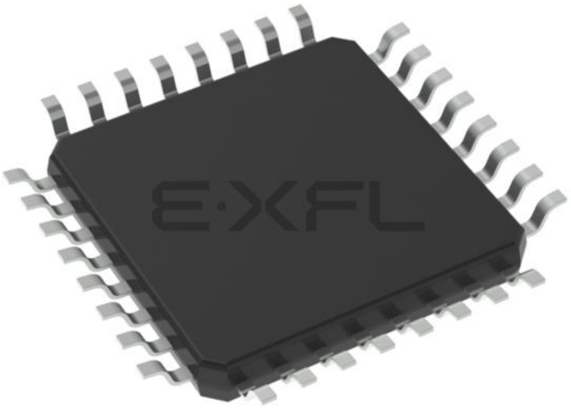
Microchip Technology - ATSAMD20E14A-AUT Datasheet



Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	26
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 10x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-TQFP
Supplier Device Package	32-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamd20e14a-aut

Table of Contents

1. Description

The Atmel® | SMART™ SAM D20 is a series of low-power microcontrollers using the 32-bit ARM® Cortex®-M0+ processor, and ranging from 32- to 64-pins with up to 256KB Flash and 32KB of SRAM. The SAM D20 devices operate at a maximum frequency of 48MHz and reach 2.46 CoreMark/MHz. They are designed for simple and intuitive migration with identical peripheral modules, hex compatible code, identical linear address map and pin compatible migration paths between all devices in the product series. All devices include intelligent and flexible peripherals, Atmel Event System for inter-peripheral signaling, and support for capacitive touch button, slider and wheel user interfaces.

The SAM D20 devices provide the following features: In-system programmable Flash, eight-channel Event System, programmable interrupt controller, up to 52 programmable I/O pins, 32-bit real-time clock and calendar, up to eight 16-bit Timer/Counters (TC) . The timer/counters can be configured to perform frequency and waveform generation, accurate program execution timing or input capture with time and frequency measurement of digital signals. The TCs can operate in 8- or 16-bit mode, selected TCs can be cascaded to form a 32-bit TC. The series provide up to six Serial Communication Modules (SERCOM) that each can be configured to act as an USART, UART, SPI, I^2C up to 400kHz, up to twenty-channel 350ksps 12-bit ADC with programmable gain and optional oversampling and decimation supporting up to 16-bit resolution, one 10-bit 350ksps DAC, two analog comparators with window mode, Peripheral Touch Controller supporting up to 256 buttons, sliders, wheels and proximity sensing; programmable Watchdog Timer, brown-out detector and power-on reset and two-pin Serial Wire Debug (SWD) program and debug interface.

All devices have accurate and low-power external and internal oscillators. All oscillators can be used as a source for the system clock. Different clock domains can be independently configured to run at different frequencies, enabling power saving by running each peripheral at its optimal clock frequency, and thus maintaining a high CPU frequency while reducing power consumption.

The SAM D20 devices have two software-selectable sleep modes, idle and standby. In idle mode the CPU is stopped while all other functions can be kept running. In standby all clocks and functions are stopped expect those selected to continue running. The device supports SleepWalking. This feature allows the peripheral to wake up from sleep based on predefined conditions, and thus allows the CPU to wake up only when needed, e.g. when a threshold is crossed or a result is ready. The Event System supports synchronous and asynchronous events, allowing peripherals to receive, react to and send events even in standby mode.

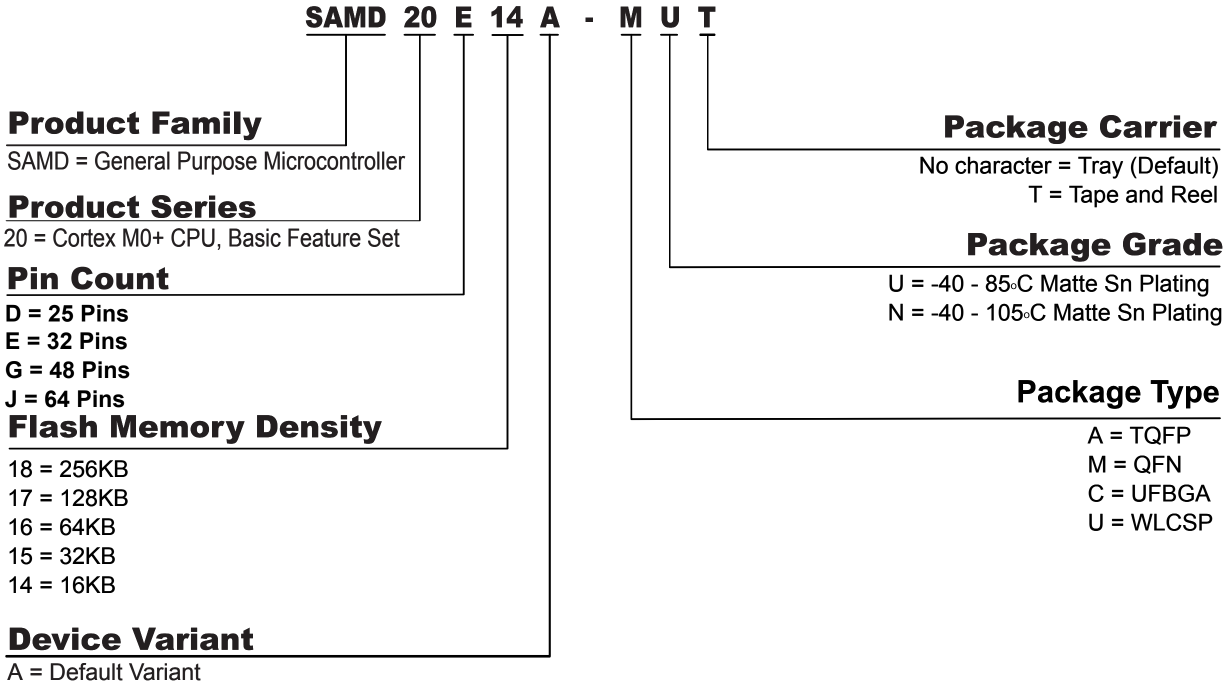
The Flash program memory can be reprogrammed in-system through the SWD interface. The same interface can be used for non-intrusive on-chip debug of application code. A boot loader running in the device can use any communication interface to download and upgrade the application program in the Flash memory.

The SAM D20 devices are supported with a full suite of program and system development tools, including C compilers, macro assemblers, program debugger/simulators, programmers and evaluation kits.

2. Configuration Summary

	SAM D20J	SAM D20G	SAM D20E
Pins	64	48	32
General Purpose I/O-pins (GPIOs)	52	38	26
Flash	256/128/64/32KB	256/128/64/32KB	256/128/64/32KB
SRAM	32/16/8/4/2KB	32/16/8/4/2KB	32/16/8/4/2KB
Timer Counter (TC) instances	8	6	6
Waveform output channels per TC instance	2	2	2
Serial Communication Interface (SERCOM) instances	6	6	4
Analog-to-Digital Converter (ADC) channels	20	14	10
Analog Comparators (AC)	2	2	2
Digital-to-Analog Converter (DAC) channels	1	1	1
Real-Time Counter (RTC)	Yes	Yes	Yes
RTC alarms	1	1	1
RTC compare values	One 32-bit value or two 16-bit values	One 32-bit value or two 16-bit values	One 32-bit value or two 16-bit values
External Interrupt lines	16	16	16
Peripheral Touch Controller (PTC) X and Y lines	16x16	12x10	10x6
Maximum CPU frequency	48MHz		
Packages	QFN TQFP UFBGA	QFN TQFP WLCSP	QFN TQFP
Oscillators	32.768kHz crystal oscillator (XOSC32K) 0.4-32MHz crystal oscillator (XOSC) 32.768kHz internal oscillator (OSC32K) 32KHz ultra-low-power internal oscillator (OSCULP32K) 8MHz high-accuracy internal oscillator (OSC8M) 48MHz Digital Frequency Locked Loop (DFLL48M)		
Event System channels	8	8	8
SW Debug Interface	Yes	Yes	Yes
Watchdog Timer (WDT)	Yes	Yes	Yes

3. Ordering Information



SAMD 20 E 14 A - M U T

Product Family
SAMD = General Purpose Microcontroller

Product Series
20 = Cortex M0+ CPU, Basic Feature Set

Pin Count
D = 25 Pins
E = 32 Pins
G = 48 Pins
J = 64 Pins

Flash Memory Density
18 = 256KB
17 = 128KB
16 = 64KB
15 = 32KB
14 = 16KB

Device Variant
A = Default Variant

Package Carrier
No character = Tray (Default)
T = Tape and Reel

Package Grade
U = -40 - 85°C Matte Sn Plating
N = -40 - 105°C Matte Sn Plating

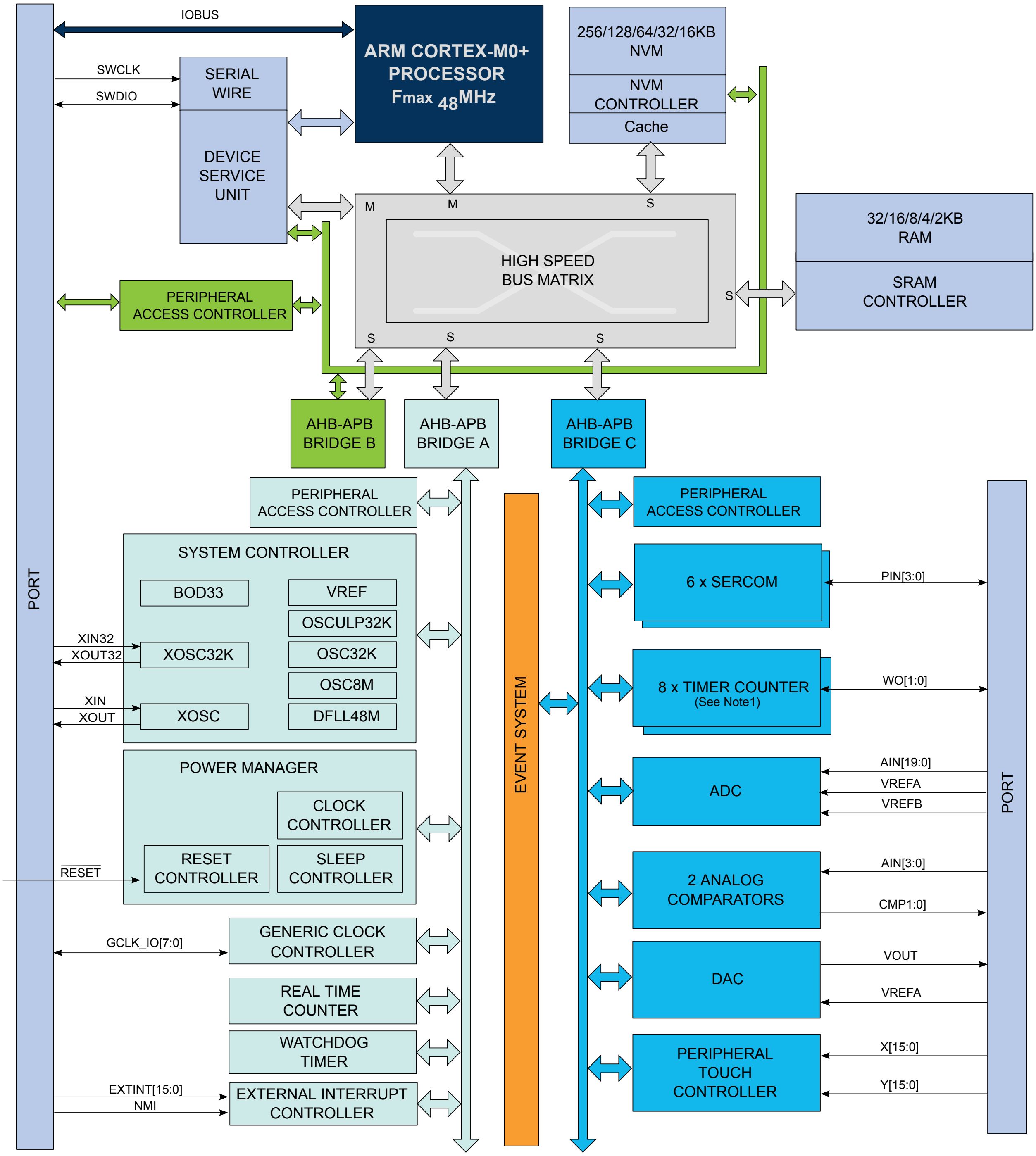
Package Type
A = TQFP
M = QFN
C = UFBGA
U = WLCSP

3.1. SAM D20E

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAMD20E14A-AU	16K	2K	TQFP32	Tray
ATSAMD20E14A-AUT				Tape & Reel
ATSAMD20E14A-AN				Tray
ATSAMD20E14A-ANT				Tape & Reel
ATSAMD20E14A-MU			QFN32	Tray
ATSAMD20E14A-MUT				Tape & Reel
ATSAMD20E14A-MN				Tray
ATSAMD20E14A-MNT				Tape & Reel

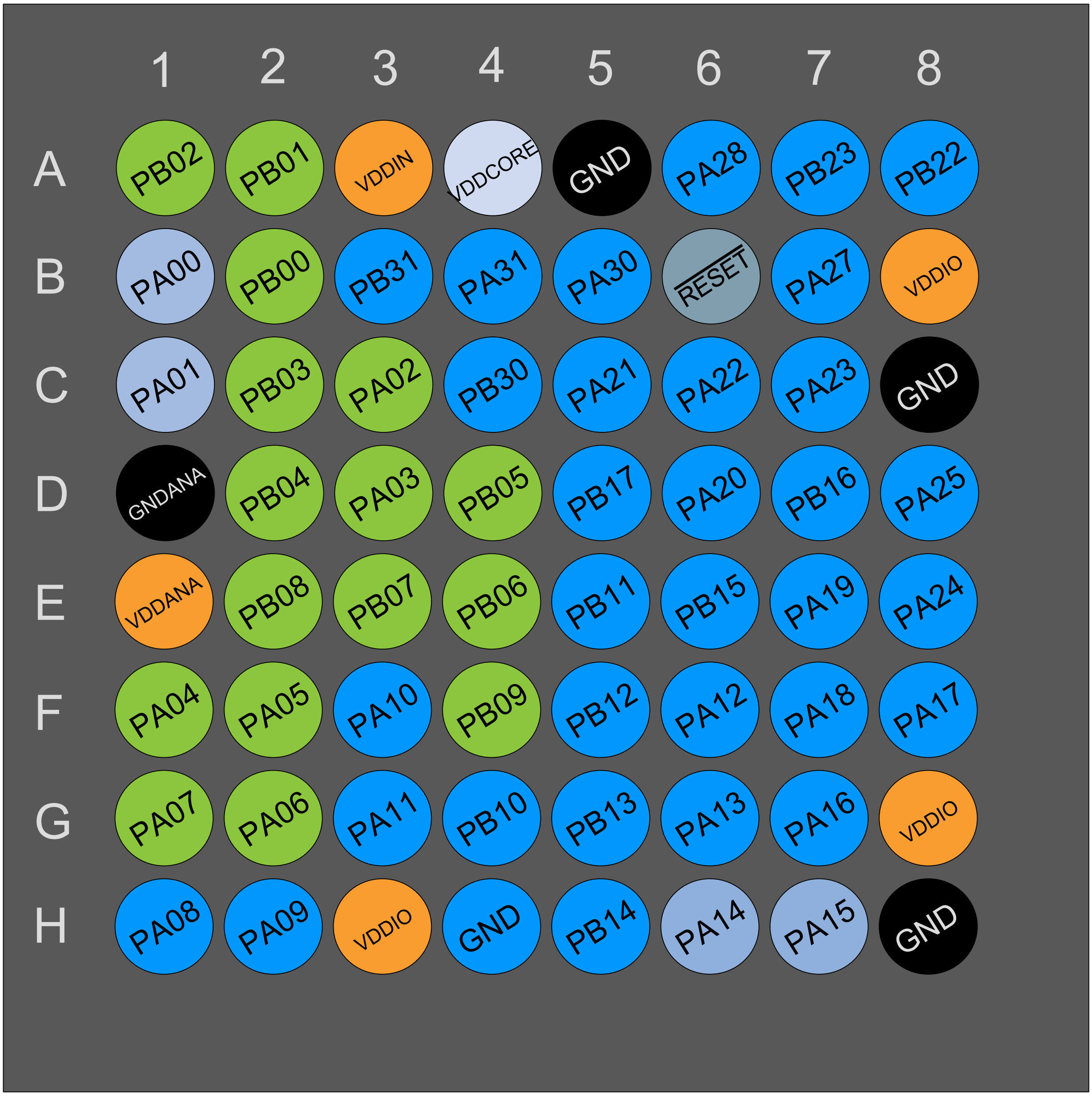
Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAMD20E15A-AU	32K	4K	TQFP32	Tray
ATSAMD20E15A-AUT				Tape & Reel
ATSAMD20E15A-AN				Tray
ATSAMD20E15A-ANT				Tape & Reel
ATSAMD20E15A-MU			QFN32	Tray
ATSAMD20E15A-MUT				Tape & Reel
ATSAMD20E15A-MN				Tray
ATSAMD20E15A-MNT				Tape & Reel
ATSAMD20E16A-AU	64K	8K	TQFP32	Tray
ATSAMD20E16A-AUT				Tape & Reel
ATSAMD20E16A-AN				Tray
ATSAMD20E16A-AFT				Tape & Reel
ATSAMD20E16A-MU			QFN32	Tray
ATSAMD20E16A-MUT				Tape & Reel
ATSAMD20E16A-MN				Tray
ATSAMD20E16A-MNT				Tape & Reel
ATSAMD20E17A-AU	128K	16K	TQFP32	Tray
ATSAMD20E17A-AUT				Tape & Reel
ATSAMD20E17A-AN				Tray
ATSAMD20E17A-ANT				Tape & Reel
ATSAMD20E17A-MU			QFN32	Tray
ATSAMD20E17A-MUT				Tape & Reel
ATSAMD20E17A-MN				Tray
ATSAMD20E17A-MNT				Tape & Reel
ATSAMD20E18A-AU	256K	32K	TQFP32	Tray
ATSAMD20E18A-AUT				Tape & Reel
ATSAMD20E18A-AN				Tray
ATSAMD20E18A-AFT				Tape & Reel
ATSAMD20E18A-MU			QFN32	Tray
ATSAMD20E18A-MUT				Tape & Reel
ATSAMD20E18A-MN				Tray
ATSAMD20E18A-MNT				Tape & Reel

4. Block Diagram



Note: 1. Some products have different number of SERCOM instances, Timer/Counter instances, PTC signals and ADC signals. Refer to *Peripherals Configuration Summary* for details.

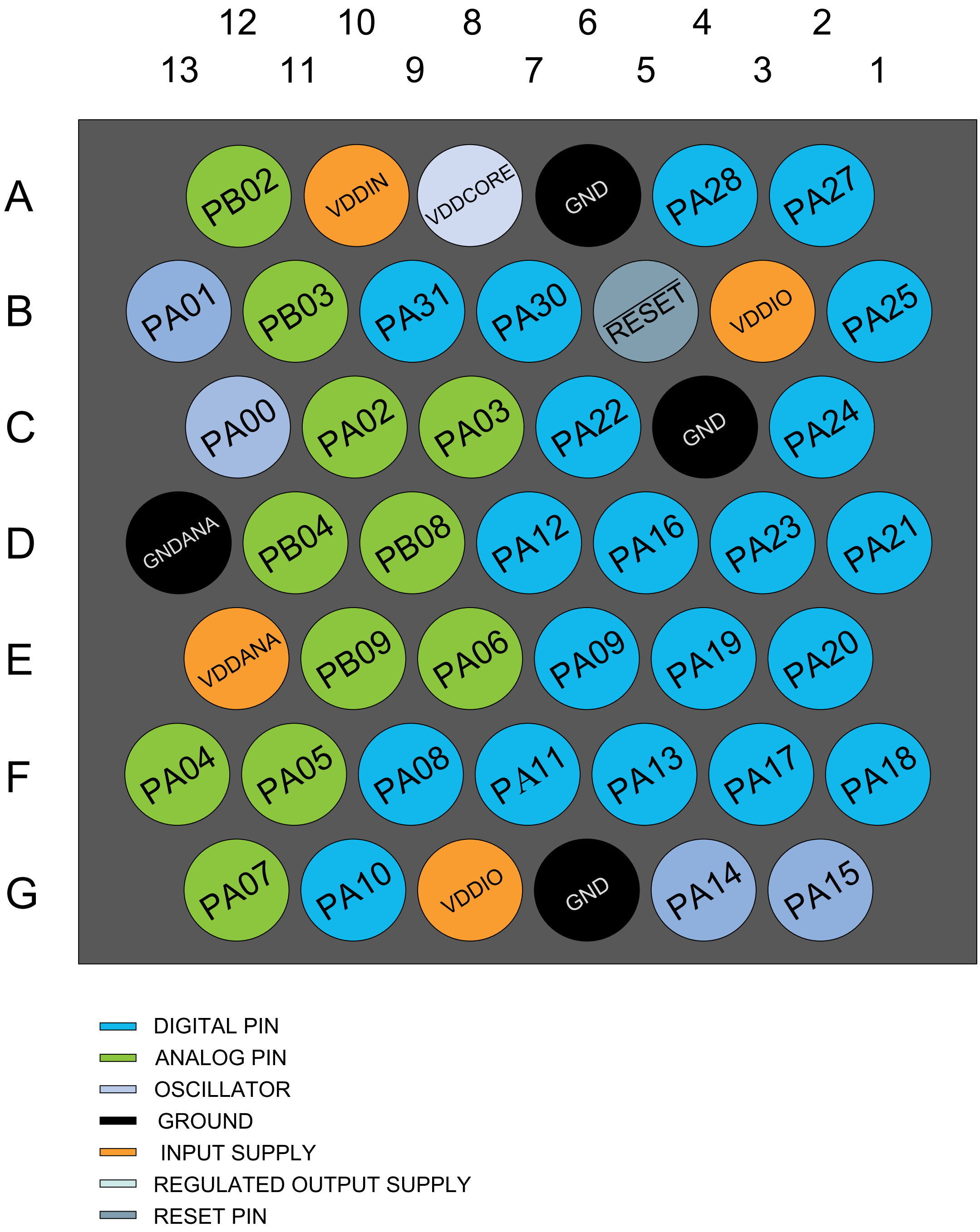
5.1.2. UFBGA64



	1	2	3	4	5	6	7	8
A	PB02	PB01	VDDIN	VDDCORE	GND	PA28	PB23	PB22
B	PA00	PB00	PB31	PA31	PA30	RESET	PA27	VDDIO
C	PA01	PB03	PA02	PB30	PA21	PA22	PA23	GND
D	GNDANA	PB04	PA03	PB05	PB17	PA20	PB16	PA25
E	VDDANA	PB08	PB07	PB06	PB11	PB15	PA19	PA24
F	PA04	PA05	PA10	PB09	PB12	PA12	PA18	PA17
G	PA07	PA06	PA11	PB10	PB13	PA13	PA16	VDDIO
H	PA08	PA09	VDDIO	GND	PB14	PA14	PA15	GND

- ▬ DIGITAL PIN
- ▬ ANALOG PIN
- ▬ OSCILLATOR
- ▬ GROUND
- ▬ INPUT SUPPLY
- ▬ REGULATED OUTPUT SUPPLY
- ▬ RESET PIN

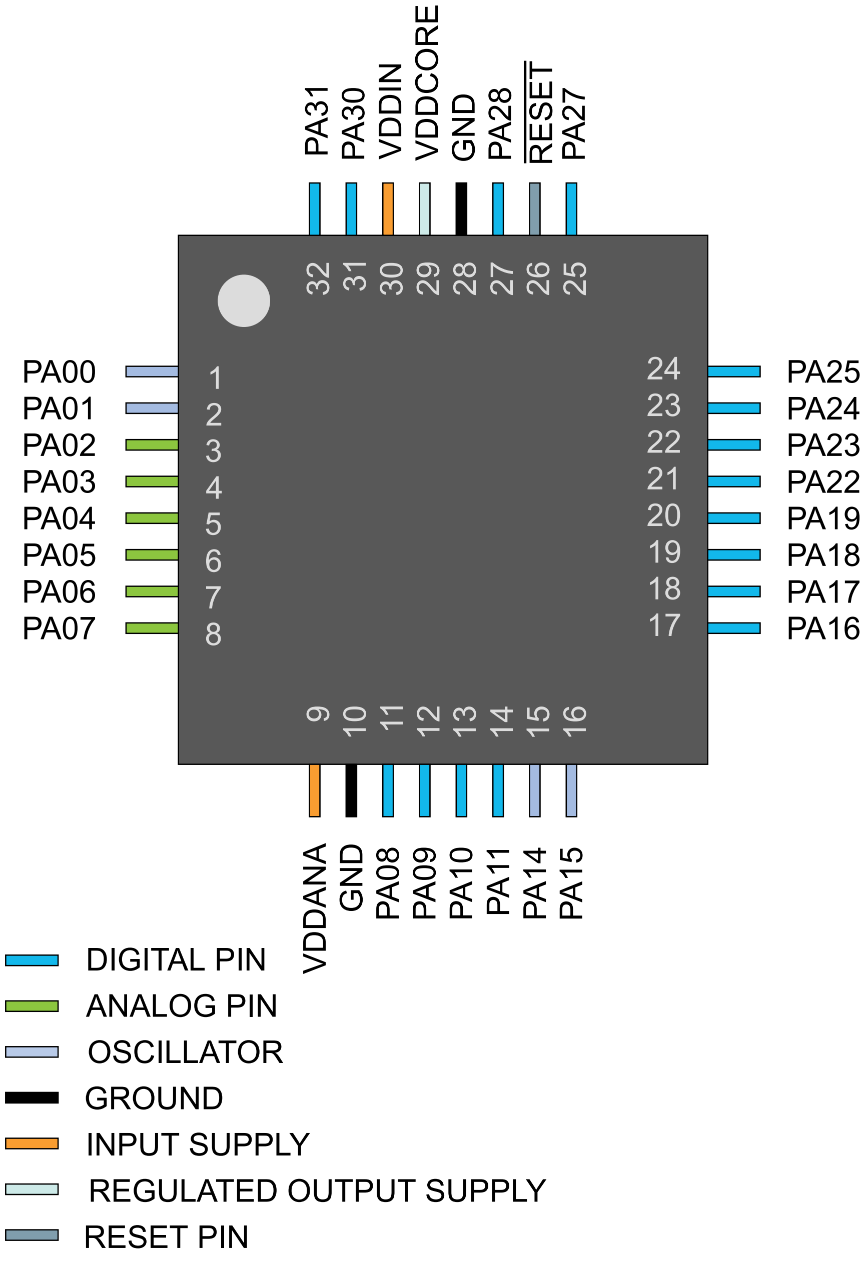
5.2.2. WLCSP45



	13	12	11	10	9	8	7	6	5	4	3	2	1
A		PB02		VDDIN		VDDCORE		GND		PA28		PA27	
B	PA01		PB03		PA31		PA30		RESET		VDDIO		PA25
C		PA00		PA02		PA03		PA22		GND		PA24	
D	GNDANA		PB04		PB08		PA12		PA16		PA23		PA21
E		VDDANA		PB09		PA06		PA09		PA19		PA20	
F	PA04		PA05		PA08		PA11		PA13		PA17		PA18
G		PA07		PA10		VDDIO		GND		PA14		PA15	

5.3. SAM D20E

5.3.1. QFN32 / TQFP32



7. Processor And Architecture

7.1. Cortex M0+ Processor

The SAM D20 implements the ARM® Cortex®-M0+ processor, based on the ARMv6 Architecture and Thumb®-2 ISA. The Cortex M0+ is 100% instruction set compatible with its predecessor, the Cortex-M0 core, and upward compatible to Cortex-M3 and M4 cores. The ARM Cortex-M0+ implemented is revision r0p1. For more information refer to http://www.arm.com.

7.1.1. Cortex M0+ Configuration

Table 7-1. Cortex M0+ Configuration

Features	Configurable option	Device configuration
Interrupts	External interrupts 0-32	28
Data endianness	Little-endian or big-endian	Little-endian
SysTick timer	Present or absent	Present
Number of watchpoint comparators	0, 1, 2	2
Number of breakpoint comparators	0, 1, 2, 3, 4	4
Halting debug support	Present or absent	Present
Multiplier	Fast or small	Fast (single cycle)
Single-cycle I/O port	Present or absent	Present
Wake-up interrupt controller	Supported or not supported	Not supported
Vector Table Offset Register	Present or absent	Present
Unprivileged/Privileged support	Present or absent	Absent(1)
Memory Protection Unit	Not present or 8-region	Not present
Reset all registers	Present or absent	Absent
Instruction fetch width	16-bit only or mostly 32-bit	32-bit

Note:

1. All software run in privileged mode only.

The ARM Cortex-M0+ core has two bus interfaces:

- Single 32-bit AMBA-3 AHB-Lite system interface that provides connections to peripherals and all system memory, which includes flash and RAM.
- Single 32-bit I/O port bus interfacing to the PORT with 1-cycle loads and stores.

7.1.2. Cortex-M0+ Peripherals

- System Control Space (SCS)
  - The processor provides debug through registers in the SCS. Refer to the Cortex-M0+ Technical Reference Manual for details (www.arm.com).
- System Timer (SysTick)

7.4. High-Speed Bus System

7.4.1. Features

High-Speed Bus Matrix has the following features:

- Symmetric crossbar bus switch implementation
- Allows concurrent accesses from different masters to different slaves
- 32-bit data bus
- Operation at a one-to-one clock frequency with the bus masters

7.4.2. Configuration

Table 7-4. Bus Matrix Masters

Bus Matrix Masters	Master ID
CM0+ - Cortex M0+ Processor	0
DSU - Device Service Unit	1

Table 7-5. Bus Matrix Slaves

Bus Matrix Slaves	Slave ID
Internal Flash Memory	0
AHB-APB Bridge A	1
AHB-APB Bridge B	2
AHB-APB Bridge C	3

7.5. AHB-APB Bridge

The AHB-APB bridge is an AHB slave, providing an interface between the high-speed AHB domain and the low-power APB domain. It is used to provide access to the programmable control registers of peripherals (see *Product Mapping*).

AHB-APB bridge is based on AMBA APB Protocol Specification V2.0 (ref. as APB4) including:

- Wait state support
- Error reporting
- Transaction protection
- Sparse data transfer (byte, half-word and word)

Additional enhancements:

- Address and data cycles merged into a single cycle
- Sparse data transfer also apply to read access

to operate the AHB-APB bridge, the clock (CLK_HPBx_AHB) must be enabled. See *PM – Power Manager* for details.

Write-protect registers allow the user to disable a selected peripheral’s write-protection without doing a read-modify-write operation. These registers are mapped into two I/O memory locations, one for clearing and one for setting the register bits. Writing a one to a bit in the Write Protect Clear register (WPCLR) will clear the corresponding bit in both registers (WPCLR and WPSET) and disable the write-protection for the corresponding peripheral, while writing a one to a bit in the Write Protect Set (WPSET) register will set the corresponding bit in both registers (WPCLR and WPSET) and enable the write-protection for the corresponding peripheral. Both registers (WPCLR and WPSET) will return the same value when read.

If a peripheral is write-protected, and if a write access is performed, data will not be written, and the peripheral will return an access error (CPU exception).

The PAC also offers a safety feature for correct program execution, with a CPU exception generated on double write-protection or double unprotection of a peripheral. If a peripheral n is write-protected and a write to one in WPSET[n] is detected, the PAC returns an error. This can be used to ensure that the application follows the intended program flow by always following a write-protect with an unprotect, and vice versa. However, in applications where a write-protected peripheral is used in several contexts, e.g., interrupts, care should be taken so that either the interrupt can not happen while the main application or other interrupt levels manipulate the write-protection status, or when the interrupt handler needs to unprotect the peripheral, based on the current protection status, by reading WPSET.

7.7. Register Description

Atomic 8-, 16- and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly. Refer to the Product Mapping for PAC locations.

Related Links

Product Mapping on page 19

7.7.1. PAC0 Register Description

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 1 – DSU
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

7.7.3. PAC2 Register Description

7.7.3.1. Write Protect Clear

Name: WPCLR
Offset: 0x00
Reset: 0x00800000
Property: –

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
					PTC	DAC	AC	ADC
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TC7	TC6	TC5	TC4	TC3	TC2	TC1	TC0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SERCOM5	SERCOM4	SERCOM3	SERCOM2	SERCOM1	SERCOM0	EVSYS	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	

Bit 19 – PTC
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 18 – DAC
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

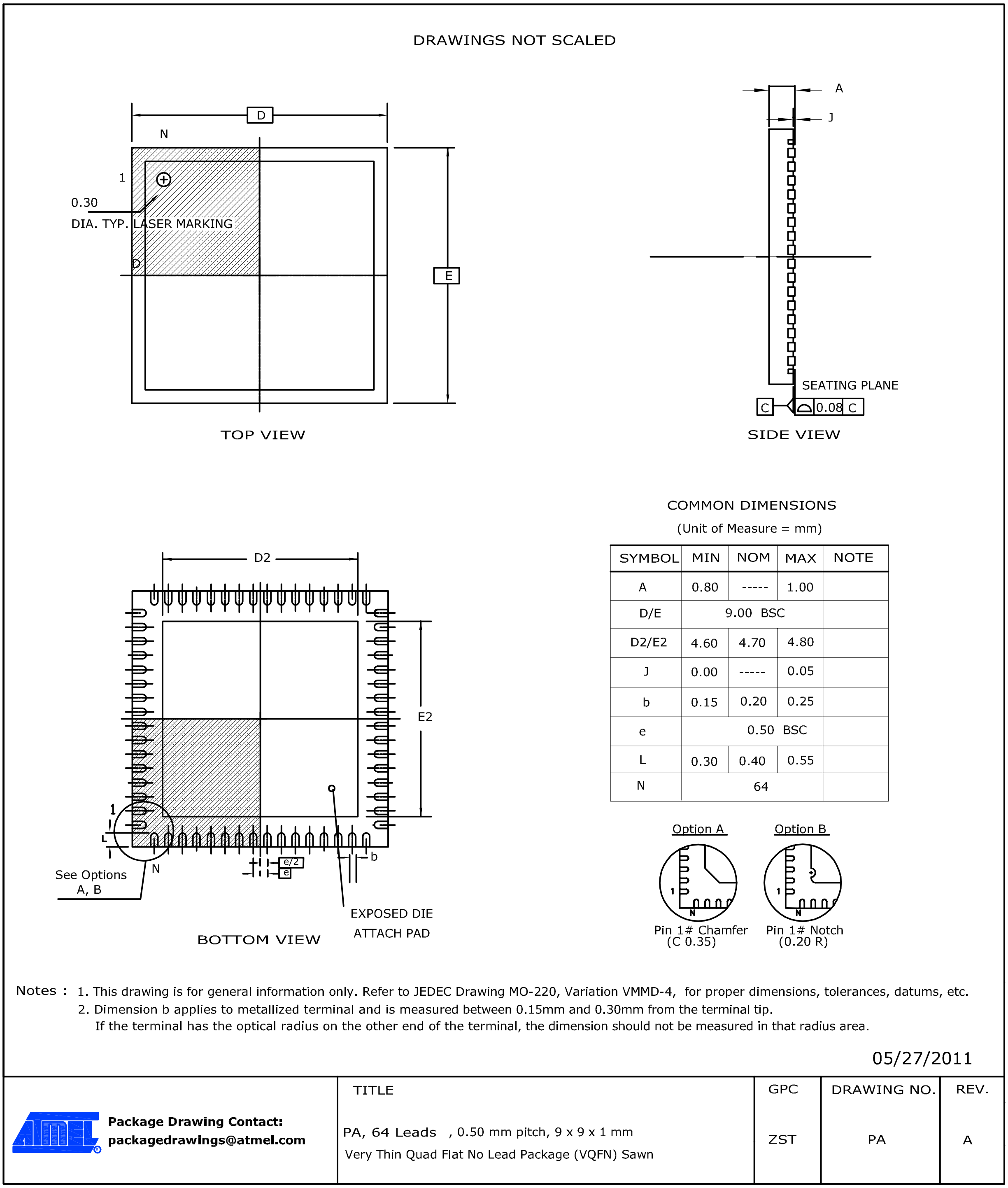
Bit 17 – AC
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Table 8-4. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

8.2.2. 64 pin QFN



COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	-----	1.00	
D/E	9.00 BSC			
D2/E2	4.60	4.70	4.80	
J	0.00	-----	0.05	
b	0.15	0.20	0.25	
e	0.50 BSC			
L	0.30	0.40	0.55	
N	64			

Notes :
1. This drawing is for general information only. Refer to JEDEC Drawing MO-220, Variation VMMD-4, for proper dimensions, tolerances, datums, etc.
2. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
   If the terminal has the optical radius on the other end of the terminal, the dimension should not be measured in that radius area.

05/27/2011

Package Drawing Contact: packagedrawings@atmel.com	TITLE PA, 64 Leads , 0.50 mm pitch, 9 x 9 x 1 mm Very Thin Quad Flat No Lead Package (VQFN) Sawn	GPC ZST	DRAWING NO. PA	REV. A

Note: The exposed die attach pad is not connected electrically inside the device.

Table 8-5. Device and Package Maximum Weight

200	mg

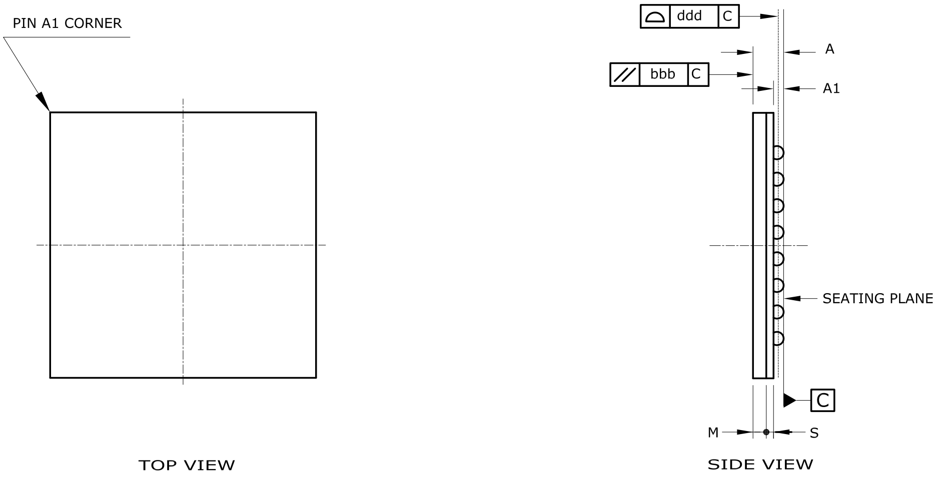
Table 8-6. Package Charateristics

Moisture Sensitivity Level	MSL3

Table 8-7. Package Reference

JEDEC Drawing Reference	MO-220
JESD97 Classification	E3

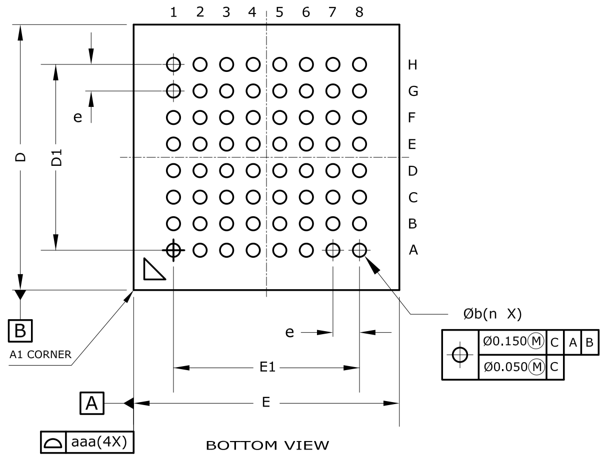
8.2.3. 64-ball UFBGA



COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-----	-----	0.650	
A1	0.140	-----	0.240	
E/D	5.00 / 5.00			
E1/D1	3.50 / 3.50			
b	0.200	-----	0.300	
e	Ball pitch : 0.500			
M	Mold thickness : 0.250 ref			
S	Subst thickness : 0.136 ref			
aaa	Pack edge tolerance : 0.100			
bbb	Mold flatness : 0.100			
ddd	Copla : 0.100			
ball diam	0.250			
n	64			



Notes :
1. This drawing is for general information only. Refer to JEDEC Drawing MO-280, Variation UCCBB for proper dimensions, tolerances, datums, etc.
2. Array as seen from the bottom of the package.
3. Dimension A includes stand-off height A1, package body thickness, and lid height, but does not include attached features.
4. Dimension b is measured at the maximum ball diameter, parallel to primary datum C.

Table 8-8. Device and Package Maximum Weight

27.4	mg

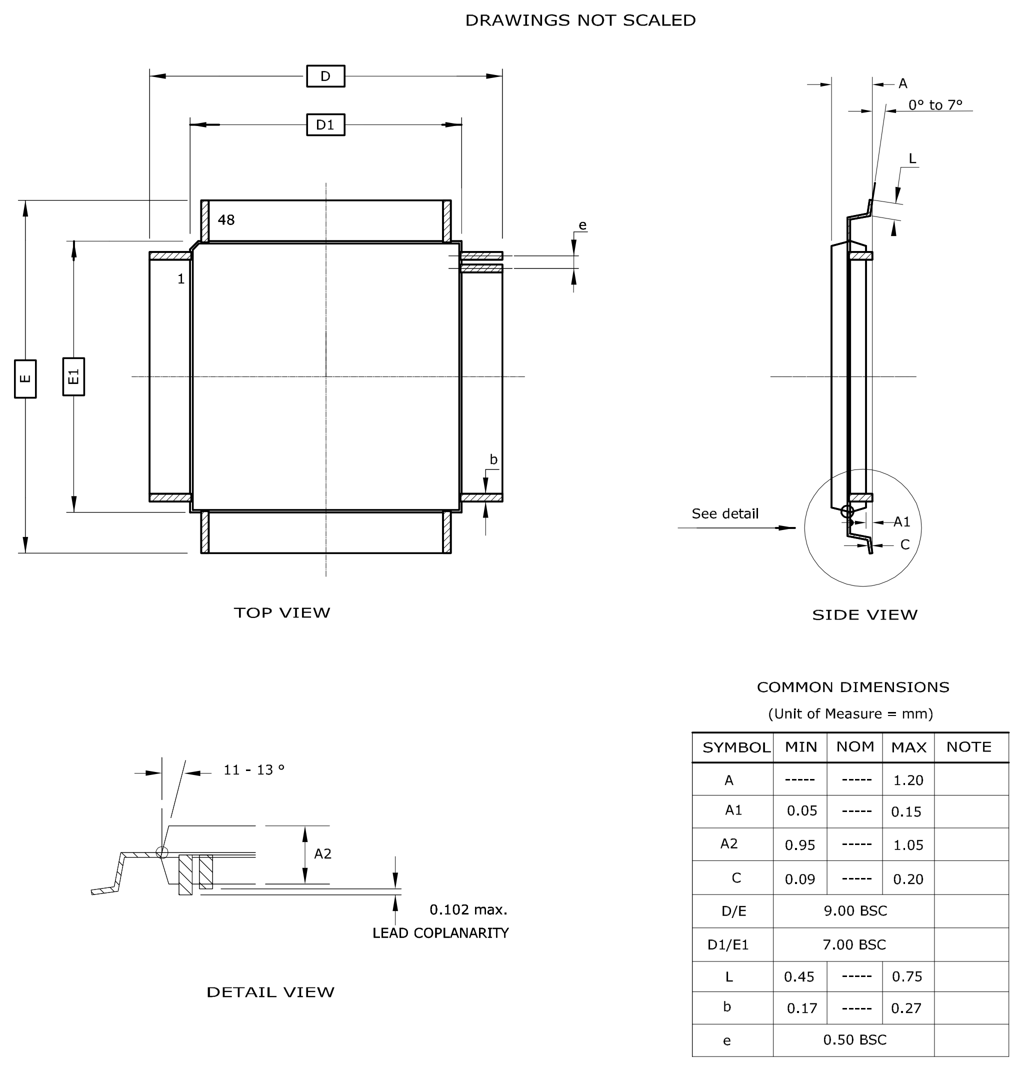
Table 8-9. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 8-10. Package Reference

JEDEC Drawing Reference	MO-220
JESD97 Classification	E8

8.2.4. 48 pin TQFP



COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-----	-----	1.20	
A1	0.05	-----	0.15	
A2	0.95	-----	1.05	
C	0.09	-----	0.20	
D/E	9.00 BSC			
D1/E1	7.00 BSC			
L	0.45	-----	0.75	
b	0.17	-----	0.27	
e	0.50 BSC			

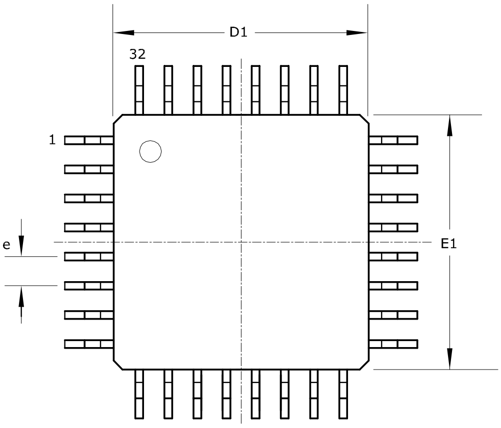
Notes :
1. This drawing is for general information only. Refer to JEDEC Drawing MS-026, Variation ABC.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

10/04/2011

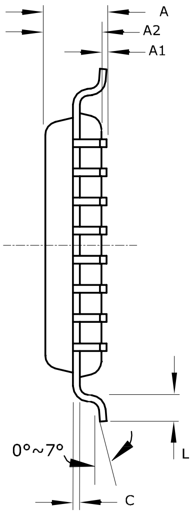
	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: **packagedrawings@atmel.com**	MC, 48 Lds - 0.5mm Pitch, 7x7x1,mm Body size Thin Profile Plastic Quad Flat Package (TQFP)	ALV	MC	E

8.2.7. 32 pin TQFP

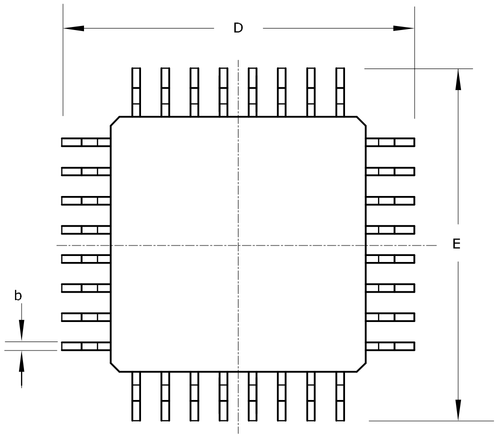
DRAWINGS NOT SCALED



TOP VIEW



SIDE VIEW



BOTTOM VIEW

COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-----	-----	1.20	
A1	0.05	-----	0.15	
A2	0.95	1.00	1.05	
D/E	8.75	9.00	9.25	
D1/E1	6.90	7.00	7.10	2
C	0.09	-----	0.20	
L	0.45	-----	0.75	
b	0.30	-----	0.45	
e	0.80 TYP			
n	32			

Notes :
1. This drawing is for general information only. Refer to JEDEC Drawing MS-026, Variation ABA.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

02/29/2012

	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: **packagedrawings@atmel.com**	MA, 32 Lds - 0.80mm Pitch, 7x7x1.00mm Body size Thin Profile Plastic Quad Flat Package (TQFP)	AUT	MA	C

Table 8-20. Device and Package Maximum Weight

100	mg

Table 8-21. Package Charateristics

Moisture Sensitivity Level	MSL3

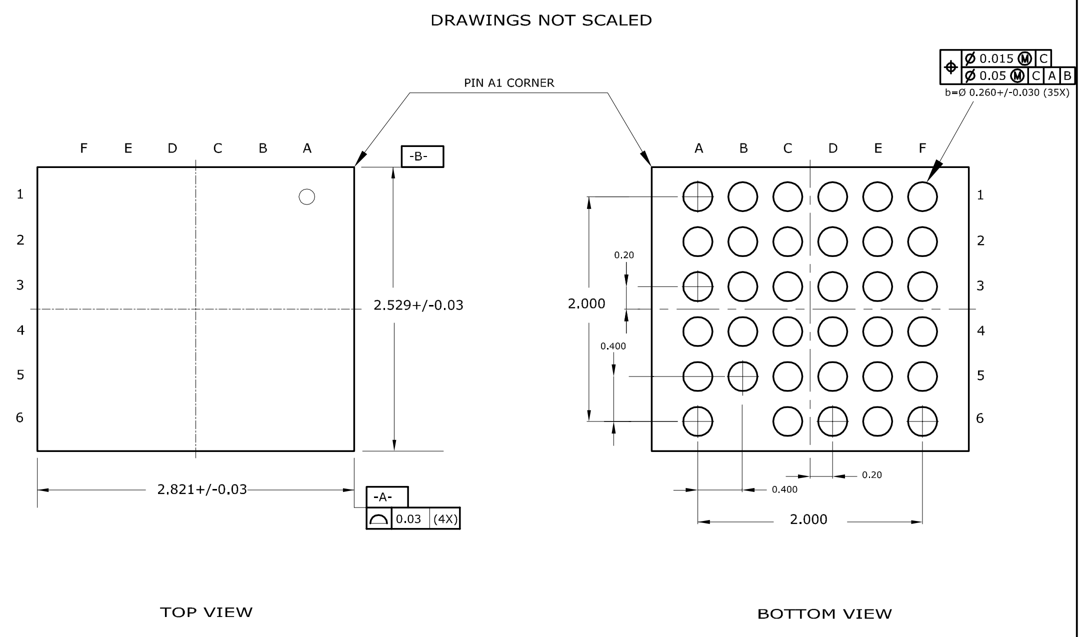
Table 8-24. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 8-25. Package Reference

JEDEC Drawing Reference	MO-220
JESD97 Classification	E3

8.2.9. 35 ball WLCSP

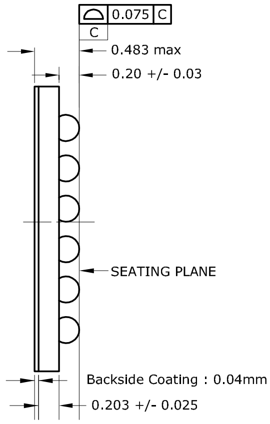


COMMON DIMENSIONS
(Unit of Measure = mm)

BALL	SIGNAL	X COORD	Y COORD
A1	PA00	1	-1
A2	PA01	0.6	-0.6
A3	GNDANA	0.2	-0.2
A4	VDDANA	-0.2	0.2
A5	PA06	1	0.4
A6	VDDIO	1	1
B1	PA30	0.6	-1
B2	PA31	0.2	-0.6
B3	PA02	-0.2	-0.2
B4	PA04	1	0.2
B5	PA07	1	0.4
B6	NO BALL		
C1	VDDCORE	0.2	-1
C2	VDDIO	-0.2	-0.6
C3	PA03	1	-0.2
C4	PA05	1	0.2
C5	PA08	0.6	0.4
C6	PA10	0.2	1
D1	GND	-0.2	-1
D2	PA28	1	-0.6
D3	GND	1	-0.2
D4	PA11	0.6	0.2
D5	PA09	0.2	0.4

BALL	SIGNAL	X COORD	Y COORD
D6	GND	-0.2	1
E1	RESET_N	1	-1
E2	PA27	1	-0.6
E3	PA22	0.6	-0.2
E4	PA17	0.2	0.2
E5	PA16	-0.2	0.4
E6	PA14	1	1
F1	PA25	1	-1
F2	PA24	0.6	-0.6
F3	PA23	0.2	-0.2
F4	PA19	-0.2	0.2
F5	PA18	1	0.4
F6	PA15	1	1

SIDE VIEW



Notes : 1. Dimension "b" is measured at the maximum ball diameter in a plane to the seating plane.

01/07/2016

Atmel **Package Drawing Contact:** **packagedrawings@atmel.com**	TITLE 35 ball - (6X6 Array), 0.4mm pitch 2.821 x 2.529 x 0.483mm, WLCSP	GPC GJR	DRAWING NO. VJ	REV. B

Table 8-26. Device and Package Maximum Weight

6.2	mg

Table 8-27. Package Characteristics

Moisture Sensitivity Level	MSL1

Table 8-28. Package Reference

JEDEC Drawing Reference	MO-220
JESD97 Classification	E1

8.3. Soldering Profile

The following table gives the recommended soldering profile from J-STD-20.

Table 8-29.

Profile Feature	Green Package
Average Ramp-up Rate (217°C to peak)	3°C/s max.
Preheat Temperature 175°C ±25°C	150-200°C
Time Maintained Above 217°C	60-150s
Time within 5°C of Actual Peak Temperature	30s
Peak Temperature Range	260°C
Ramp-down Rate	6°C/s max.
Time 25°C to Peak Temperature	8 minutes max.

A maximum of three reflow passes is allowed per component.