



Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

| | |
|----------------------------|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0+ |
| Core Size | 32-Bit Single-Core |
| Speed | 48MHz |
| Connectivity | I ² C, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, WDT |
| Number of I/O | 26 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.62V ~ 3.6V |
| Data Converters | A/D 10x12b; D/A 1x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 32-TQFP |
| Supplier Device Package | 32-TQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/atsamd20e16a-aut |

1. Description

The Atmel® | SMART™ SAM D20 is a series of low-power microcontrollers using the 32-bit ARM® Cortex®-M0+ processor, and ranging from 32- to 64-pins with up to 256KB Flash and 32KB of SRAM. The SAM D20 devices operate at a maximum frequency of 48MHz and reach 2.46 CoreMark/MHz. They are designed for simple and intuitive migration with identical peripheral modules, hex compatible code, identical linear address map and pin compatible migration paths between all devices in the product series. All devices include intelligent and flexible peripherals, Atmel Event System for inter-peripheral signaling, and support for capacitive touch button, slider and wheel user interfaces.

The SAM D20 devices provide the following features: In-system programmable Flash, eight-channel Event System, programmable interrupt controller, up to 52 programmable I/O pins, 32-bit real-time clock and calendar, up to eight 16-bit Timer/Counters (TC) . The timer/counters can be configured to perform frequency and waveform generation, accurate program execution timing or input capture with time and frequency measurement of digital signals. The TCs can operate in 8- or 16-bit mode, selected TCs can be cascaded to form a 32-bit TC. The series provide up to six Serial Communication Modules (SERCOM) that each can be configured to act as an USART, UART, SPI, I²C up to 400kHz, up to twenty-channel 350ksps 12-bit ADC with programmable gain and optional oversampling and decimation supporting up to 16-bit resolution, one 10-bit 350ksps DAC, two analog comparators with window mode, Peripheral Touch Controller supporting up to 256 buttons, sliders, wheels and proximity sensing; programmable Watchdog Timer, brown-out detector and power-on reset and two-pin Serial Wire Debug (SWD) program and debug interface.

All devices have accurate and low-power external and internal oscillators. All oscillators can be used as a source for the system clock. Different clock domains can be independently configured to run at different frequencies, enabling power saving by running each peripheral at its optimal clock frequency, and thus maintaining a high CPU frequency while reducing power consumption.

The SAM D20 devices have two software-selectable sleep modes, idle and standby. In idle mode the CPU is stopped while all other functions can be kept running. In standby all clocks and functions are stopped except those selected to continue running. The device supports SleepWalking. This feature allows the peripheral to wake up from sleep based on predefined conditions, and thus allows the CPU to wake up only when needed, e.g. when a threshold is crossed or a result is ready. The Event System supports synchronous and asynchronous events, allowing peripherals to receive, react to and send events even in standby mode.

The Flash program memory can be reprogrammed in-system through the SWD interface. The same interface can be used for non-intrusive on-chip debug of application code. A boot loader running in the device can use any communication interface to download and upgrade the application program in the Flash memory.

The SAM D20 devices are supported with a full suite of program and system development tools, including C compilers, macro assemblers, program debugger/simulators, programmers and evaluation kits.

2. Configuration Summary

| | SAM D20J | SAM D20G | SAM D20E |
|---|---|---------------------------------------|---------------------------------------|
| Pins | 64 | 48 | 32 |
| General Purpose I/O-pins (GPIOs) | 52 | 38 | 26 |
| Flash | 256/128/64/32KB | 256/128/64/32KB | 256/128/64/32KB |
| SRAM | 32/16/8/4/2KB | 32/16/8/4/2KB | 32/16/8/4/2KB |
| Timer Counter (TC) instances | 8 | 6 | 6 |
| Waveform output channels per TC instance | 2 | 2 | 2 |
| Serial Communication Interface (SERCOM) instances | 6 | 6 | 4 |
| Analog-to-Digital Converter (ADC) channels | 20 | 14 | 10 |
| Analog Comparators (AC) | 2 | 2 | 2 |
| Digital-to-Analog Converter (DAC) channels | 1 | 1 | 1 |
| Real-Time Counter (RTC) | Yes | Yes | Yes |
| RTC alarms | 1 | 1 | 1 |
| RTC compare values | One 32-bit value or two 16-bit values | One 32-bit value or two 16-bit values | One 32-bit value or two 16-bit values |
| External Interrupt lines | 16 | 16 | 16 |
| Peripheral Touch Controller (PTC) X and Y lines | 16x16 | 12x10 | 10x6 |
| Maximum CPU frequency | 48MHz | | |
| Packages | QFN TQFP UFBGA | QFN TQFP WLCSP | QFN TQFP |
| Oscillators | 32.768kHz crystal oscillator (XOSC32K) 0.4-32MHz crystal oscillator (XOSC) 32.768kHz internal oscillator (OSC32K) 32KHz ultra-low-power internal oscillator (OSCULP32K) 8MHz high-accuracy internal oscillator (OSC8M) 48MHz Digital Frequency Locked Loop (DFLL48M) | | |
| Event System channels | 8 | 8 | 8 |
| SW Debug Interface | Yes | Yes | Yes |
| Watchdog Timer (WDT) | Yes | Yes | Yes |

3.2. SAM D20G

| Ordering Code | FLASH (bytes) | SRAM (bytes) | Package | Carrier Type |
|------------------|---------------|--------------|---------|--------------|
| ATSAMD20G14A-AU | 16K | 2K | TQFP32 | Tray |
| ATSAMD20G14A-AUT | | | | Tape & Reel |
| ATSAMD20G14A-AN | | | | Tray |
| ATSAMD20G14A-ANT | | | | Tape & Reel |
| ATSAMD20G14A-MU | | | QFN32 | Tray |
| ATSAMD20G14A-MUT | | | | Tape & Reel |
| ATSAMD20G14A-MN | | | | Tray |
| ATSAMD20G14A-MNT | | | | Tape & Reel |
| ATSAMD20G15A-AU | 32K | 4K | TQFP48 | Tray |
| ATSAMD20G15A-AUT | | | | Tape & Reel |
| ATSAMD20G15A-AN | | | | Tray |
| ATSAMD20G15A-ANT | | | | Tape & Reel |
| ATSAMD20G15A-MU | | | QFN48 | Tray |
| ATSAMD20G15A-MUT | | | | Tape & Reel |
| ATSAMD20G15A-MN | | | | Tray |
| ATSAMD20G15A-MNT | | | | Tape & Reel |
| ATSAMD20G16A-AU | 64K | 8K | TQFP48 | Tray |
| ATSAMD20G16A-AUT | | | | Tape & Reel |
| ATSAMD20G16A-AN | | | | Tray |
| ATSAMD20G16A-ANT | | | | Tape & Reel |
| ATSAMD20G16A-MU | | | QFN48 | Tray |
| ATSAMD20G16A-MUT | | | | Tape & Reel |
| ATSAMD20G16A-MN | | | | Tray |
| ATSAMD20G16A-MNT | | | | Tape & Reel |

| Ordering Code | FLASH (bytes) | SRAM (bytes) | Package | Carrier Type |
|------------------|---------------|--------------|---------|--------------|
| ATSAMD20G17A-AU | 128K | 16K | TQFP48 | Tray |
| ATSAMD20G17A-AUT | | | | Tape & Reel |
| ATSAMD20G17A-AN | | | | Tray |
| ATSAMD20G17A-ANT | | | | Tape & Reel |
| ATSAMD20G17A-MU | | | QFN48 | Tray |
| ATSAMD20G17A-MUT | | | | Tape & Reel |
| ATSAMD20G17A-MN | | | | Tray |
| ATSAMD20G17A-MNT | | | | Tape & Reel |
| ATSAMD20G17A-UUT | | | WLCSP45 | Tape & Reel |
| ATSAMD20G18A-AU | 256K | 32K | TQFP48 | Tray |
| ATSAMD20G18A-AUT | | | | Tape & Reel |
| ATSAMD20G18A-AN | | | | Tray |
| ATSAMD20G18A-ANT | | | | Tape & Reel |
| ATSAMD20G18A-MU | | | QFN48 | Tray |
| ATSAMD20G18A-MUT | | | | Tape & Reel |
| ATSAMD20G18A-MN | | | | Tray |
| ATSAMD20G18A-MNT | | | | Tape & Reel |
| ATSAMD20G18A-UUT | | | WLCSP45 | Tape & Reel |

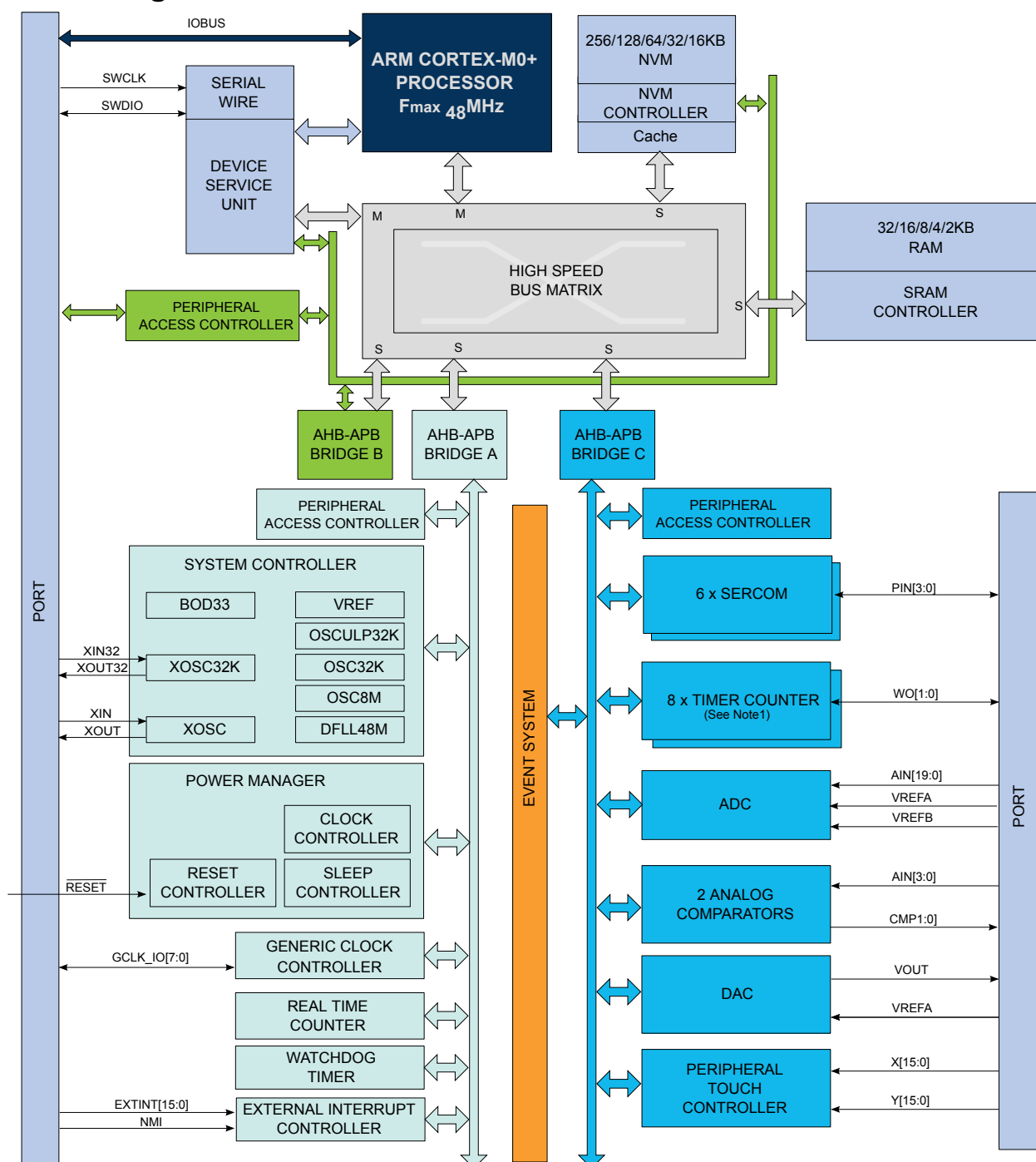
3.3. SAM D20J

| Ordering Code | FLASH (bytes) | SRAM (bytes) | Package | Carrier Type |
|------------------|---------------|--------------|---------|--------------|
| ATSAMD20J14A-AU | 16K | 2K | TQFP64 | Tray |
| ATSAMD20J14A-AUT | | | | Tape & Reel |
| ATSAMD20J14A-AN | | | | Tray |
| ATSAMD20J14A-ANT | | | | Tape & Reel |
| ATSAMD20J14A-MU | | | QFN64 | Tray |
| ATSAMD20J14A-MUT | | | | Tape & Reel |
| ATSAMD20J14A-MN | | | | Tray |
| ATSAMD20J14A-MNT | | | | Tape & Reel |

| Device Variant | DID.DEVSEL | Device ID (DID) |
|----------------|-------------|-----------------|
| SAMD20E14A | 0x0E | 0x1000130E |
| Reserved | 0x0F | |
| SAMD20G18U | 0x10 | 0x10001310 |
| SAMD20G17U | 0x11 | 0x10001311 |
| Reserved | 0x12 - 0xFF | |

Note: The device variant (last letter of the ordering number) is independent of the die revision (DSU.DID.REVISION): The device variant denotes functional differences, whereas the die revision marks evolution of the die. The device variant denotes functional differences, whereas the die revision marks evolution of the die.

4. Block Diagram

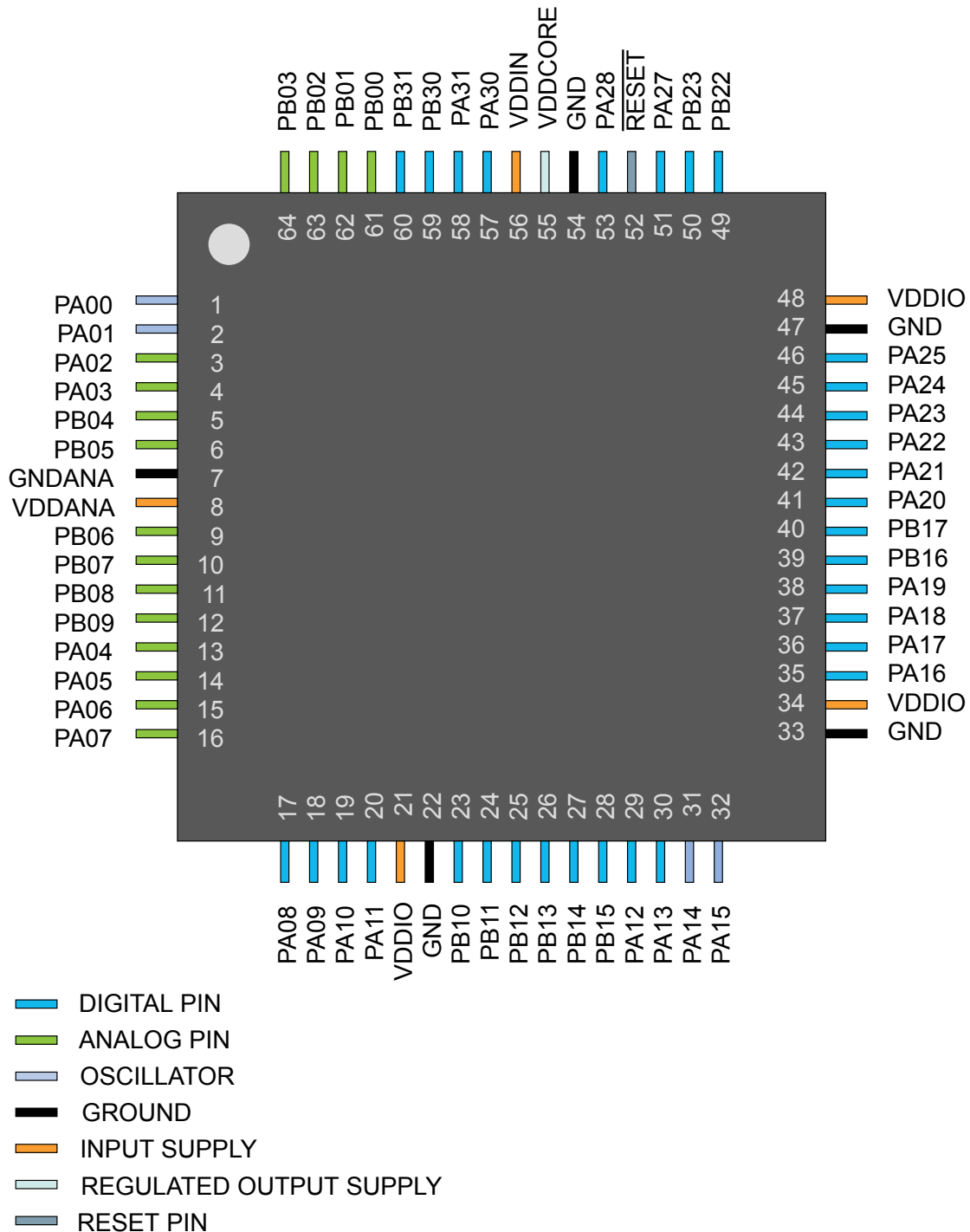


Note: 1. Some products have different number of SERCOM instances, Timer/Counter instances, PTC signals and ADC signals. Refer to *Peripherals Configuration Summary* for details.

5. Pinout

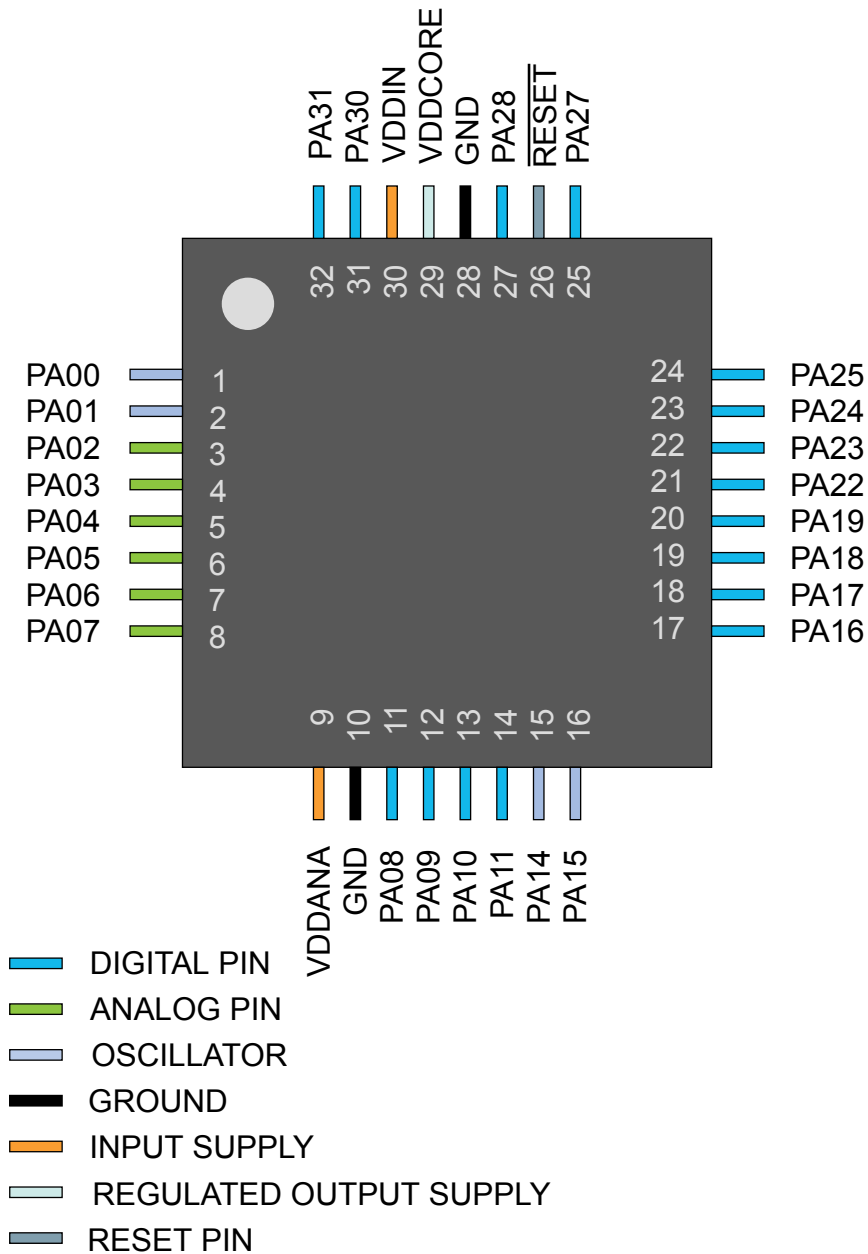
5.1. SAM D20J

5.1.1. QFN64 / TQFP64



5.3. SAM D20E

5.3.1. QFN32 / TQFP32



- The System Timer is a 24-bit timer that extends the functionality of both the processor and the NVIC. Refer to the Cortex-M0+ Technical Reference Manual for details (www.arm.com).
- Nested Vectored Interrupt Controller (NVIC)
 - External interrupt signals connect to the NVIC, and the NVIC prioritizes the interrupts. Software can set the priority of each interrupt. The NVIC and the Cortex-M0+ processor core are closely coupled, providing low latency interrupt processing and efficient processing of late arriving interrupts. Refer to [Nested Vector Interrupt Controller](#) and the Cortex-M0+ Technical Reference Manual for details (www.arm.com).
- System Control Block (SCB)
 - The System Control Block provides system implementation information, and system control. This includes configuration, control, and reporting of the system exceptions. Refer to the Cortex-M0+ Devices Generic User Guide for details (www.arm.com).
- Micro Trace Buffer (MTB)
 - The CoreSight MTB-M0+ (MTB) provides a simple execution trace capability to the Cortex-M0+ processor. Refer to section [Micro Trace Buffer](#) and the CoreSight MTB-M0+ Technical Reference Manual for details (www.arm.com).

7.1.3. Cortex-M0+ Address Map

Table 7-2. Cortex-M0+ Address Map

| Address | Peripheral |
|---------------------------------------|---|
| 0xE000E000 | System Control Space (SCS) |
| 0xE000E010 | System Timer (SysTick) |
| 0xE000E100 | Nested Vectored Interrupt Controller (NVIC) |
| 0xE000ED00 | System Control Block (SCB) |
| 0x41006000 (see also Product Mapping) | Micro Trace Buffer (MTB) |

7.1.4. I/O Interface

7.1.4.1. Overview

Because accesses to the AMBA® AHB-Lite™ and the single cycle I/O interface can be made concurrently, the Cortex-M0+ processor can fetch the next instructions while accessing the I/Os. This enables single cycle I/O accesses to be sustained for as long as needed. Refer to *CPU Local Bus* for more information.

7.1.4.2. Description

Direct access to PORT registers.

7.2. Nested Vector Interrupt Controller

7.2.1. Overview

The Nested Vectored Interrupt Controller (NVIC) in the SAM D20 supports 32 interrupt lines with four different priority levels. For more details, refer to the Cortex-M0+ Technical Reference Manual (www.arm.com).

7.2.2. Interrupt Line Mapping

Each of the 28 interrupt lines is connected to one peripheral instance, as shown in the table below. Each peripheral can have one or more interrupt flags, located in the peripheral's Interrupt Flag Status and Clear

7.4. High-Speed Bus System

7.4.1. Features

High-Speed Bus Matrix has the following features:

- Symmetric crossbar bus switch implementation
- Allows concurrent accesses from different masters to different slaves
- 32-bit data bus
- Operation at a one-to-one clock frequency with the bus masters

7.4.2. Configuration

Table 7-4. Bus Matrix Masters

| Bus Matrix Masters | Master ID |
|-----------------------------|-----------|
| CM0+ - Cortex M0+ Processor | 0 |
| DSU - Device Service Unit | 1 |

Table 7-5. Bus Matrix Slaves

| Bus Matrix Slaves | Slave ID |
|-----------------------|----------|
| Internal Flash Memory | 0 |
| AHB-APB Bridge A | 1 |
| AHB-APB Bridge B | 2 |
| AHB-APB Bridge C | 3 |

7.5. AHB-APB Bridge

The AHB-APB bridge is an AHB slave, providing an interface between the high-speed AHB domain and the low-power APB domain. It is used to provide access to the programmable control registers of peripherals (see *Product Mapping*).

AHB-APB bridge is based on AMBA APB Protocol Specification V2.0 (ref. as APB4) including:

- Wait state support
- Error reporting
- Transaction protection
- Sparse data transfer (byte, half-word and word)

Additional enhancements:

- Address and data cycles merged into a single cycle
- Sparse data transfer also apply to read access

to operate the AHB-APB bridge, the clock (CLK_HPBB_AHB) must be enabled. See *PM – Power Manager* for details.

Figure 7-1. APB Write Access.

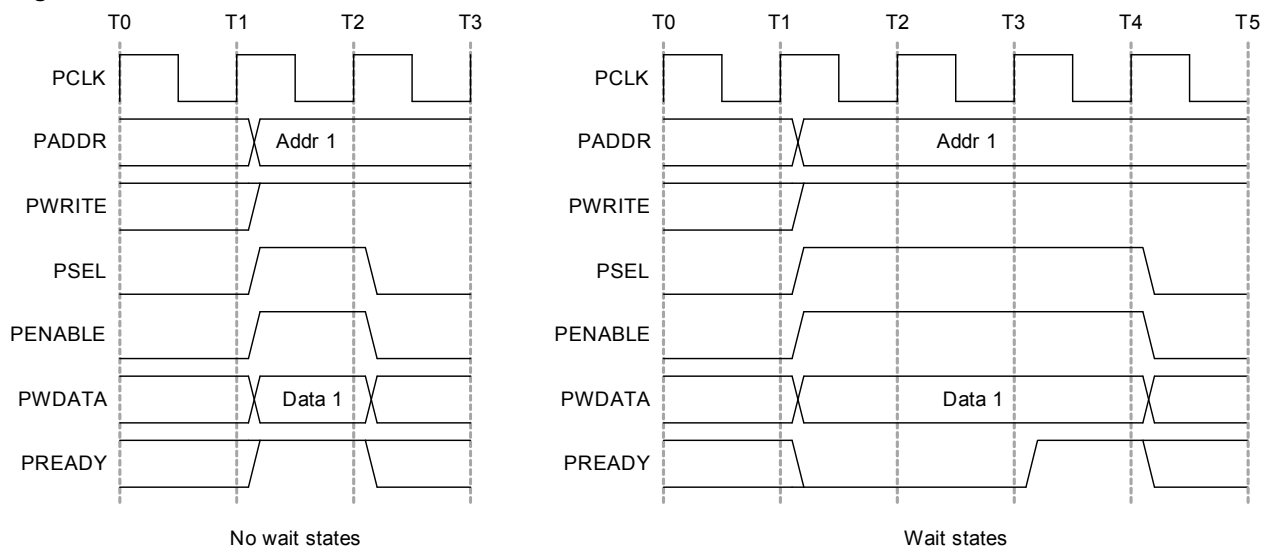
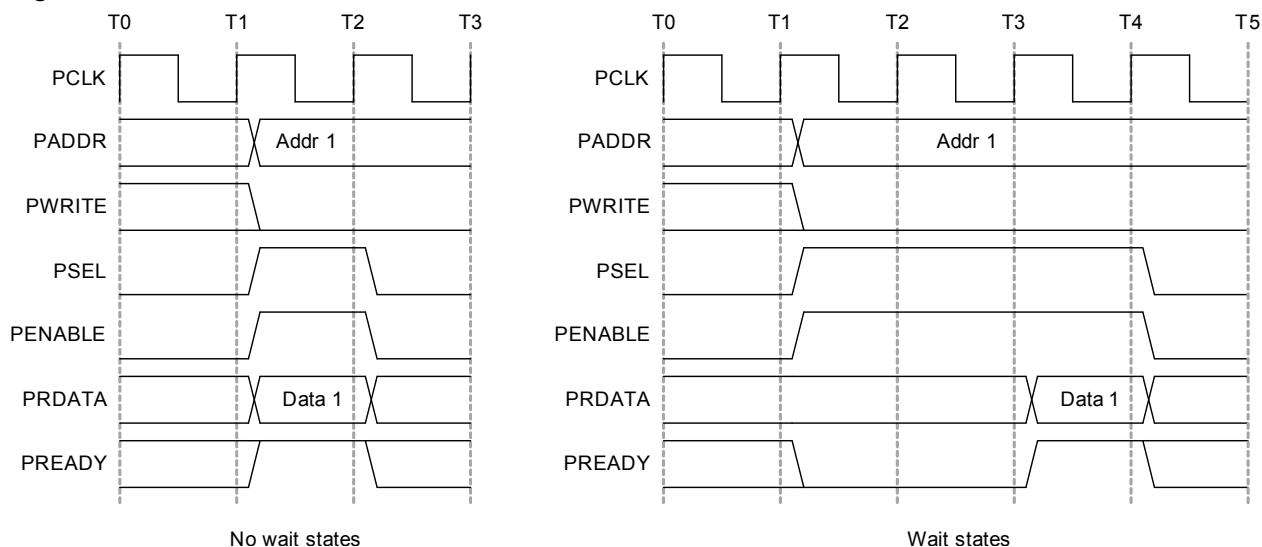


Figure 7-2. APB Read Access.



Related Links

[Product Mapping](#) on page 19

7.6. PAC - Peripheral Access Controller

7.6.1. Overview

There is one PAC associated with each AHB-APB bridge. The PAC can provide write protection for registers of each peripheral connected on the same bridge.

The PAC peripheral bus clock (CLK_PACx_APB) can be enabled and disabled in the Power Manager. CLK_PAC0_APB and CLK_PAC1_APB are enabled at reset. CLK_PAC2_APB is disabled at reset. Refer to *PM – Power Manager* for details. The PAC will continue to operate in any sleep mode where the selected clock source is running. Write-protection does not apply for debugger access. When the debugger makes an access to a peripheral, write-protection is ignored so that the debugger can update the register.

Write-protect registers allow the user to disable a selected peripheral's write-protection without doing a read-modify-write operation. These registers are mapped into two I/O memory locations, one for clearing and one for setting the register bits. Writing a one to a bit in the Write Protect Clear register (WPCLR) will clear the corresponding bit in both registers (WPCLR and WPSET) and disable the write-protection for the corresponding peripheral, while writing a one to a bit in the Write Protect Set (WPSET) register will set the corresponding bit in both registers (WPCLR and WPSET) and enable the write-protection for the corresponding peripheral. Both registers (WPCLR and WPSET) will return the same value when read.

If a peripheral is write-protected, and if a write access is performed, data will not be written, and the peripheral will return an access error (CPU exception).

The PAC also offers a safety feature for correct program execution, with a CPU exception generated on double write-protection or double unprotection of a peripheral. If a peripheral *n* is write-protected and a write to one in WPSET[*n*] is detected, the PAC returns an error. This can be used to ensure that the application follows the intended program flow by always following a write-protect with an unprotect, and vice versa. However, in applications where a write-protected peripheral is used in several contexts, e.g., interrupts, care should be taken so that either the interrupt can not happen while the main application or other interrupt levels manipulate the write-protection status, or when the interrupt handler needs to unprotect the peripheral, based on the current protection status, by reading WPSET.

7.7. Register Description

Atomic 8-, 16- and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly. Refer to the Product Mapping for PAC locations.

Related Links

[Product Mapping](#) on page 19

7.7.1. PAC0 Register Description

7.7.1.1. Write Protect Clear

Name: WPCLR
Offset: 0x00
Reset: 0x000000
Property: –

| | | | | | | | | |
|--------|----|-----|-----|-----|------|---------|-----|----|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| | | | | | | | | |
| Access | | | | | | | | |
| Reset | | | | | | | | |
| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | | | | | | | |
| Access | | | | | | | | |
| Reset | | | | | | | | |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | | | | | | |
| Access | | | | | | | | |
| Reset | | | | | | | | |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | EIC | RTC | WDT | GCLK | SYSCTRL | PM | |
| Access | | R/W | R/W | R/W | R/W | R/W | R/W | |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | |

Bit 6 – EIC

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|-------|-------------------------------|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

Bit 5 – RTC

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|-------|-------------------------------|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

Bit 4 – WDT

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|-------|-------------------------------|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

Bit 3 – GCLK

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|-------|-------------------------------|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

Bit 2 – SYSCTRL

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|-------|-------------------------------|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

Bit 1 – PM

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|-------|-------------------------------|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

| Value | Description |
|-------|-------------------------------|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

Bit 3 – GCLK

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|-------|-------------------------------|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

Bit 2 – SYSCTRL

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|-------|-------------------------------|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

Bit 1 – PM

Writing a zero to these bits has no effect.

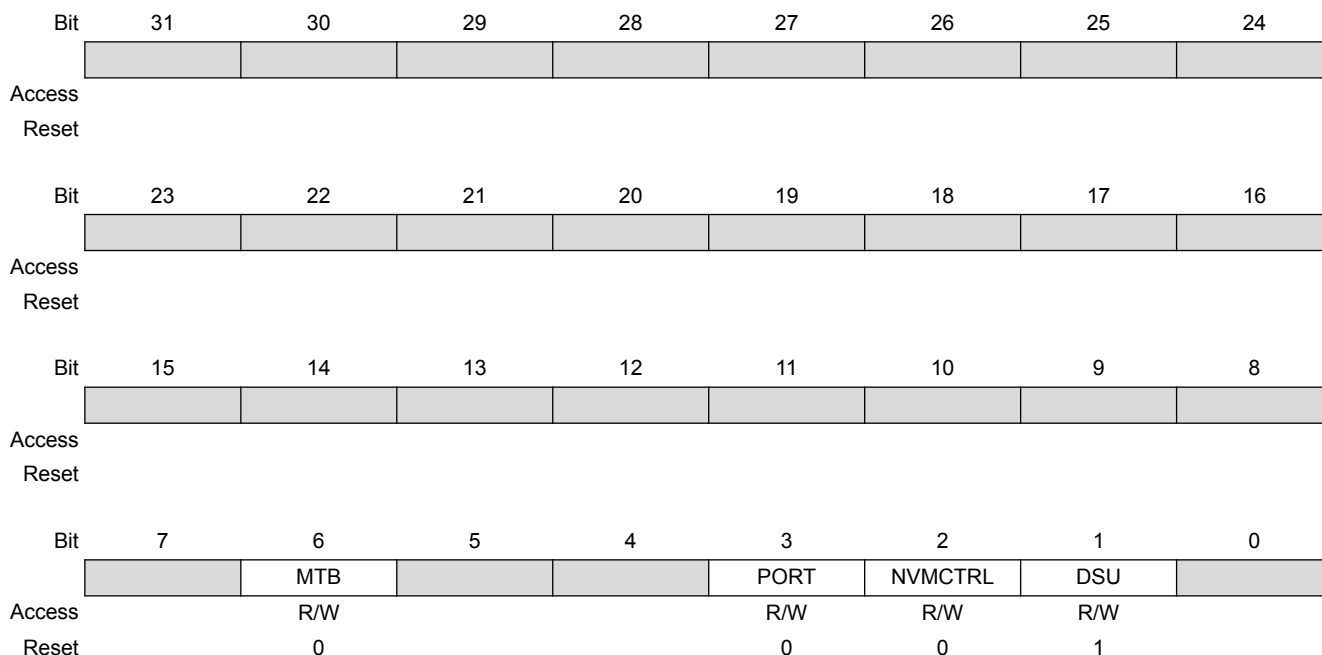
Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|-------|-------------------------------|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

7.7.2. PAC1 Register Description

7.7.2.1. Write Protect Clear

Name: WPCLR
Offset: 0x00
Reset: 0x000002
Property: –



Bit 6 – MTB

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|-------|-------------------------------|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

Bit 3 – PORT

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|-------|-------------------------------|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

Bit 2 – NVMCTRL

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

8.2. Package Drawings

8.2.1. 64 pin TQFP

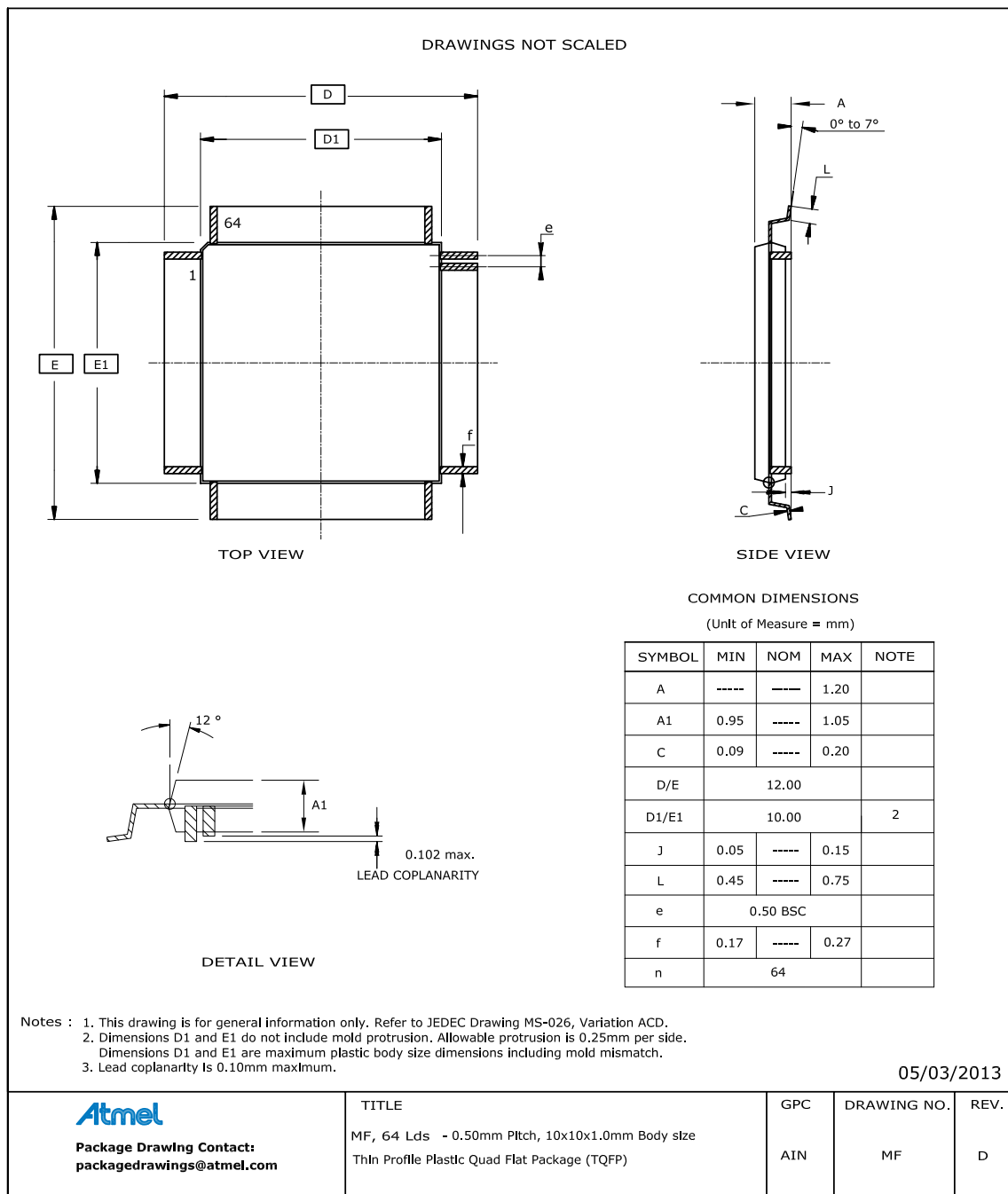


Table 8-2. Device and Package Maximum Weight

| | |
|-----|----|
| 300 | mg |
|-----|----|

Table 8-3. Package Characteristics

| | |
|----------------------------|------|
| Moisture Sensitivity Level | MSL3 |
|----------------------------|------|

Table 8-5. Device and Package Maximum Weight

| | |
|-----|----|
| 200 | mg |
|-----|----|

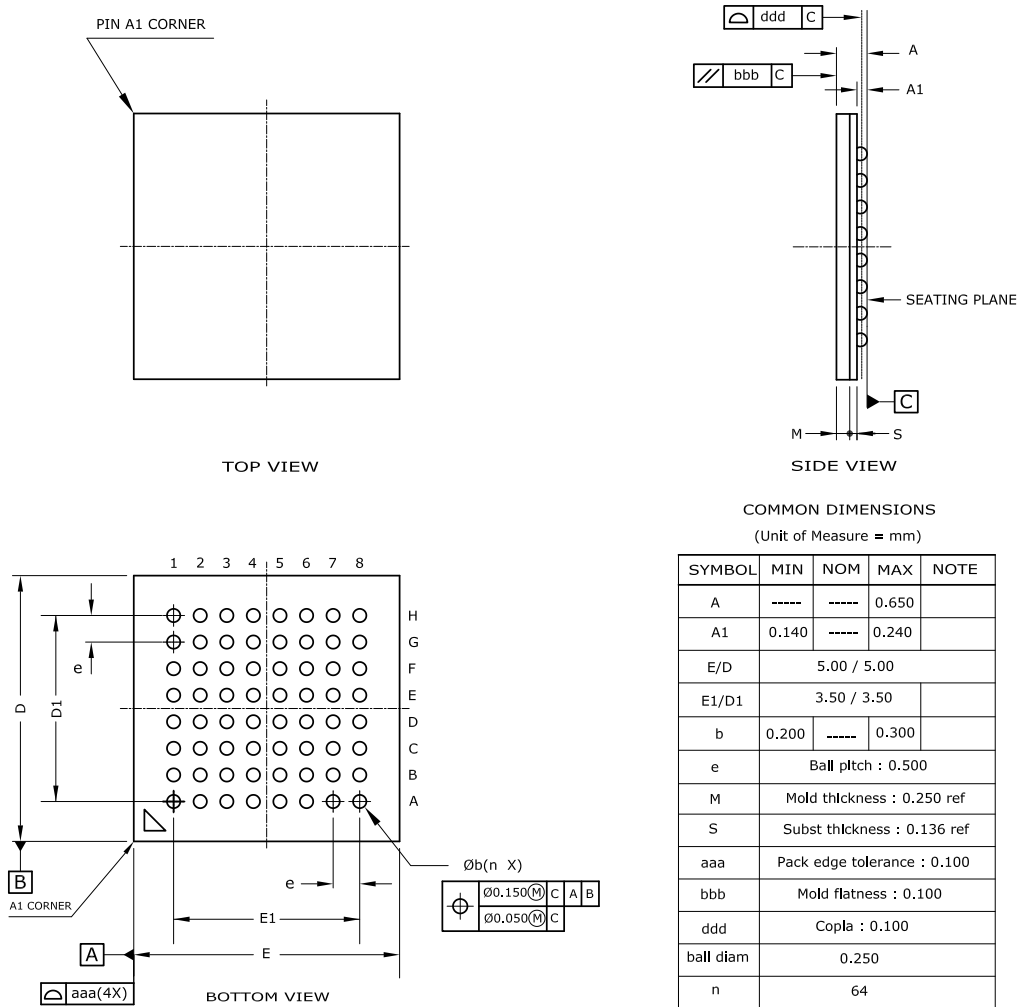
Table 8-6. Package Characteristics

| | |
|----------------------------|------|
| Moisture Sensitivity Level | MSL3 |
|----------------------------|------|

Table 8-7. Package Reference

| | |
|-------------------------|--------|
| JEDEC Drawing Reference | MO-220 |
| JESD97 Classification | E3 |

8.2.3. 64-ball UFBGA



- Notes :
1. This drawing is for general information only. Refer to JEDEC Drawing MO-280, Variation UCCBB for proper dimensions, tolerances, datums, etc.
 2. Array as seen from the bottom of the package.
 3. Dimension A includes stand-off height A1, package body thickness, and lid height, but does not include attached features.
 4. Dimension b is measured at the maximum ball diameter, parallel to primary datum C.

Table 8-8. Device and Package Maximum Weight

| | |
|------|----|
| 27.4 | mg |
|------|----|

Table 8-16. Package Reference

| | |
|-------------------------|--------|
| JEDEC Drawing Reference | MO-220 |
| JESD97 Classification | E3 |

8.2.6. 45-ball WLCSP

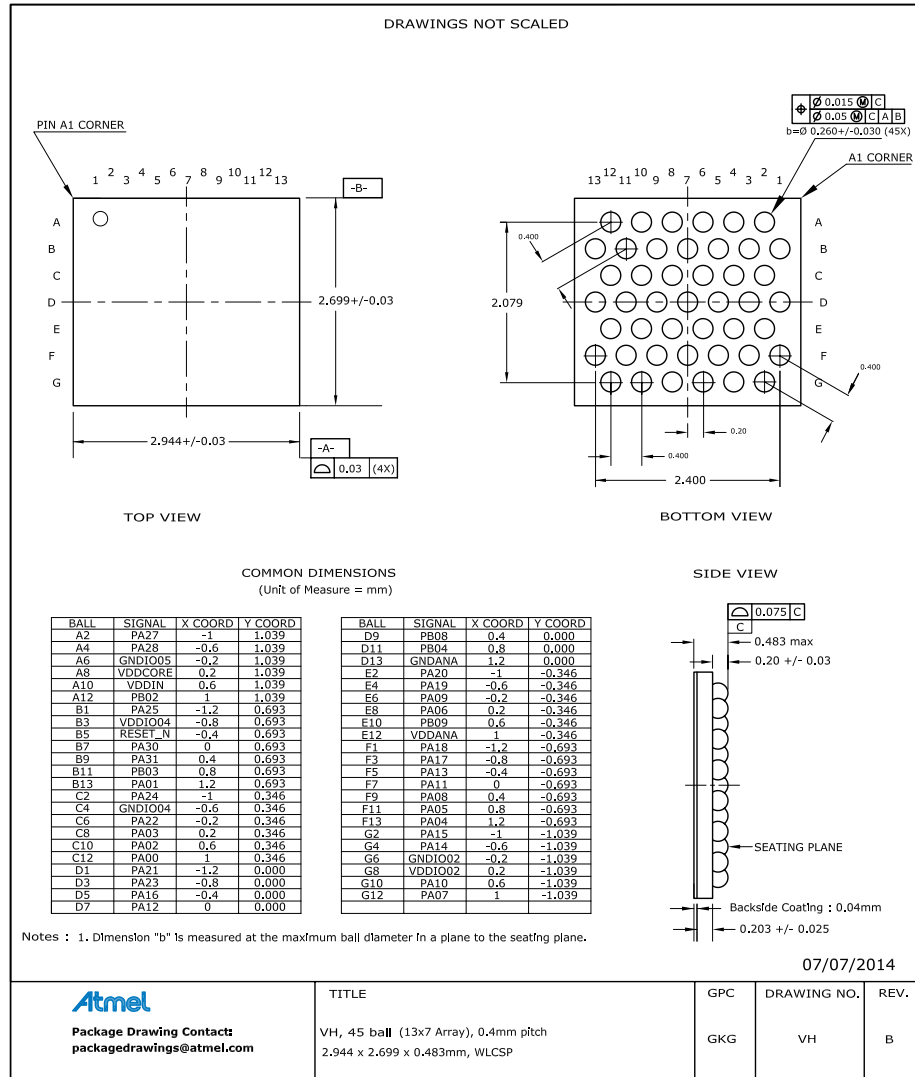


Table 8-17. Device and Package Maximum Weight

| | |
|-----|----|
| 7.3 | mg |
|-----|----|

Table 8-18. Package Characteristics

| | |
|----------------------------|------|
| Moisture Sensitivity Level | MSL1 |
|----------------------------|------|

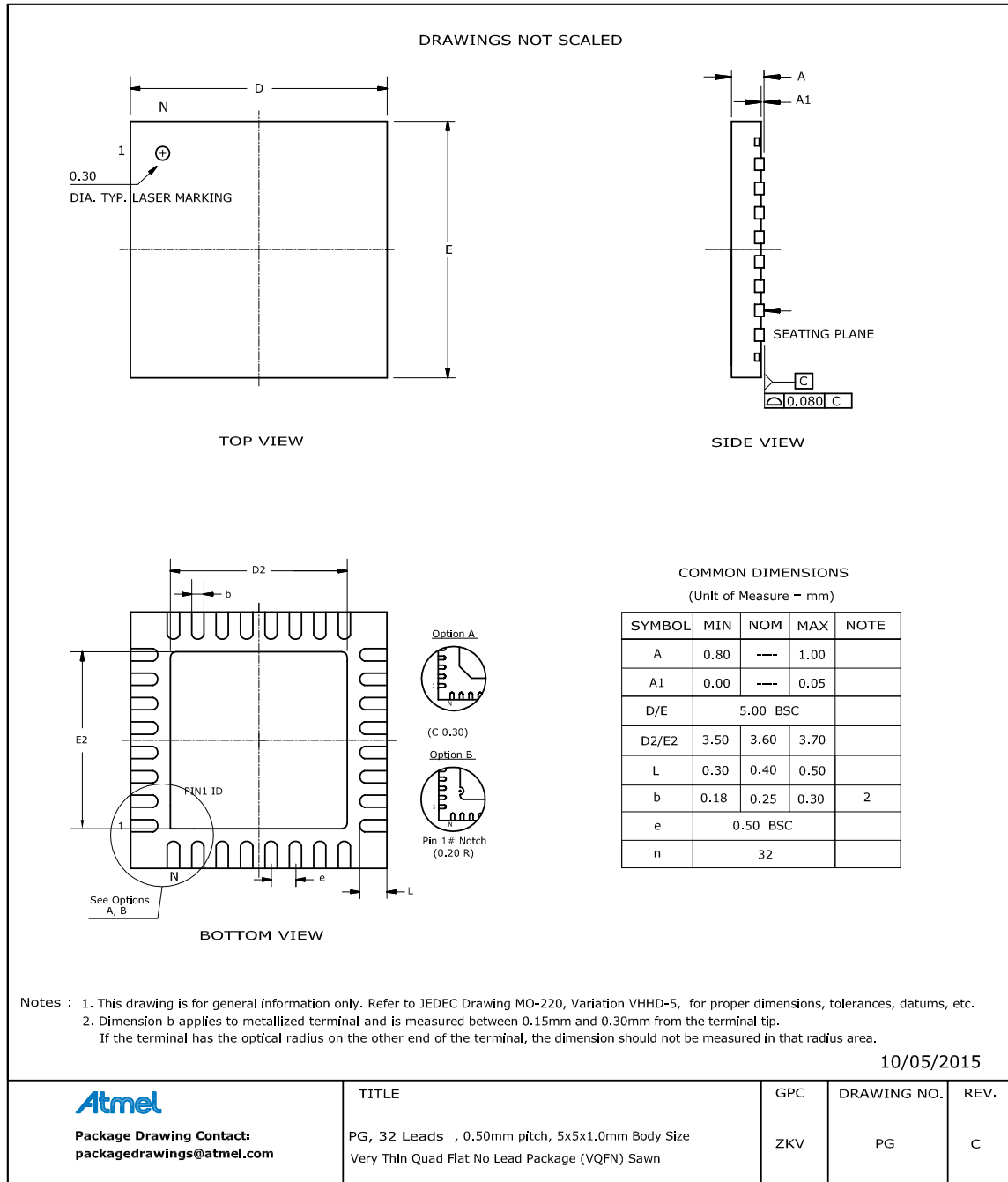
Table 8-19. Package Reference

| | |
|-------------------------|--------|
| JEDEC Drawing Reference | MO-220 |
| JESD97 Classification | E1 |

Table 8-22. Package Reference

| | |
|-------------------------|--------|
| JEDEC Drawing Reference | MS-026 |
| JESD97 Classification | E3 |

8.2.8. 32 pin QFN



Note: The exposed die attach pad is connected inside the device to GND and GNDANA.

Table 8-23. Device and Package Maximum Weight

| | |
|----|----|
| 90 | mg |
|----|----|