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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	26
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 10x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-VQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamd20e16a-mn

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAMD20E15A-AU	32K	4K	TQFP32	Tray
ATSAMD20E15A-AUT				Tape & Reel
ATSAMD20E15A-AN				Tray
ATSAMD20E15A-ANT				Tape & Reel
ATSAMD20E15A-MU			QFN32	Tray
ATSAMD20E15A-MUT				Tape & Reel
ATSAMD20E15A-MN				Tray
ATSAMD20E15A-MNT				Tape & Reel
ATSAMD20E16A-AU	64K	8K	TQFP32	Tray
ATSAMD20E16A-AUT				Tape & Reel
ATSAMD20E16A-AN				Tray
ATSAMD20E16A-AFT				Tape & Reel
ATSAMD20E16A-MU			QFN32	Tray
ATSAMD20E16A-MUT				Tape & Reel
ATSAMD20E16A-MN				Tray
ATSAMD20E16A-MNT				Tape & Reel
ATSAMD20E17A-AU	128K	16K	TQFP32	Tray
ATSAMD20E17A-AUT				Tape & Reel
ATSAMD20E17A-AN				Tray
ATSAMD20E17A-ANT				Tape & Reel
ATSAMD20E17A-MU			QFN32	Tray
ATSAMD20E17A-MUT				Tape & Reel
ATSAMD20E17A-MN				Tray
ATSAMD20E17A-MNT				Tape & Reel
ATSAMD20E18A-AU	256K	32K	TQFP32	Tray
ATSAMD20E18A-AUT				Tape & Reel
ATSAMD20E18A-AN				Tray
ATSAMD20E18A-AFT				Tape & Reel
ATSAMD20E18A-MU			QFN32	Tray
ATSAMD20E18A-MUT				Tape & Reel
ATSAMD20E18A-MN				Tray
ATSAMD20E18A-MNT				Tape & Reel

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAMD20G17A-AU	128K	16K	TQFP48	Tray
ATSAMD20G17A-AUT				Tape & Reel
ATSAMD20G17A-AN				Tray
ATSAMD20G17A-ANT				Tape & Reel
ATSAMD20G17A-MU			QFN48	Tray
ATSAMD20G17A-MUT				Tape & Reel
ATSAMD20G17A-MN				Tray
ATSAMD20G17A-MNT				Tape & Reel
ATSAMD20G17A-UUT			WLCSP45	Tape & Reel
ATSAMD20G18A-AU	256K	32K	TQFP48	Tray
ATSAMD20G18A-AUT				Tape & Reel
ATSAMD20G18A-AN				Tray
ATSAMD20G18A-ANT				Tape & Reel
ATSAMD20G18A-MU			QFN48	Tray
ATSAMD20G18A-MUT				Tape & Reel
ATSAMD20G18A-MN				Tray
ATSAMD20G18A-MNT				Tape & Reel
ATSAMD20G18A-UUT			WLCSP45	Tape & Reel

3.3. SAM D20J

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAMD20J14A-AU	16K	2K	TQFP64	Tray
ATSAMD20J14A-AUT				Tape & Reel
ATSAMD20J14A-AN				Tray
ATSAMD20J14A-ANT				Tape & Reel
ATSAMD20J14A-MU			QFN64	Tray
ATSAMD20J14A-MUT				Tape & Reel
ATSAMD20J14A-MN				Tray
ATSAMD20J14A-MNT				Tape & Reel

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAMD20J18A-AU	256K	32K	TQFP64	Tray
ATSAMD20J18A-AUT				Tape & Reel
ATSAMD20J18A-AN				Tray
ATSAMD20J18A-ANT				Tape & Reel
ATSAMD20J18A-MU			QFN64	Tray
ATSAMD20J18A-MUT				Tape & Reel
ATSAMD20J18A-MN				Tray
ATSAMD20J18A-MNT				Tape & Reel
ATSAMD20J18A-CU			UFBGA64	Tray
ATSAMD20J18A-CUT				Tape & Reel

3.4. Device Identification

The DSU - Device Service Unit peripheral provides the Device Selection bits in the Device Identification register (DID.DEVSEL) in order to identify the device by software. The device variants have a reset value of DID=0x1001drxx, with the LSB identifying the die number ('d'), the die revision ('r') and the device selection ('xx').

Table 3-1. Device Identification Values

Device Variant	DID.DEVSEL	Device ID (DID)
SAMD20J18C	0x00	0x10001300
SAMD20J18A	0x00	0x10001300
SAMD20J17A	0x01	0x10001301
SAMD20J16A	0x02	0x10001302
SAMD20J15A	0x03	0x10001303
SAMD20J14A	0x04	0x10001304
SAMD20G18A	0x05	0x10001305
SAMD20G17A	0x06	0x10001306
SAMD20G16A	0x07	0x10001307
SAMD20G15A	0x08	0x10001308
SAMD20G14A	0x09	0x10001309
SAMD20E18A	0x0A	0x1000130A
SAMD20E17A	0x0B	0x1000130B
SAMD20E16A	0x0C	0x1000130C
SAMD20E15A	0x0D	0x1000130D

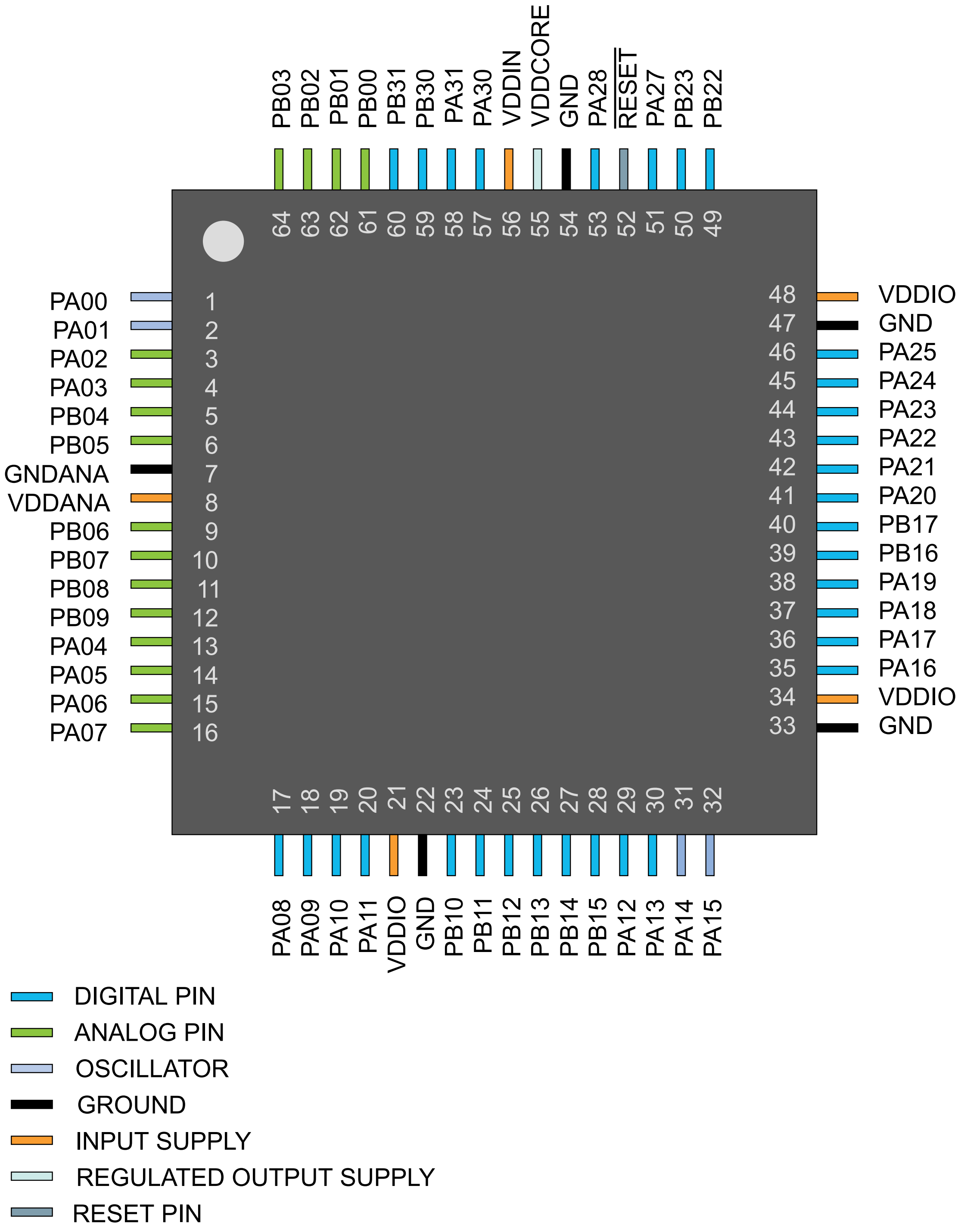
Device Variant	DID.DEVSEL	Device ID (DID)
SAMD20E14A	0x0E	0x1000130E
Reserved	0x0F	
SAMD20G18U	0x10	0x10001310
SAMD20G17U	0x11	0x10001311
Reserved	0x12 - 0xFF	

Note: The device variant (last letter of the ordering number) is independent of the die revision (DSU.DID.REVISION): The device variant denotes functional differences, whereas the die revision marks evolution of the die. The device variant denotes functional differences, whereas the die revision marks evolution of the die.

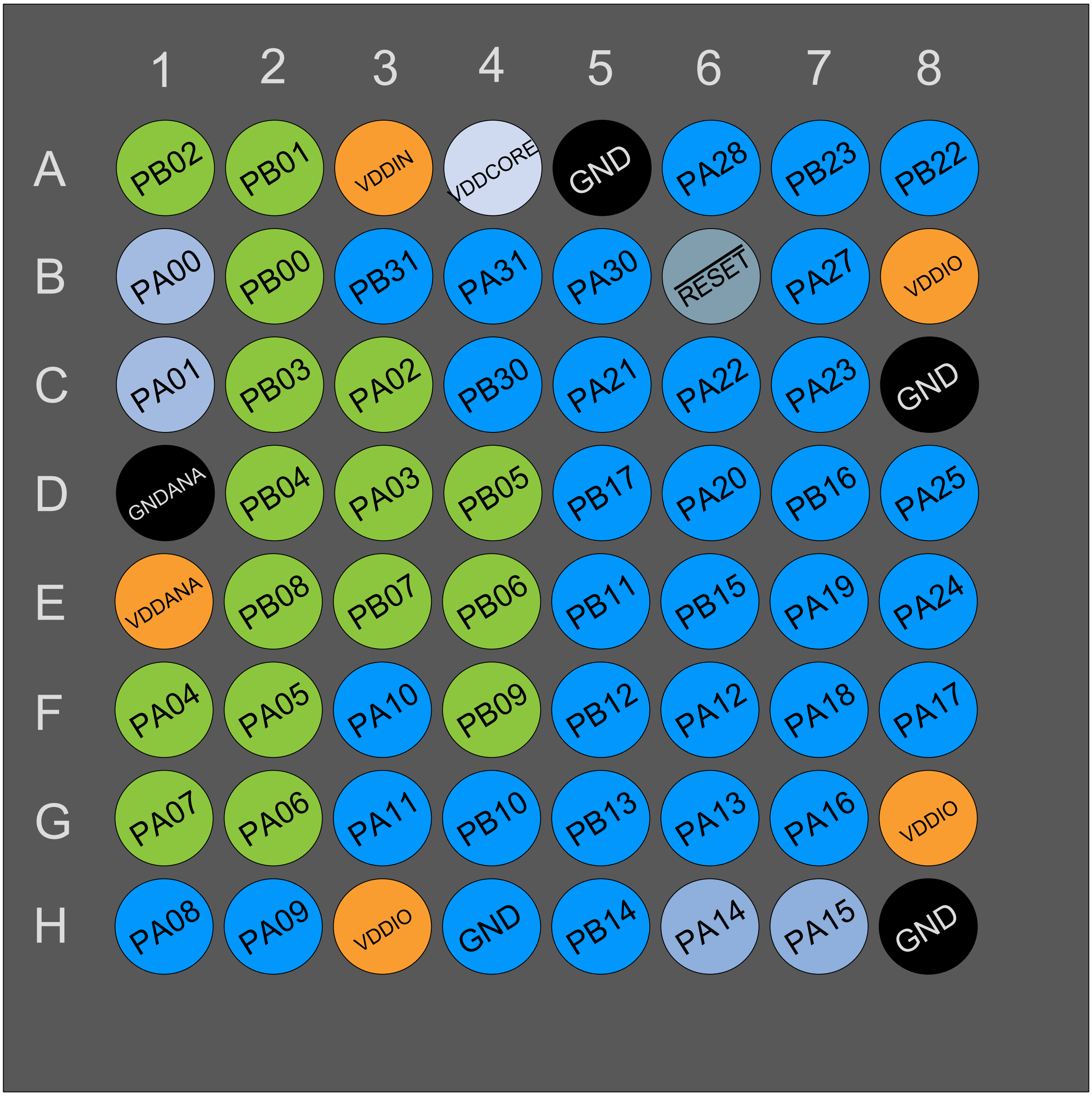
5. Pinout

5.1. SAM D20J

5.1.1. QFN64 / TQFP64



5.1.2. UFBGA64

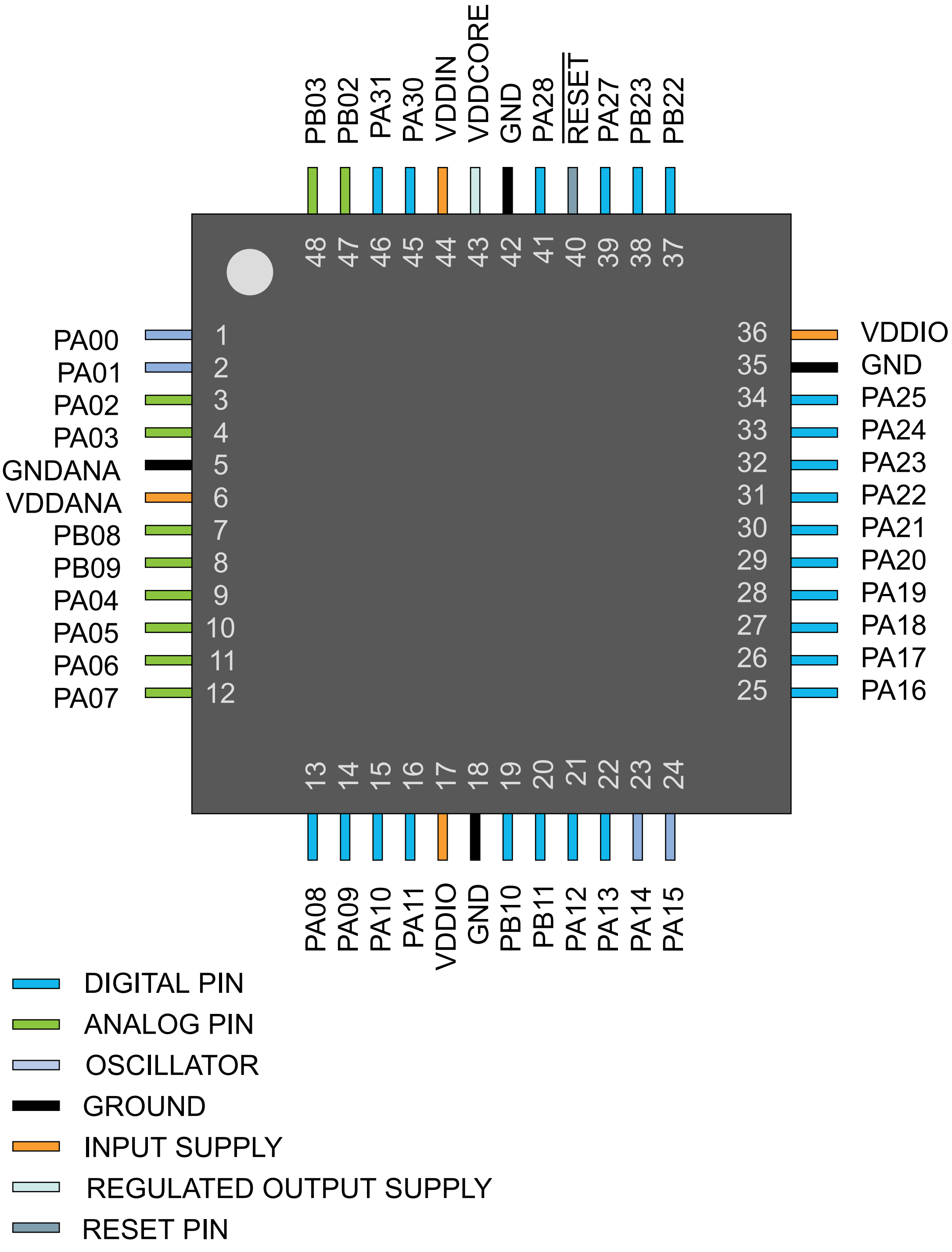


	1	2	3	4	5	6	7	8
A	PB02	PB01	VDDIN	VDDCORE	GND	PA28	PB23	PB22
B	PA00	PB00	PB31	PA31	PA30	RESET	PA27	VDDIO
C	PA01	PB03	PA02	PB30	PA21	PA22	PA23	GND
D	GNDANA	PB04	PA03	PB05	PB17	PA20	PB16	PA25
E	VDDANA	PB08	PB07	PB06	PB11	PB15	PA19	PA24
F	PA04	PA05	PA10	PB09	PB12	PA12	PA18	PA17
G	PA07	PA06	PA11	PB10	PB13	PA13	PA16	VDDIO
H	PA08	PA09	VDDIO	GND	PB14	PA14	PA15	GND

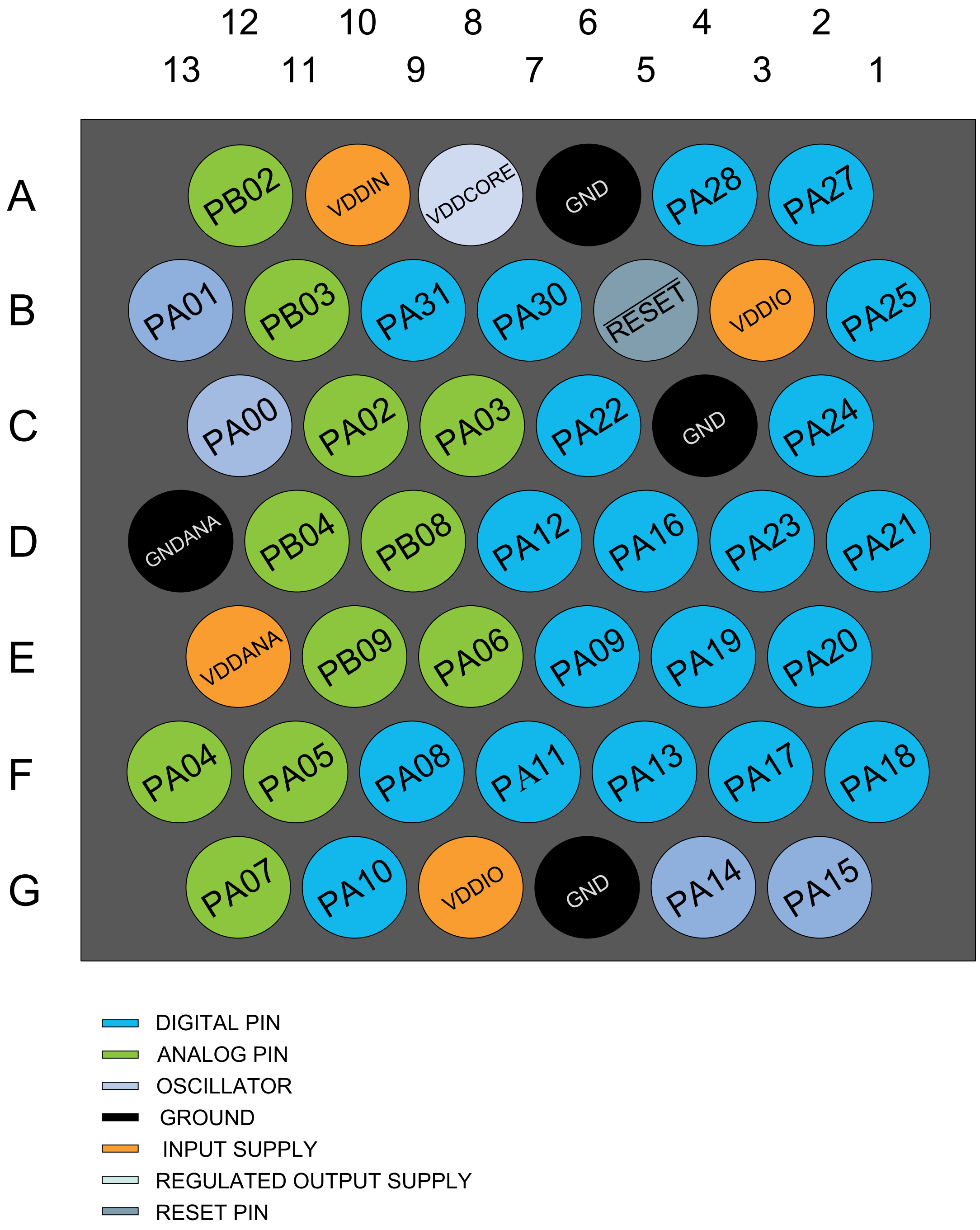
🟦 DIGITAL PIN
🟩 ANALOG PIN
▭ OSCILLATOR
▬ GROUND
🟧 INPUT SUPPLY
▭ REGULATED OUTPUT SUPPLY
▬ RESET PIN

5.2. SAM D20G

5.2.1. QFN48 / TQFP48

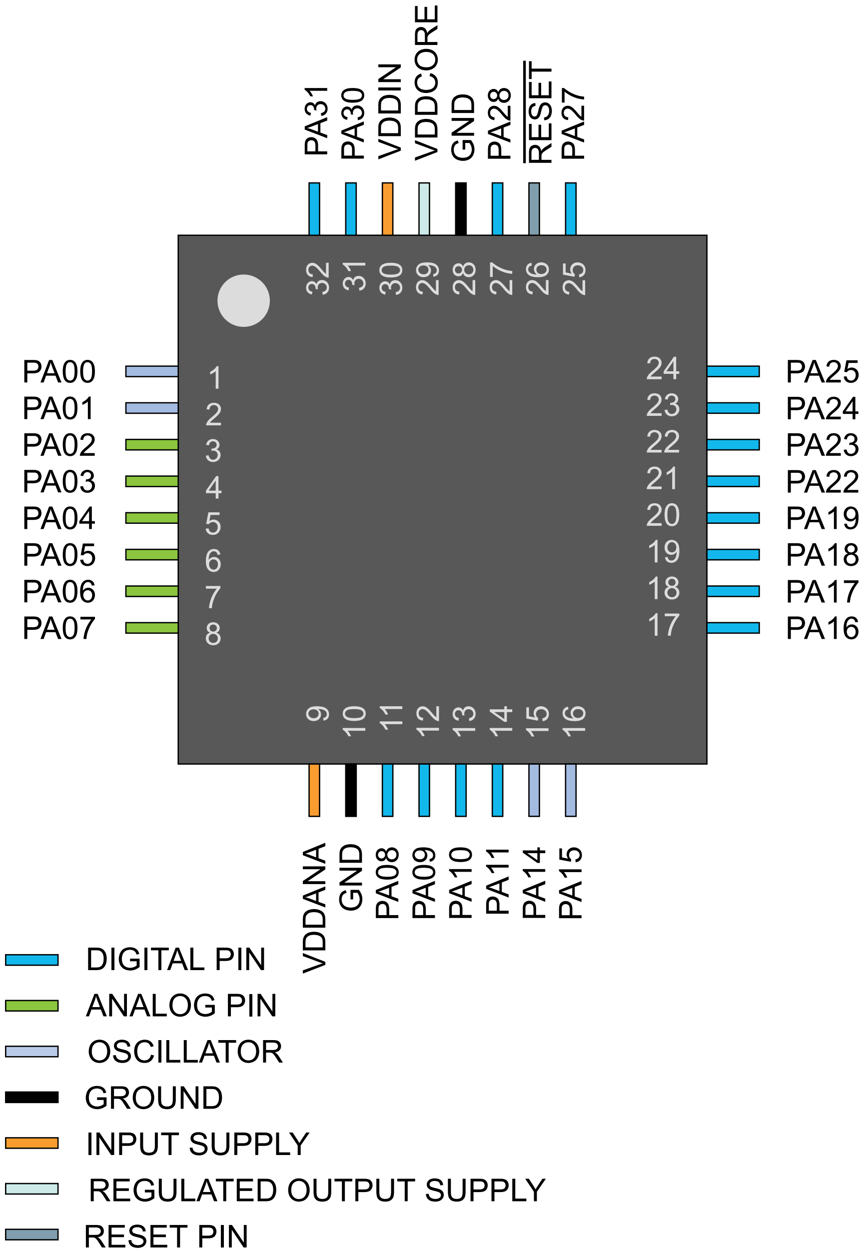


5.2.2. WLCSP45


12 10 8 6 4 2
13 11 9 7 5 3 1
A
PB02 VDDIN VDDCORE GND PA28 PA27
B
PA01 PB03 PA31 PA30 RESET VDDIO PA25
C
PA00 PA02 PA03 PA22 GND PA24
D
GNDANA PB04 PB08 PA12 PA16 PA23 PA21
E
VDDANA PB09 PA06 PA09 PA19 PA20
F
PA04 PA05 PA08 PA11 PA13 PA17 PA18
G
PA07 PA10 VDDIO GND PA14 PA15
DIGITAL PIN
ANALOG PIN
OSCILLATOR
GROUND
INPUT SUPPLY
REGULATED OUTPUT SUPPLY
RESET PIN

5.3. SAM D20E

5.3.1. QFN32 / TQFP32



(INTFLAG) register. The interrupt flag is set when the interrupt condition occurs. Each interrupt in the peripheral can be individually enabled by writing a one to the corresponding bit in the peripheral's Interrupt Enable Set (INTENSET) register, and disabled by writing a one to the corresponding bit in the peripheral's Interrupt Enable Clear (INTENCLR) register. An interrupt request is generated from the peripheral when the interrupt flag is set and the corresponding interrupt is enabled. The interrupt requests for one peripheral are ORed together on system level, generating one interrupt request for each peripheral. An interrupt request will set the corresponding interrupt pending bit in the NVIC interrupt pending registers (SETPEND/CLRPEND bits in ISPR/ICPR). For the NVIC to activate the interrupt, it must be enabled in the NVIC interrupt enable register (SETENA/CLRENA bits in ISER/ICER). The NVIC interrupt priority registers IPR0-IPR7 provide a priority field for each interrupt.

Table 7-3. Interrupt Line Mapping

Peripheral Source	NVIC Line
EIC NMI – External Interrupt Controller	NMI
PM – Power Manager	0
SYSCTRL – System Control	1
WDT – Watchdog Timer	2
RTC – Real Time Counter	3
EIC – External Interrupt Controller	4
NVMCTRL – Non-Volatile Memory Controller	5
EVSYS – Event System	6
SERCOM0 – Serial Communication Interface 0	7
SERCOM1 – Serial Communication Interface 1	8
SERCOM2 – Serial Communication Interface 2	9
SERCOM3 – Serial Communication Interface 3	10
SERCOM4 – Serial Communication Interface 4	11
SERCOM5 – Serial Communication Interface 5	12
TC0 – Timer Counter 0	13
TC1 – Timer Counter 1	14
TC2 – Timer Counter 2	15
TC3 – Timer Counter 3	16
TC4 – Timer Counter 4	17
TC5 – Timer Counter 5	18
TC6 – Timer Counter 6	19
TC7 – Timer Counter 7	20
ADC – Analog-to-Digital Converter	21
AC – Analog Comparator	22

Peripheral Source	NVIC Line
DAC – Digital-to-Analog Converter	23
PTC – Peripheral Touch Controller	24

7.3. Micro Trace Buffer

7.3.1. Features

- Program flow tracing for the Cortex-M0+ processor
- MTB SRAM can be used for both trace and general purpose storage by the processor
- The position and size of the trace buffer in SRAM is configurable by software
- CoreSight compliant

7.3.2. Overview

When enabled, the MTB records changes in program flow, reported by the Cortex-M0+ processor over the execution trace interface shared between the Cortex-M0+ processor and the CoreSight MTB-M0+. This information is stored as trace packets in the SRAM by the MTB. An off-chip debugger can extract the trace information using the Debug Access Port to read the trace information from the SRAM. The debugger can then reconstruct the program flow from this information.

The MTB simultaneously stores trace information into the SRAM, and gives the processor access to the SRAM. The MTB ensures that trace write accesses have priority over processor accesses.

The execution trace packet consists of a pair of 32-bit words that the MTB generates when it detects the processor PC value changes non-sequentially. A non-sequential PC change can occur during branch instructions or during exception entry. See the CoreSight MTB-M0+ Technical Reference Manual for more details on the MTB execution trace packet format.

Tracing is enabled when the MASTER.EN bit in the Master Trace Control Register is 1. There are various ways to set the bit to 1 to start tracing, or to 0 to stop tracing. See the CoreSight Cortex-M0+ Technical Reference Manual for more details on the Trace start and stop and for a detailed description of the MTB's MASTER register. The MTB can be programmed to stop tracing automatically when the memory fills to a specified watermark level or to start or stop tracing by writing directly to the MASTER.EN bit. If the watermark mechanism is not being used and the trace buffer overflows, then the buffer wraps around overwriting previous trace packets.

The base address of the MTB registers is 0x41006000; this address is also written in the CoreSight ROM Table. The offset of each register from the base address is fixed and as defined by the CoreSight MTB-M0+ Technical Reference Manual. The MTB has 4 programmable registers to control the behavior of the trace features:

- POSITION: Contains the trace write pointer and the wrap bit,
- MASTER: Contains the main trace enable bit and other trace control fields,
- FLOW: Contains the WATERMARK address and the AUTOSTOP and AUTOHALT control bits,
- BASE: Indicates where the SRAM is located in the processor memory map. This register is provided to enable auto discovery of the MTB SRAM location, by a debug agent.

See the CoreSight MTB-M0+ Technical Reference Manual for a detailed description of these registers.

7.4. High-Speed Bus System

7.4.1. Features

High-Speed Bus Matrix has the following features:

- Symmetric crossbar bus switch implementation
- Allows concurrent accesses from different masters to different slaves
- 32-bit data bus
- Operation at a one-to-one clock frequency with the bus masters

7.4.2. Configuration

Table 7-4. Bus Matrix Masters

Bus Matrix Masters	Master ID
CM0+ - Cortex M0+ Processor	0
DSU - Device Service Unit	1

Table 7-5. Bus Matrix Slaves

Bus Matrix Slaves	Slave ID
Internal Flash Memory	0
AHB-APB Bridge A	1
AHB-APB Bridge B	2
AHB-APB Bridge C	3

7.5. AHB-APB Bridge

The AHB-APB bridge is an AHB slave, providing an interface between the high-speed AHB domain and the low-power APB domain. It is used to provide access to the programmable control registers of peripherals (see *Product Mapping*).

AHB-APB bridge is based on AMBA APB Protocol Specification V2.0 (ref. as APB4) including:

- Wait state support
- Error reporting
- Transaction protection
- Sparse data transfer (byte, half-word and word)

Additional enhancements:

- Address and data cycles merged into a single cycle
- Sparse data transfer also apply to read access

to operate the AHB-APB bridge, the clock (CLK_HPBx_AHB) must be enabled. See *PM – Power Manager* for details.

Write-protect registers allow the user to disable a selected peripheral’s write-protection without doing a read-modify-write operation. These registers are mapped into two I/O memory locations, one for clearing and one for setting the register bits. Writing a one to a bit in the Write Protect Clear register (WPCLR) will clear the corresponding bit in both registers (WPCLR and WPSET) and disable the write-protection for the corresponding peripheral, while writing a one to a bit in the Write Protect Set (WPSET) register will set the corresponding bit in both registers (WPCLR and WPSET) and enable the write-protection for the corresponding peripheral. Both registers (WPCLR and WPSET) will return the same value when read.

If a peripheral is write-protected, and if a write access is performed, data will not be written, and the peripheral will return an access error (CPU exception).

The PAC also offers a safety feature for correct program execution, with a CPU exception generated on double write-protection or double unprotection of a peripheral. If a peripheral n is write-protected and a write to one in WPSET[n] is detected, the PAC returns an error. This can be used to ensure that the application follows the intended program flow by always following a write-protect with an unprotect, and vice versa. However, in applications where a write-protected peripheral is used in several contexts, e.g., interrupts, care should be taken so that either the interrupt can not happen while the main application or other interrupt levels manipulate the write-protection status, or when the interrupt handler needs to unprotect the peripheral, based on the current protection status, by reading WPSET.

7.7. Register Description

Atomic 8-, 16- and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly. Refer to the Product Mapping for PAC locations.

Related Links

Product Mapping on page 19

7.7.1. PAC0 Register Description

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 3 – GCLK
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 2 – SYSCTRL
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 1 – PM
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 3 – GCLK
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 2 – SYSCTRL
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 1 – PM
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

7.7.2. PAC1 Register Description

8. Packaging Information

8.1. Thermal Considerations

Related Links

Junction Temperature on page 39

8.1.1. Thermal Resistance Data

The following *table* summarizes the thermal resistance data depending on the package.

Table 8-1. Thermal Resistance Data

Package Type	θ_{JA}	θ_{JC}
32-pin TQFP	68.0°C/W	25.8°C/W
48-pin TQFP	78.8°C/W	12.3°C/W
64-pin TQFP	66.7°C/W	11.9°C/W
32-pin QFN	37.2°C/W	13.1°C/W
48-pin QFN	33.0°C/W	11.4°C/W
64-pin QFN	33.5°C/W	11.2°C/W
64-ball UFBGA	67.4°C/W	12.4°C/W
45-ball WLCSP	37.0°C/W	0.36°C/W

8.1.2. Junction Temperature

The average chip-junction temperature, T_J, in °C can be obtained from the following:

1. $T_J = T_A + (P_D \times \theta_{JA})$
2. $T_J = T_A + (P_D \times (\theta_{HEATSINK} + \theta_{JC}))$

where:

- θ_{JA} = Package thermal resistance, Junction-to-ambient (°C/W), see Thermal Resistance Data
- θ_{JC} = Package thermal resistance, Junction-to-case thermal resistance (°C/W), see Thermal Resistance Data
- $\theta_{HEATSINK}$ = Thermal resistance (°C/W) specification of the external cooling device
- P_D = Device power consumption (W)
- T_A = Ambient temperature (°C)

From the first equation, the user can derive the estimated lifetime of the chip and decide if a cooling device is necessary or not. If a cooling device is to be fitted on the chip, the second equation should be used to compute the resulting average chip-junction temperature T_J in °C.

Related Links

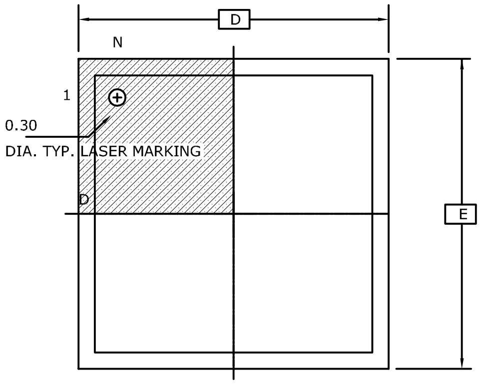
Thermal Considerations on page 39

Table 8-4. Package Reference

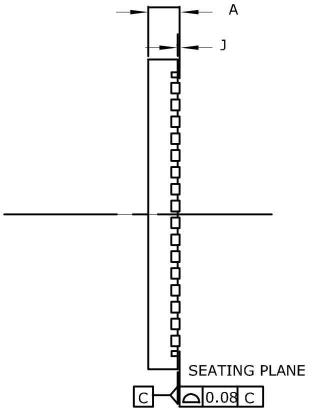
JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

8.2.2. 64 pin QFN

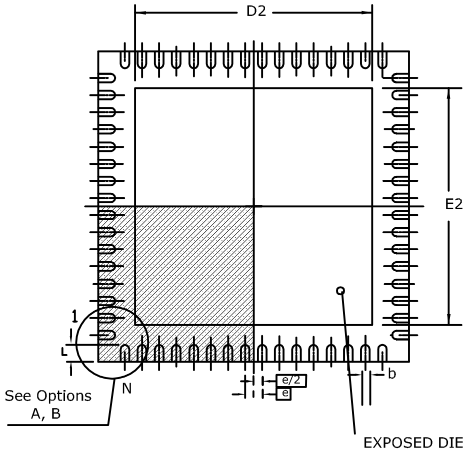
DRAWINGS NOT SCALED



TOP VIEW



SIDE VIEW

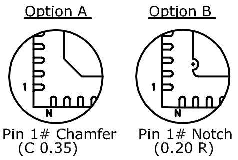


BOTTOM VIEW

COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	-----	1.00	
D/E	9.00 BSC			
D2/E2	4.60	4.70	4.80	
J	0.00	-----	0.05	
b	0.15	0.20	0.25	
e	0.50 BSC			
L	0.30	0.40	0.55	
N	64			



Pin 1# Chamfer (C 0.35)

Pin 1# Notch (0.20 R)

Notes : 1. This drawing is for general information only. Refer to JEDEC Drawing MO-220, Variation VMMD-4, for proper dimensions, tolerances, datums, etc.
2. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optical radius on the other end of the terminal, the dimension should not be measured in that radius area.

05/27/2011

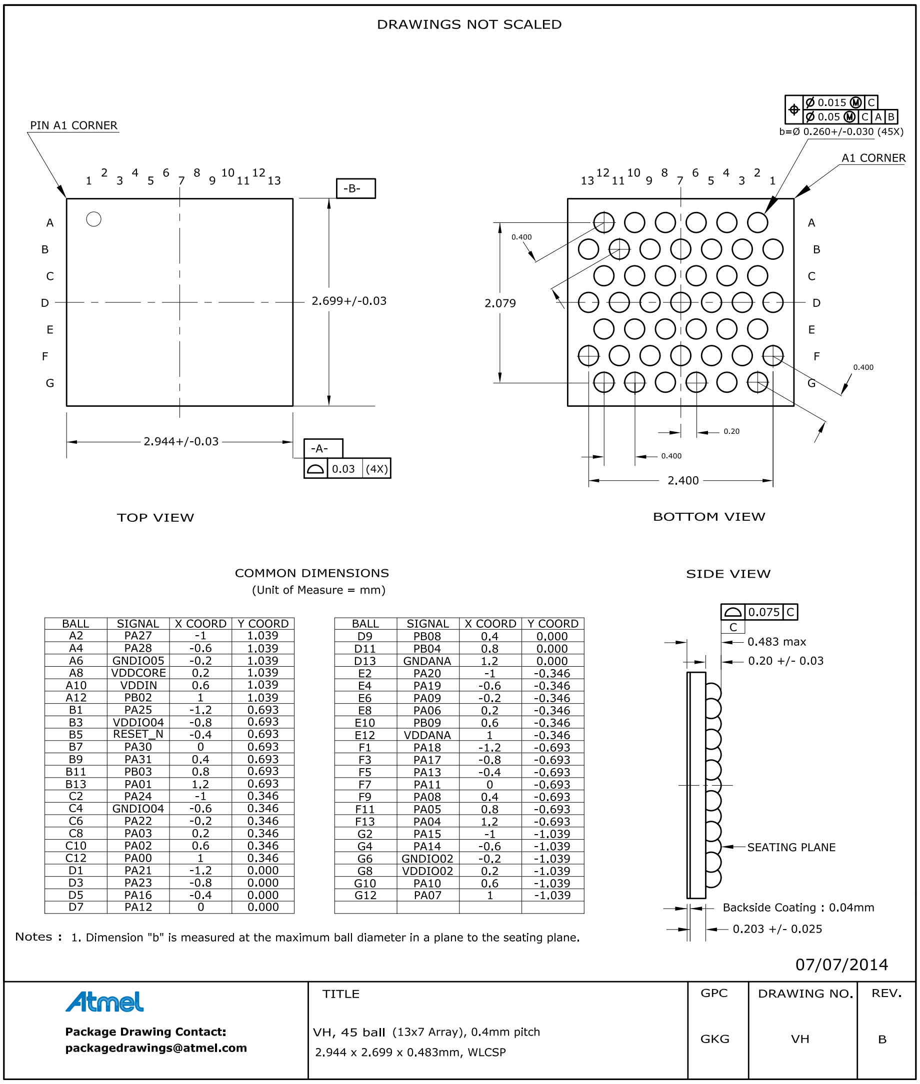
	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: **packagedrawings@atmel.com**	PA, 64 Leads , 0.50 mm pitch, 9 x 9 x 1 mm Very Thin Quad Flat No Lead Package (VQFN) Sawn	ZST	PA	A

Note: The exposed die attach pad is not connected electrically inside the device.

Table 8-16. Package Reference

JEDEC Drawing Reference	MO-220
JESD97 Classification	E3

8.2.6. 45-ball WLCSP



COMMON DIMENSIONS
(Unit of Measure = mm)

BALL	SIGNAL	X COORD	Y COORD
A2	PA27	-1	1.039
A4	PA28	-0.6	1.039
A6	GNDIO05	-0.2	1.039
A8	VDDCORE	0.2	1.039
A10	VDDIN	0.6	1.039
A12	PB02	1	1.039
B1	PA25	-1.2	0.693
B3	VDDIO04	-0.8	0.693
B5	RESET_N	-0.4	0.693
B7	PA30	0	0.693
B9	PA31	0.4	0.693
B11	PB03	0.8	0.693
B13	PA01	1.2	0.693
C2	PA24	-1	0.346
C4	GNDIO04	-0.6	0.346
C6	PA22	-0.2	0.346
C8	PA03	0.2	0.346
C10	PA02	0.6	0.346
C12	PA00	1	0.346
D1	PA21	-1.2	0.000
D3	PA23	-0.8	0.000
D5	PA16	-0.4	0.000
D7	PA12	0	0.000

BALL	SIGNAL	X COORD	Y COORD
D9	PB08	0.4	0.000
D11	PB04	0.8	0.000
D13	GNDANA	1.2	0.000
E2	PA20	-1	-0.346
E4	PA19	-0.6	-0.346
E6	PA09	-0.2	-0.346
E8	PA06	0.2	-0.346
E10	PB09	0.6	-0.346
E12	VDDANA	1	-0.346
F1	PA18	-1.2	-0.693
F3	PA17	-0.8	-0.693
F5	PA13	-0.4	-0.693
F7	PA11	0	-0.693
F9	PA08	0.4	-0.693
F11	PA05	0.8	-0.693
F13	PA04	1.2	-0.693
G2	PA15	-1	-1.039
G4	PA14	-0.6	-1.039
G6	GNDIO02	-0.2	-1.039
G8	VDDIO02	0.2	-1.039
G10	PA10	0.6	-1.039
G12	PA07	1	-1.039

Notes : 1. Dimension "b" is measured at the maximum ball diameter in a plane to the seating plane.

07/07/2014

	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: **packagedrawings@atmel.com**	VH, 45 ball (13x7 Array), 0.4mm pitch 2.944 x 2.699 x 0.483mm, WLCSP	GKG	VH	B

Table 8-17. Device and Package Maximum Weight

7.3	mg

Table 8-18. Package Characteristics

Moisture Sensitivity Level	MSL1

Table 8-19. Package Reference

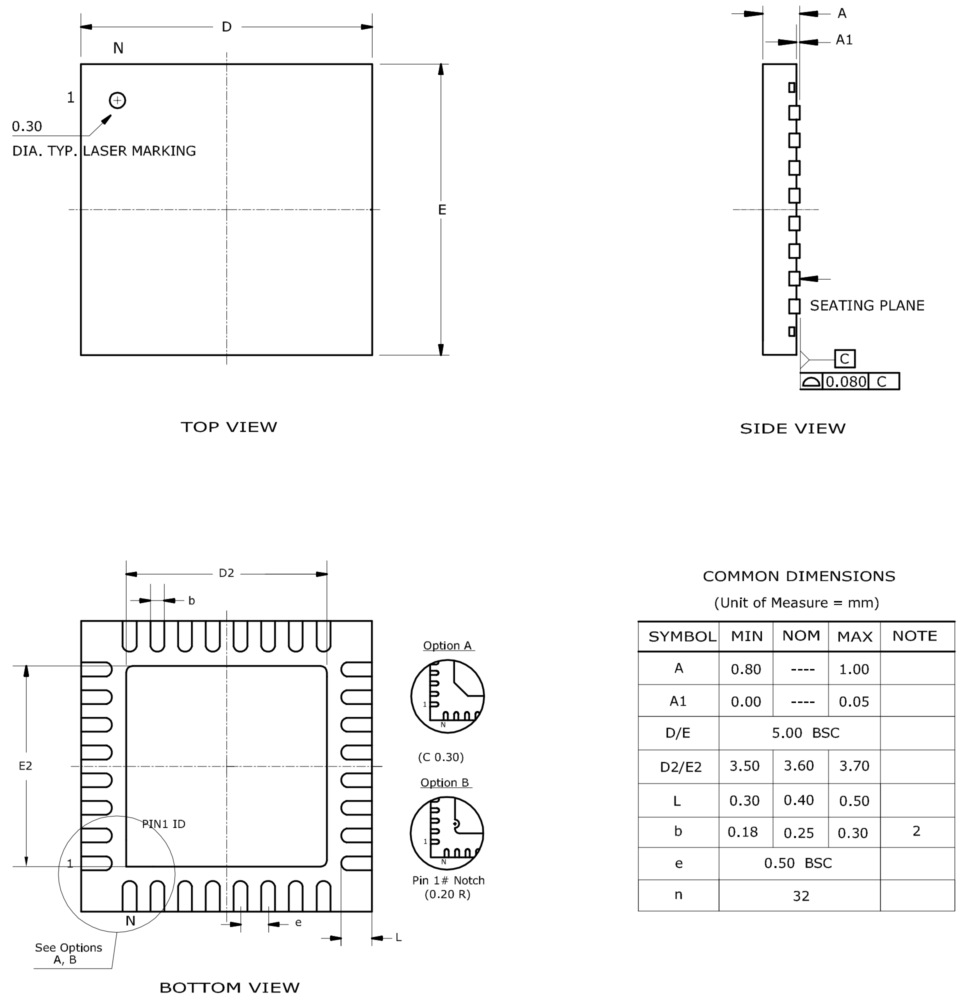
JEDEC Drawing Reference	MO-220
JESD97 Classification	E1

Table 8-22. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

8.2.8. 32 pin QFN

DRAWINGS NOT SCALED



COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	----	1.00	
A1	0.00	----	0.05	
D/E	5.00 BSC			
D2/E2	3.50	3.60	3.70	
L	0.30	0.40	0.50	
b	0.18	0.25	0.30	2
e	0.50 BSC			
n	32			

Notes :
1. This drawing is for general information only. Refer to JEDEC Drawing MO-220, Variation VHHD-5, for proper dimensions, tolerances, datums, etc.
2. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optical radius on the other end of the terminal, the dimension should not be measured in that radius area.

10/05/2015

	TITLE	GPC	DRAWING NO.	REV.
Atmel **Package Drawing Contact:** **packagedrawings@atmel.com**	PG, 32 Leads , 0.50mm pitch, 5x5x1.0mm Body Size Very Thin Quad Flat No Lead Package (VQFN) Sawn	ZKV	PG	C

Note: The exposed die attach pad is connected inside the device to GND and GNDANA.

Table 8-23. Device and Package Maximum Weight

90	mg

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