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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	38
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 14x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamd20g15a-aut

1. Description

The Atmel® | SMART™ SAM D20 is a series of low-power microcontrollers using the 32-bit ARM® Cortex®-M0+ processor, and ranging from 32- to 64-pins with up to 256KB Flash and 32KB of SRAM. The SAM D20 devices operate at a maximum frequency of 48MHz and reach 2.46 CoreMark/MHz. They are designed for simple and intuitive migration with identical peripheral modules, hex compatible code, identical linear address map and pin compatible migration paths between all devices in the product series. All devices include intelligent and flexible peripherals, Atmel Event System for inter-peripheral signaling, and support for capacitive touch button, slider and wheel user interfaces.

The SAM D20 devices provide the following features: In-system programmable Flash, eight-channel Event System, programmable interrupt controller, up to 52 programmable I/O pins, 32-bit real-time clock and calendar, up to eight 16-bit Timer/Counters (TC) . The timer/counters can be configured to perform frequency and waveform generation, accurate program execution timing or input capture with time and frequency measurement of digital signals. The TCs can operate in 8- or 16-bit mode, selected TCs can be cascaded to form a 32-bit TC. The series provide up to six Serial Communication Modules (SERCOM) that each can be configured to act as an USART, UART, SPI, I²C up to 400kHz, up to twenty-channel 350ksps 12-bit ADC with programmable gain and optional oversampling and decimation supporting up to 16-bit resolution, one 10-bit 350ksps DAC, two analog comparators with window mode, Peripheral Touch Controller supporting up to 256 buttons, sliders, wheels and proximity sensing; programmable Watchdog Timer, brown-out detector and power-on reset and two-pin Serial Wire Debug (SWD) program and debug interface.

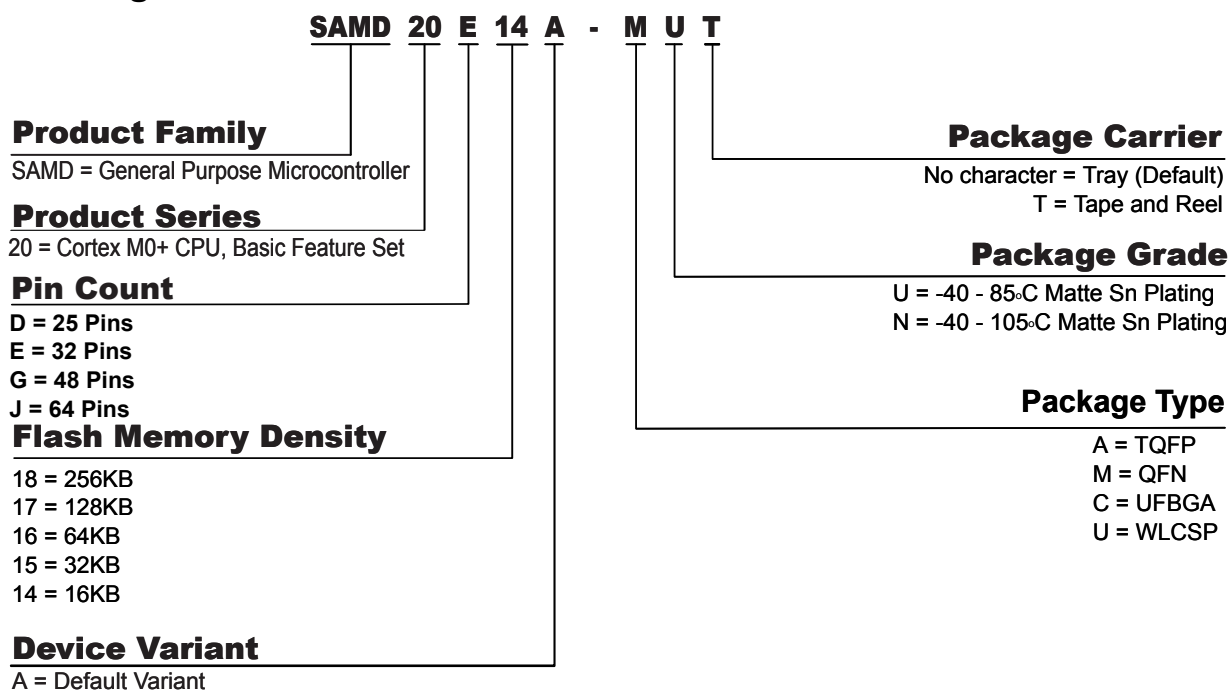
All devices have accurate and low-power external and internal oscillators. All oscillators can be used as a source for the system clock. Different clock domains can be independently configured to run at different frequencies, enabling power saving by running each peripheral at its optimal clock frequency, and thus maintaining a high CPU frequency while reducing power consumption.

The SAM D20 devices have two software-selectable sleep modes, idle and standby. In idle mode the CPU is stopped while all other functions can be kept running. In standby all clocks and functions are stopped except those selected to continue running. The device supports SleepWalking. This feature allows the peripheral to wake up from sleep based on predefined conditions, and thus allows the CPU to wake up only when needed, e.g. when a threshold is crossed or a result is ready. The Event System supports synchronous and asynchronous events, allowing peripherals to receive, react to and send events even in standby mode.

The Flash program memory can be reprogrammed in-system through the SWD interface. The same interface can be used for non-intrusive on-chip debug of application code. A boot loader running in the device can use any communication interface to download and upgrade the application program in the Flash memory.

The SAM D20 devices are supported with a full suite of program and system development tools, including C compilers, macro assemblers, program debugger/simulators, programmers and evaluation kits.

3. Ordering Information



3.1. SAM D20E

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAMD20E14A-AU	16K	2K	TQFP32	Tray
ATSAMD20E14A-AUT				Tape & Reel
ATSAMD20E14A-AN				Tray
ATSAMD20E14A-ANT				Tape & Reel
ATSAMD20E14A-MU			QFN32	Tray
ATSAMD20E14A-MUT				Tape & Reel
ATSAMD20E14A-MN				Tray
ATSAMD20E14A-MNT				Tape & Reel

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAMD20E15A-AU	32K	4K	TQFP32	Tray
ATSAMD20E15A-AUT				Tape & Reel
ATSAMD20E15A-AN				Tray
ATSAMD20E15A-ANT				Tape & Reel
ATSAMD20E15A-MU			QFN32	Tray
ATSAMD20E15A-MUT				Tape & Reel
ATSAMD20E15A-MN				Tray
ATSAMD20E15A-MNT				Tape & Reel
ATSAMD20E16A-AU	64K	8K	TQFP32	Tray
ATSAMD20E16A-AUT				Tape & Reel
ATSAMD20E16A-AN				Tray
ATSAMD20E16A-AFT				Tape & Reel
ATSAMD20E16A-MU			QFN32	Tray
ATSAMD20E16A-MUT				Tape & Reel
ATSAMD20E16A-MN				Tray
ATSAMD20E16A-MNT				Tape & Reel
ATSAMD20E17A-AU	128K	16K	TQFP32	Tray
ATSAMD20E17A-AUT				Tape & Reel
ATSAMD20E17A-AN				Tray
ATSAMD20E17A-ANT				Tape & Reel
ATSAMD20E17A-MU			QFN32	Tray
ATSAMD20E17A-MUT				Tape & Reel
ATSAMD20E17A-MN				Tray
ATSAMD20E17A-MNT				Tape & Reel
ATSAMD20E18A-AU	256K	32K	TQFP32	Tray
ATSAMD20E18A-AUT				Tape & Reel
ATSAMD20E18A-AN				Tray
ATSAMD20E18A-AFT				Tape & Reel
ATSAMD20E18A-MU			QFN32	Tray
ATSAMD20E18A-MUT				Tape & Reel
ATSAMD20E18A-MN				Tray
ATSAMD20E18A-MNT				Tape & Reel

3.2. SAM D20G

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAMD20G14A-AU	16K	2K	TQFP32	Tray
ATSAMD20G14A-AUT				Tape & Reel
ATSAMD20G14A-AN				Tray
ATSAMD20G14A-ANT				Tape & Reel
ATSAMD20G14A-MU			QFN32	Tray
ATSAMD20G14A-MUT				Tape & Reel
ATSAMD20G14A-MN				Tray
ATSAMD20G14A-MNT				Tape & Reel
ATSAMD20G15A-AU	32K	4K	TQFP48	Tray
ATSAMD20G15A-AUT				Tape & Reel
ATSAMD20G15A-AN				Tray
ATSAMD20G15A-ANT				Tape & Reel
ATSAMD20G15A-MU			QFN48	Tray
ATSAMD20G15A-MUT				Tape & Reel
ATSAMD20G15A-MN				Tray
ATSAMD20G15A-MNT				Tape & Reel
ATSAMD20G16A-AU	64K	8K	TQFP48	Tray
ATSAMD20G16A-AUT				Tape & Reel
ATSAMD20G16A-AN				Tray
ATSAMD20G16A-ANT				Tape & Reel
ATSAMD20G16A-MU			QFN48	Tray
ATSAMD20G16A-MUT				Tape & Reel
ATSAMD20G16A-MN				Tray
ATSAMD20G16A-MNT				Tape & Reel

Device Variant	DID.DEVSEL	Device ID (DID)
SAMD20E14A	0x0E	0x1000130E
Reserved	0x0F	
SAMD20G18U	0x10	0x10001310
SAMD20G17U	0x11	0x10001311
Reserved	0x12 - 0xFF	

Note: The device variant (last letter of the ordering number) is independent of the die revision (DSU.DID.REVISION): The device variant denotes functional differences, whereas the die revision marks evolution of the die. The device variant denotes functional differences, whereas the die revision marks evolution of the die.

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13

(INTFLAG) register. The interrupt flag is set when the interrupt condition occurs. Each interrupt in the peripheral can be individually enabled by writing a one to the corresponding bit in the peripheral's Interrupt Enable Set (INTENSET) register, and disabled by writing a one to the corresponding bit in the peripheral's Interrupt Enable Clear (INTENCLR) register. An interrupt request is generated from the peripheral when the interrupt flag is set and the corresponding interrupt is enabled. The interrupt requests for one peripheral are ORed together on system level, generating one interrupt request for each peripheral. An interrupt request will set the corresponding interrupt pending bit in the NVIC interrupt pending registers (SETPEND/CLRPEND bits in ISPR/ICPR). For the NVIC to activate the interrupt, it must be enabled in the NVIC interrupt enable register (SETENA/CLRENA bits in ISER/ICER). The NVIC interrupt priority registers IPR0-IPR7 provide a priority field for each interrupt.

Table 7-3. Interrupt Line Mapping

Peripheral Source	NVIC Line
EIC NMI – External Interrupt Controller	NMI
PM – Power Manager	0
SYSCTRL – System Control	1
WDT – Watchdog Timer	2
RTC – Real Time Counter	3
EIC – External Interrupt Controller	4
NVMCTRL – Non-Volatile Memory Controller	5
EVSYS – Event System	6
SERCOM0 – Serial Communication Interface 0	7
SERCOM1 – Serial Communication Interface 1	8
SERCOM2 – Serial Communication Interface 2	9
SERCOM3 – Serial Communication Interface 3	10
SERCOM4 – Serial Communication Interface 4	11
SERCOM5 – Serial Communication Interface 5	12
TC0 – Timer Counter 0	13
TC1 – Timer Counter 1	14
TC2 – Timer Counter 2	15
TC3 – Timer Counter 3	16
TC4 – Timer Counter 4	17
TC5 – Timer Counter 5	18
TC6 – Timer Counter 6	19
TC7 – Timer Counter 7	20
ADC – Analog-to-Digital Converter	21
AC – Analog Comparator	22

Figure 7-1. APB Write Access.

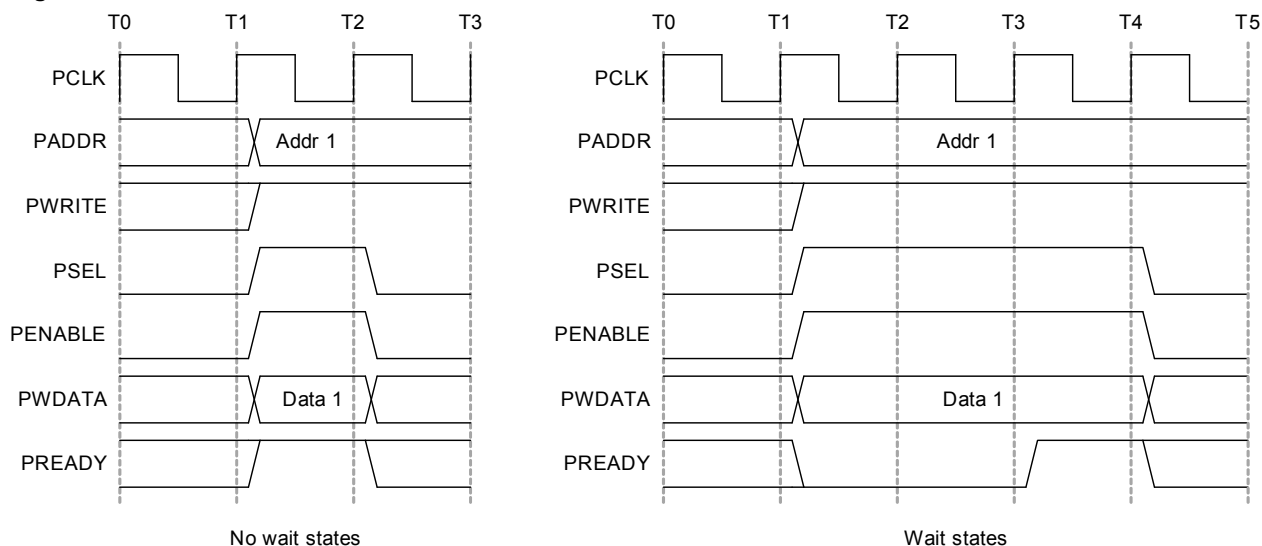
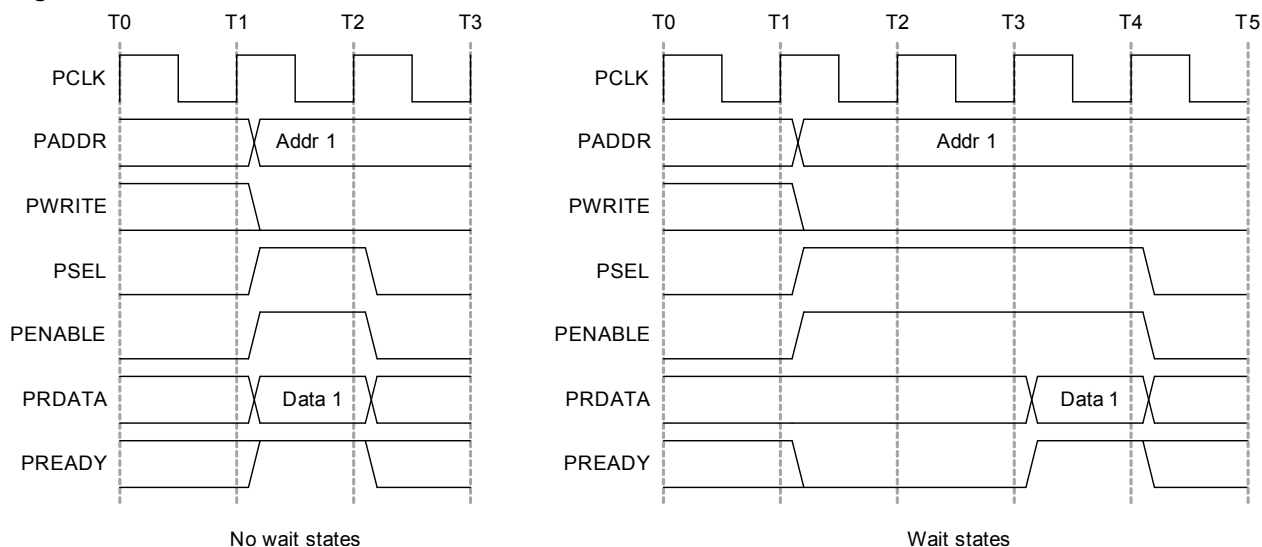


Figure 7-2. APB Read Access.



Related Links

[Product Mapping](#) on page 19

7.6. PAC - Peripheral Access Controller

7.6.1. Overview

There is one PAC associated with each AHB-APB bridge. The PAC can provide write protection for registers of each peripheral connected on the same bridge.

The PAC peripheral bus clock (CLK_PACx_APB) can be enabled and disabled in the Power Manager. CLK_PAC0_APB and CLK_PAC1_APB are enabled at reset. CLK_PAC2_APB is disabled at reset. Refer to *PM – Power Manager* for details. The PAC will continue to operate in any sleep mode where the selected clock source is running. Write-protection does not apply for debugger access. When the debugger makes an access to a peripheral, write-protection is ignored so that the debugger can update the register.

7.7.1.2. Write Protect Set

Name: WPSET
Offset: 0x04
Reset: 0x000000
Property: –

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access								
Reset								
Bit	7	6	5	4	3	2	1	0
		EIC	RTC	WDT	GCLK	SYSCTRL	PM	
Access		R/W	R/W	R/W	R/W	R/W	R/W	
Reset		0	0	0	0	0	0	

Bit 6 – EIC

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 5 – RTC

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

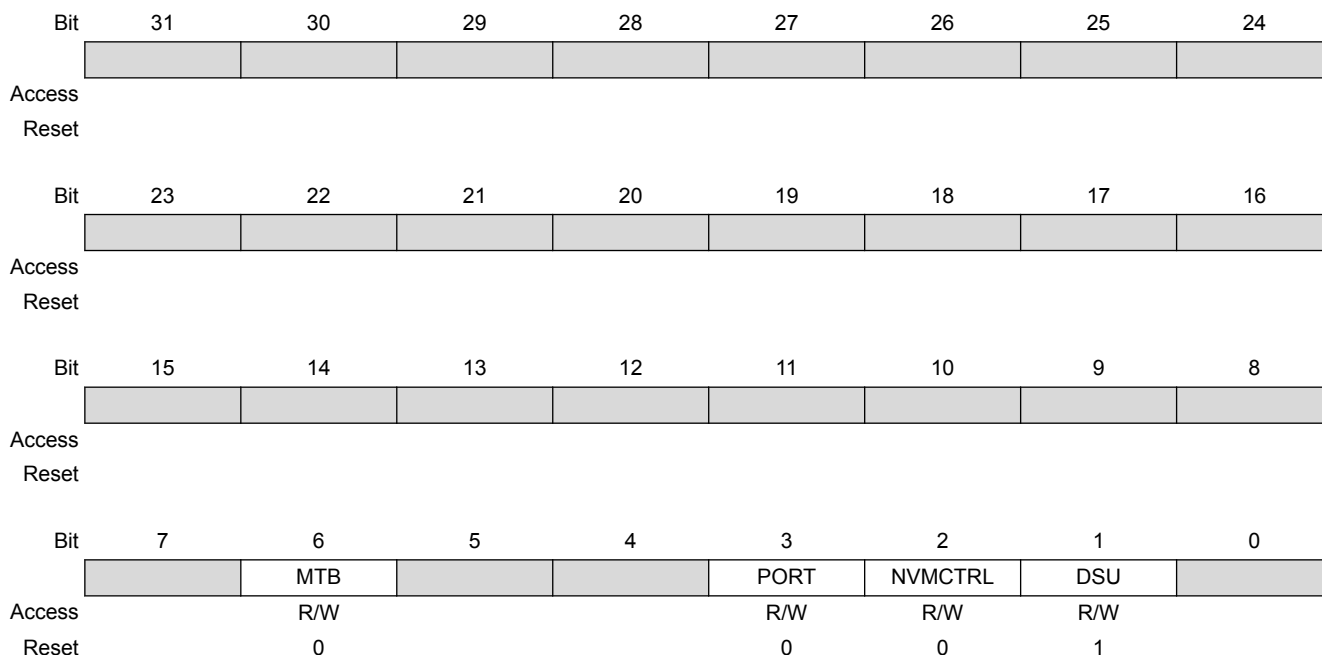
Bit 4 – WDT

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

7.7.2.1. Write Protect Clear

Name: WPCLR
Offset: 0x00
Reset: 0x000002
Property: –



Bit 6 – MTB

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 3 – PORT

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 2 – NVMCTRL

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 1 – DSU

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

7.7.3. PAC2 Register Description

7.7.3.2. Write Protect Set

Name: WPSET
Offset: 0x04
Reset: 0x00800000
Property: –

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
					PTC	DAC	AC	ADC
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0
Bit	15	14	13	12	11	10	9	8
	TC7	TC6	TC5	TC4	TC3	TC2	TC1	TC0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	SERCOM5	SERCOM4	SERCOM3	SERCOM2	SERCOM1	SERCOM0	EVSYS	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	

Bit 19 – PTC

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 18 – DAC

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 17 – AC

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

8.2. Package Drawings

8.2.1. 64 pin TQFP

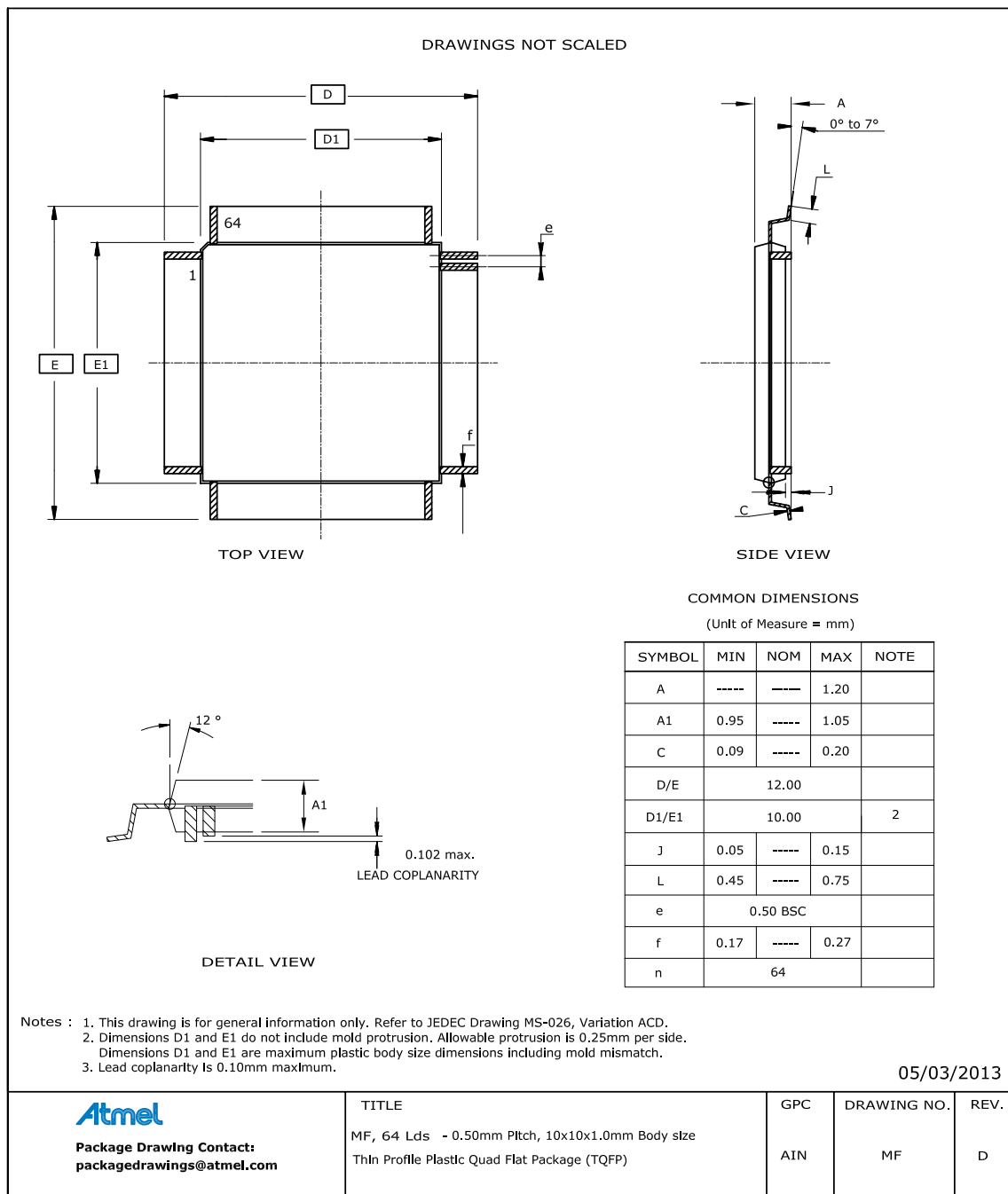


Table 8-2. Device and Package Maximum Weight

300	mg
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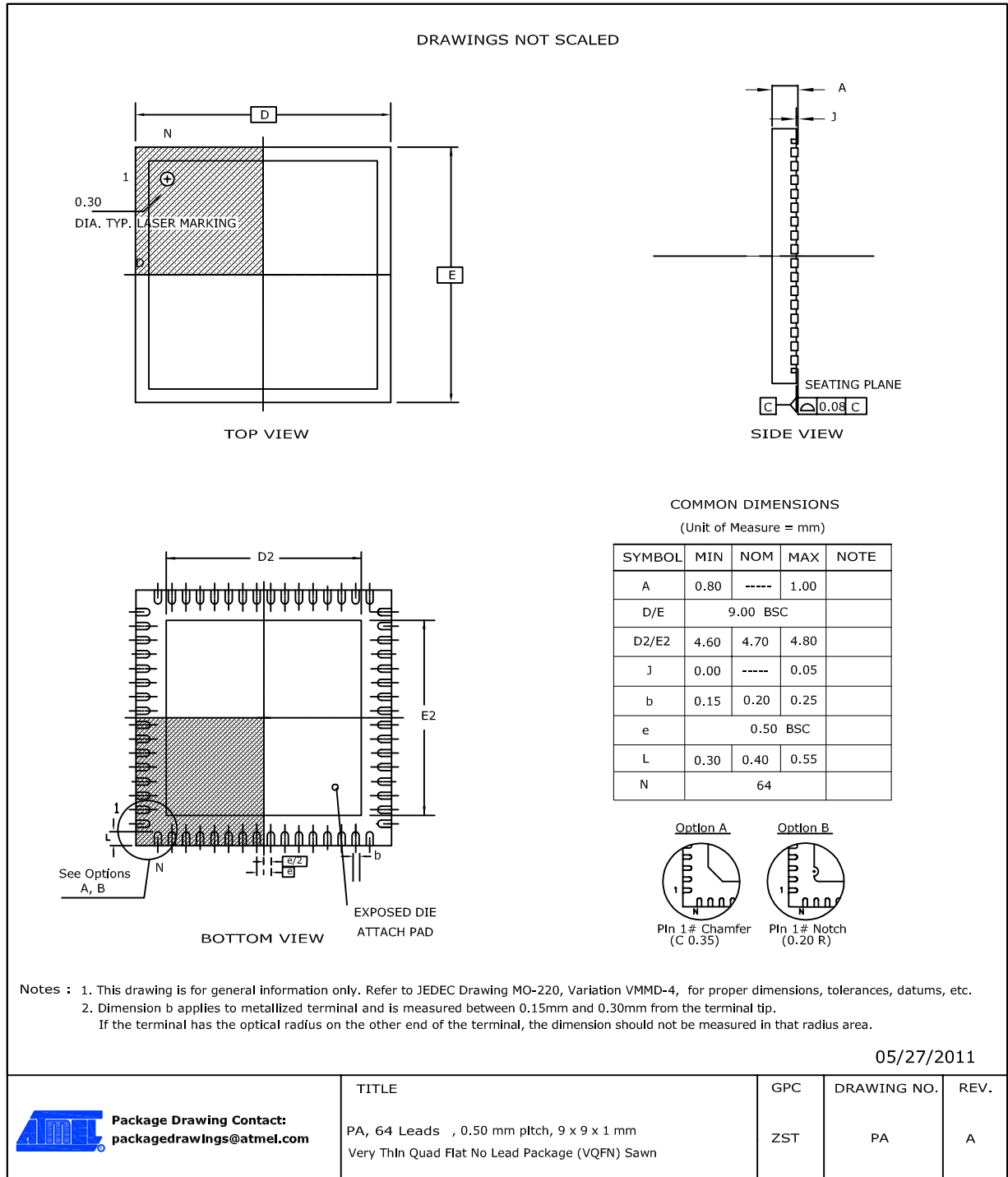
Table 8-3. Package Characteristics

Moisture Sensitivity Level	MSL3
----------------------------	------

Table 8-4. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

8.2.2. 64 pin QFN



Note: The exposed die attach pad is not connected electrically inside the device.

Table 8-9. Package Characteristics

Moisture Sensitivity Level	MSL3
----------------------------	------

Table 8-10. Package Reference

JEDEC Drawing Reference	MO-220
JESD97 Classification	E8

8.2.4. 48 pin TQFP

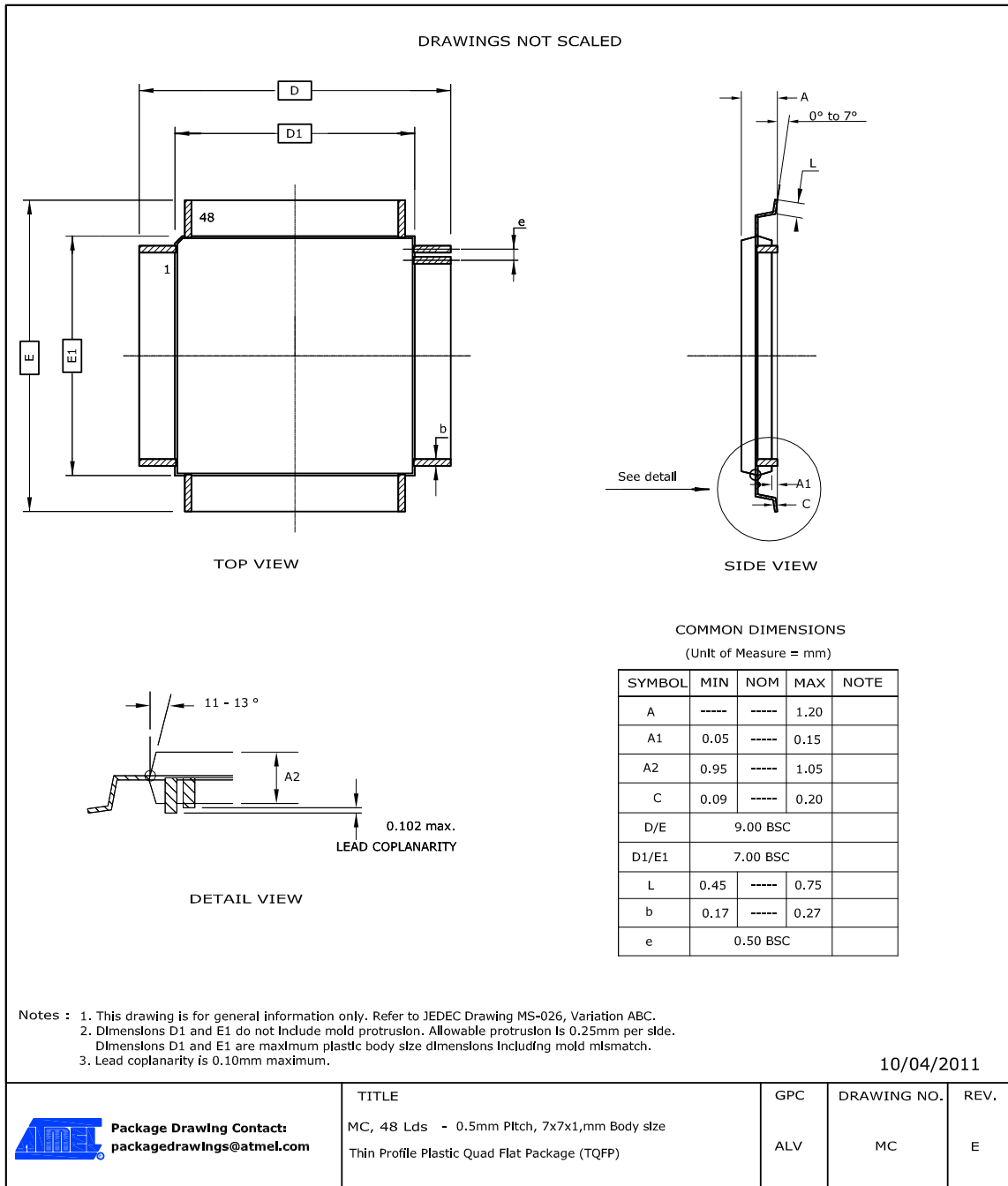


Table 8-11. Device and Package Maximum Weight

140	mg
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Table 8-12. Package Characteristics

Moisture Sensitivity Level	MSL3
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Table 8-13. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

Table 8-16. Package Reference

JEDEC Drawing Reference	MO-220
JESD97 Classification	E3

8.2.6. 45-ball WLCSP

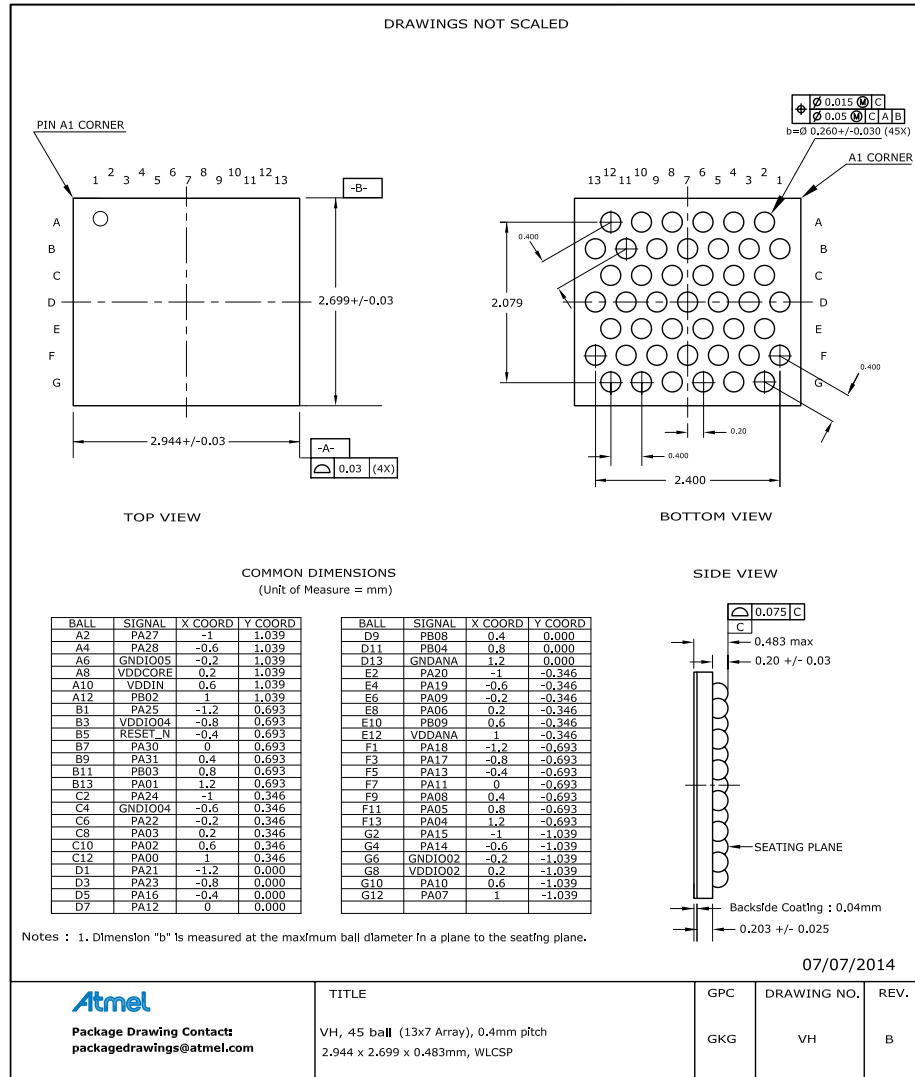


Table 8-17. Device and Package Maximum Weight

7.3	mg
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Table 8-18. Package Characteristics

Moisture Sensitivity Level	MSL1
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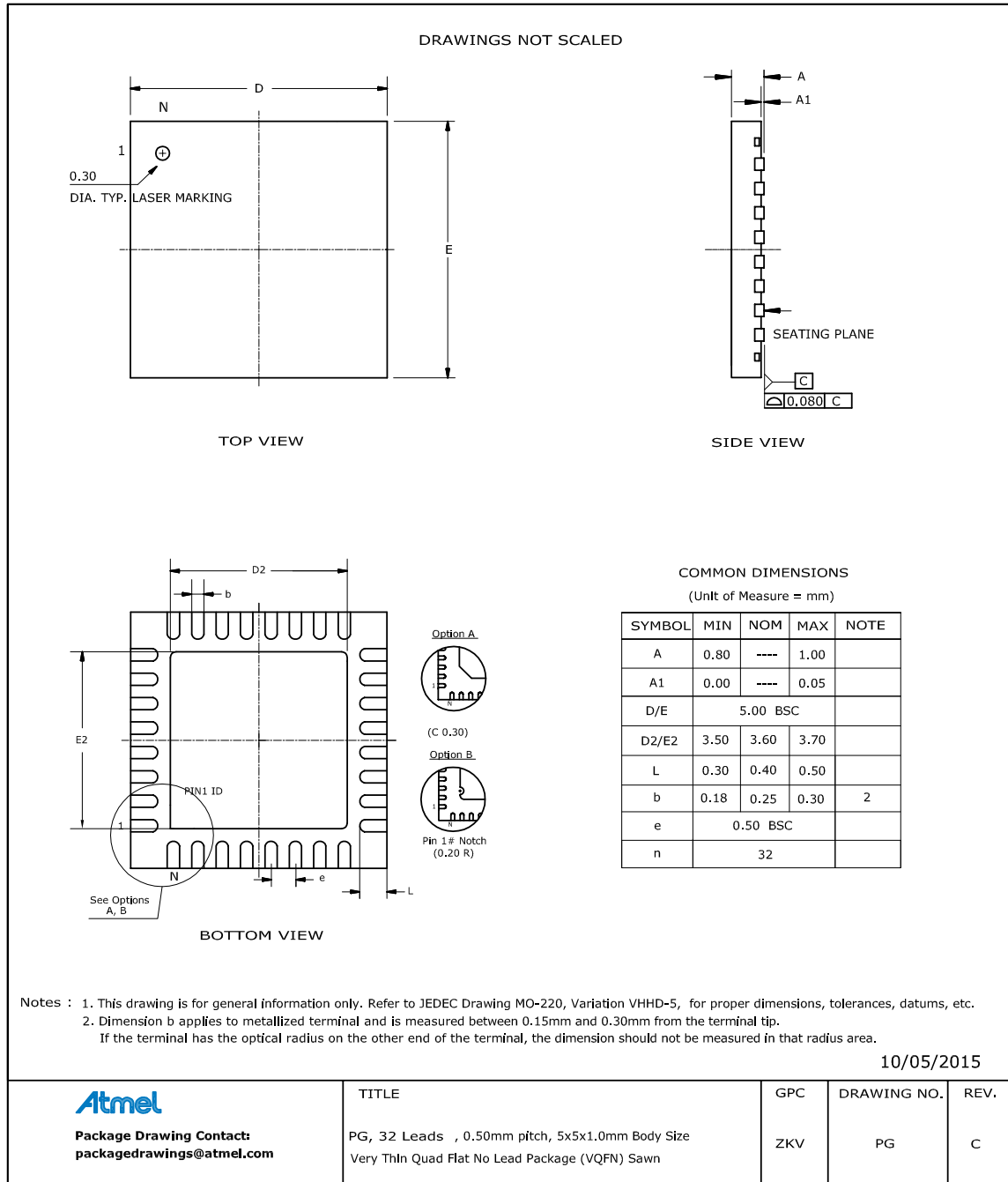
Table 8-19. Package Reference

JEDEC Drawing Reference	MO-220
JESD97 Classification	E1

Table 8-22. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

8.2.8. 32 pin QFN



Note: The exposed die attach pad is connected inside the device to GND and GNDANA.

Table 8-23. Device and Package Maximum Weight

90	mg
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Table 8-24. Package Characteristics

Moisture Sensitivity Level	MSL3
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Table 8-25. Package Reference

JEDEC Drawing Reference	MO-220
JESD97 Classification	E3

8.2.9. 35 ball WLCSP

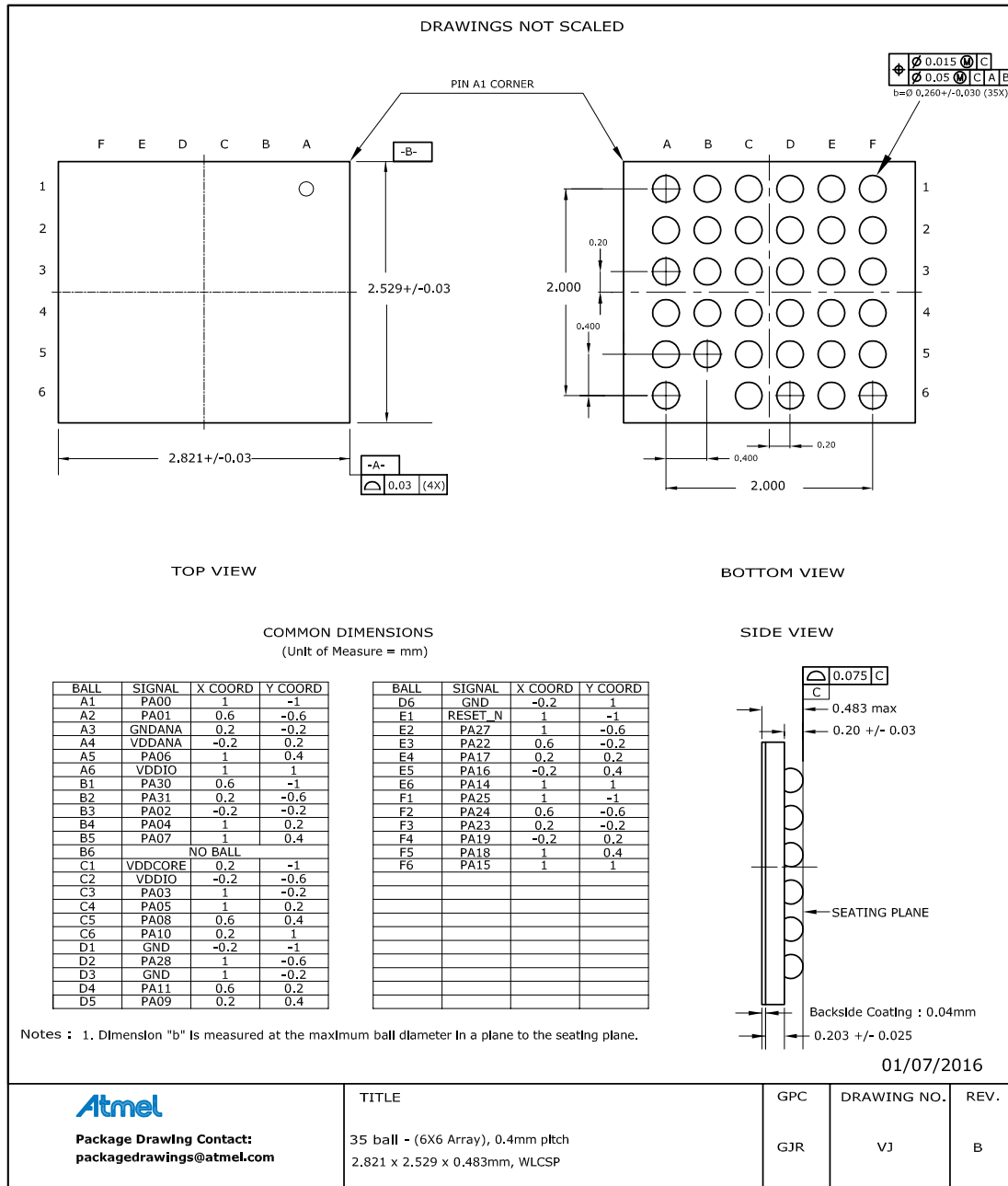


Table 8-26. Device and Package Maximum Weight

6.2	mg
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