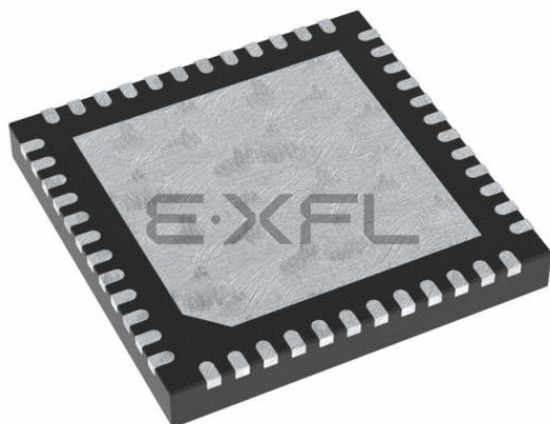




Welcome to [E-XFL.COM](#)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	38
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 14x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamd20g17a-mnt

Table of Contents

Introduction.....	1
Features.....	1
1. Description.....	4
2. Configuration Summary.....	5
3. Ordering Information.....	6
3.1. SAM D20E.....	6
3.2. SAM D20G.....	8
3.3. SAM D20J.....	9
3.4. Device Identification.....	11
4. Block Diagram.....	13
5. Pinout.....	14
5.1. SAM D20J.....	14
5.2. SAM D20G.....	16
5.3. SAM D20E.....	18
6. Product Mapping.....	19
7. Processor And Architecture.....	20
7.1. Cortex M0+ Processor.....	20
7.2. Nested Vector Interrupt Controller.....	21
7.3. Micro Trace Buffer.....	23
7.4. High-Speed Bus System.....	24
7.5. AHB-APB Bridge.....	24
7.6. PAC - Peripheral Access Controller.....	25
7.7. Register Description.....	26
8. Packaging Information.....	39
8.1. Thermal Considerations.....	39
8.2. Package Drawings.....	40
8.3. Soldering Profile.....	50

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAMD20E15A-AU	32K	4K	TQFP32	Tray
ATSAMD20E15A-AUT				Tape & Reel
ATSAMD20E15A-AN				Tray
ATSAMD20E15A-ANT				Tape & Reel
ATSAMD20E15A-MU			QFN32	Tray
ATSAMD20E15A-MUT				Tape & Reel
ATSAMD20E15A-MN				Tray
ATSAMD20E15A-MNT				Tape & Reel
ATSAMD20E16A-AU	64K	8K	TQFP32	Tray
ATSAMD20E16A-AUT				Tape & Reel
ATSAMD20E16A-AN				Tray
ATSAMD20E16A-AFT				Tape & Reel
ATSAMD20E16A-MU			QFN32	Tray
ATSAMD20E16A-MUT				Tape & Reel
ATSAMD20E16A-MN				Tray
ATSAMD20E16A-MNT				Tape & Reel
ATSAMD20E17A-AU	128K	16K	TQFP32	Tray
ATSAMD20E17A-AUT				Tape & Reel
ATSAMD20E17A-AN				Tray
ATSAMD20E17A-ANT				Tape & Reel
ATSAMD20E17A-MU			QFN32	Tray
ATSAMD20E17A-MUT				Tape & Reel
ATSAMD20E17A-MN				Tray
ATSAMD20E17A-MNT				Tape & Reel
ATSAMD20E18A-AU	256K	32K	TQFP32	Tray
ATSAMD20E18A-AUT				Tape & Reel
ATSAMD20E18A-AN				Tray
ATSAMD20E18A-AFT				Tape & Reel
ATSAMD20E18A-MU			QFN32	Tray
ATSAMD20E18A-MUT				Tape & Reel
ATSAMD20E18A-MN				Tray
ATSAMD20E18A-MNT				Tape & Reel

3.2. SAM D20G

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAMD20G14A-AU	16K	2K	TQFP32	Tray
ATSAMD20G14A-AUT				Tape & Reel
ATSAMD20G14A-AN				Tray
ATSAMD20G14A-ANT				Tape & Reel
ATSAMD20G14A-MU			QFN32	Tray
ATSAMD20G14A-MUT				Tape & Reel
ATSAMD20G14A-MN				Tray
ATSAMD20G14A-MNT				Tape & Reel
ATSAMD20G15A-AU	32K	4K	TQFP48	Tray
ATSAMD20G15A-AUT				Tape & Reel
ATSAMD20G15A-AN				Tray
ATSAMD20G15A-ANT				Tape & Reel
ATSAMD20G15A-MU			QFN48	Tray
ATSAMD20G15A-MUT				Tape & Reel
ATSAMD20G15A-MN				Tray
ATSAMD20G15A-MNT				Tape & Reel
ATSAMD20G16A-AU	64K	8K	TQFP48	Tray
ATSAMD20G16A-AUT				Tape & Reel
ATSAMD20G16A-AN				Tray
ATSAMD20G16A-ANT				Tape & Reel
ATSAMD20G16A-MU			QFN48	Tray
ATSAMD20G16A-MUT				Tape & Reel
ATSAMD20G16A-MN				Tray
ATSAMD20G16A-MNT				Tape & Reel

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAMD20J15A-AU	32K	4K	TQFP64	Tray
ATSAMD20J15A-AUT				Tape & Reel
ATSAMD20J15A-AN				Tray
ATSAMD20J15A-ANT				Tape & Reel
ATSAMD20J15A-MU			QFN64	Tray
ATSAMD20J15A-MUT				Tape & Reel
ATSAMD20J15A-MN				Tray
ATSAMD20J15A-MNT				Tape & Reel
ATSAMD20J16A-AU	64K	8K	TQFP64	Tray
ATSAMD20J16A-AUT				Tape & Reel
ATSAMD20J16A-AN				Tray
ATSAMD20J16A-ANT				Tape & Reel
ATSAMD20J16A-MU			QFN64	Tray
ATSAMD20J16A-MUT				Tape & Reel
ATSAMD20J16A-MN				Tray
ATSAMD20J16A-MNT				Tape & Reel
ATSAMD20J16A-CU			UFBGA64	Tray
ATSAMD20J16A-CUT				Tape & Reel
ATSAMD20J17A-AU	128K	16K	TQFP64	Tray
ATSAMD20J17A-AUT				Tape & Reel
ATSAMD20J17A-AN				Tray
ATSAMD20J17A-ANT				Tape & Reel
ATSAMD20J17A-MU			QFN64	Tray
ATSAMD20J17A-MUT				Tape & Reel
ATSAMD20J17A-MN				Tray
ATSAMD20J17A-MNT				Tape & Reel
ATSAMD20J17A-CU			UFBGA64	Tray
ATSAMD20J17A-CUT				Tape & Reel

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAMD20J18A-AU	256K	32K	TQFP64	Tray
ATSAMD20J18A-AUT				Tape & Reel
ATSAMD20J18A-AN				Tray
ATSAMD20J18A-ANT				Tape & Reel
ATSAMD20J18A-MU			QFN64	Tray
ATSAMD20J18A-MUT				Tape & Reel
ATSAMD20J18A-MN				Tray
ATSAMD20J18A-MNT				Tape & Reel
ATSAMD20J18A-CU			UFBGA64	Tray
ATSAMD20J18A-CUT				Tape & Reel

3.4. Device Identification

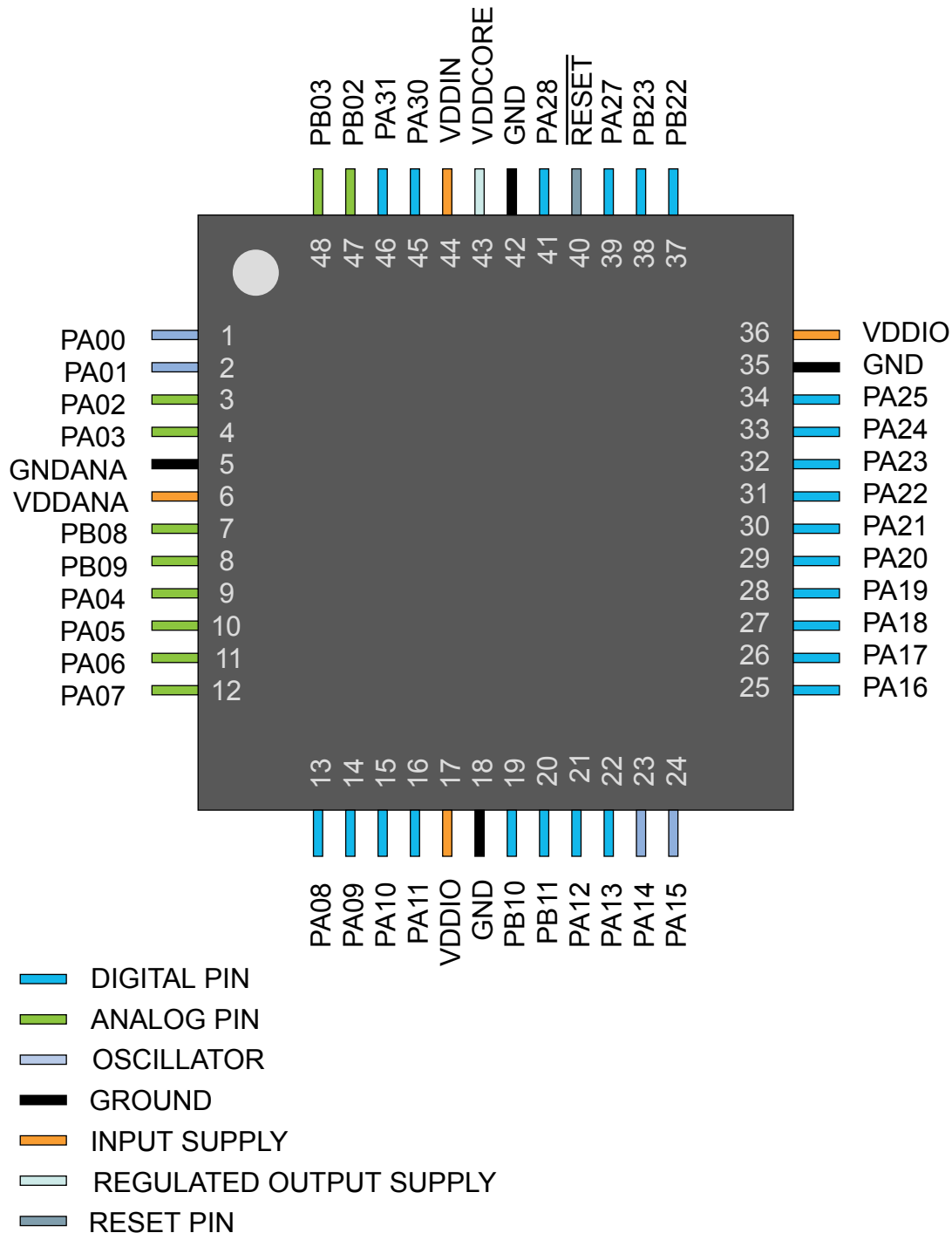
The DSU - Device Service Unit peripheral provides the Device Selection bits in the Device Identification register (DID.DEVSEL) in order to identify the device by software. The device variants have a reset value of DID=0x1001drxx, with the LSB identifying the die number ('d'), the die revision ('r') and the device selection ('xx').

Table 3-1. Device Identification Values

Device Variant	DID.DEVSEL	Device ID (DID)
SAMD20J18C	0x00	0x10001300
SAMD20J18A	0x00	0x10001300
SAMD20J17A	0x01	0x10001301
SAMD20J16A	0x02	0x10001302
SAMD20J15A	0x03	0x10001303
SAMD20J14A	0x04	0x10001304
SAMD20G18A	0x05	0x10001305
SAMD20G17A	0x06	0x10001306
SAMD20G16A	0x07	0x10001307
SAMD20G15A	0x08	0x10001308
SAMD20G14A	0x09	0x10001309
SAMD20E18A	0x0A	0x1000130A
SAMD20E17A	0x0B	0x1000130B
SAMD20E16A	0x0C	0x1000130C
SAMD20E15A	0x0D	0x1000130D

5.2. SAM D20G

5.2.1. QFN48 / TQFP48



(INTFLAG) register. The interrupt flag is set when the interrupt condition occurs. Each interrupt in the peripheral can be individually enabled by writing a one to the corresponding bit in the peripheral's Interrupt Enable Set (INTENSET) register, and disabled by writing a one to the corresponding bit in the peripheral's Interrupt Enable Clear (INTENCLR) register. An interrupt request is generated from the peripheral when the interrupt flag is set and the corresponding interrupt is enabled. The interrupt requests for one peripheral are ORed together on system level, generating one interrupt request for each peripheral. An interrupt request will set the corresponding interrupt pending bit in the NVIC interrupt pending registers (SETPEND/CLRPEND bits in ISPR/ICPR). For the NVIC to activate the interrupt, it must be enabled in the NVIC interrupt enable register (SETENA/CLRENA bits in ISER/ICER). The NVIC interrupt priority registers IPR0-IPR7 provide a priority field for each interrupt.

Table 7-3. Interrupt Line Mapping

Peripheral Source	NVIC Line
EIC NMI – External Interrupt Controller	NMI
PM – Power Manager	0
SYSCTRL – System Control	1
WDT – Watchdog Timer	2
RTC – Real Time Counter	3
EIC – External Interrupt Controller	4
NVMCTRL – Non-Volatile Memory Controller	5
EVSYS – Event System	6
SERCOM0 – Serial Communication Interface 0	7
SERCOM1 – Serial Communication Interface 1	8
SERCOM2 – Serial Communication Interface 2	9
SERCOM3 – Serial Communication Interface 3	10
SERCOM4 – Serial Communication Interface 4	11
SERCOM5 – Serial Communication Interface 5	12
TC0 – Timer Counter 0	13
TC1 – Timer Counter 1	14
TC2 – Timer Counter 2	15
TC3 – Timer Counter 3	16
TC4 – Timer Counter 4	17
TC5 – Timer Counter 5	18
TC6 – Timer Counter 6	19
TC7 – Timer Counter 7	20
ADC – Analog-to-Digital Converter	21
AC – Analog Comparator	22

Peripheral Source	NVIC Line
DAC – Digital-to-Analog Converter	23
PTC – Peripheral Touch Controller	24

7.3. Micro Trace Buffer

7.3.1. Features

- Program flow tracing for the Cortex-M0+ processor
- MTB SRAM can be used for both trace and general purpose storage by the processor
- The position and size of the trace buffer in SRAM is configurable by software
- CoreSight compliant

7.3.2. Overview

When enabled, the MTB records changes in program flow, reported by the Cortex-M0+ processor over the execution trace interface shared between the Cortex-M0+ processor and the CoreSight MTB-M0+. This information is stored as trace packets in the SRAM by the MTB. An off-chip debugger can extract the trace information using the Debug Access Port to read the trace information from the SRAM. The debugger can then reconstruct the program flow from this information.

The MTB simultaneously stores trace information into the SRAM, and gives the processor access to the SRAM. The MTB ensures that trace write accesses have priority over processor accesses.

The execution trace packet consists of a pair of 32-bit words that the MTB generates when it detects the processor PC value changes non-sequentially. A non-sequential PC change can occur during branch instructions or during exception entry. See the CoreSight MTB-M0+ Technical Reference Manual for more details on the MTB execution trace packet format.

Tracing is enabled when the MASTER.EN bit in the Master Trace Control Register is 1. There are various ways to set the bit to 1 to start tracing, or to 0 to stop tracing. See the CoreSight Cortex-M0+ Technical Reference Manual for more details on the Trace start and stop and for a detailed description of the MTB's MASTER register. The MTB can be programmed to stop tracing automatically when the memory fills to a specified watermark level or to start or stop tracing by writing directly to the MASTER.EN bit. If the watermark mechanism is not being used and the trace buffer overflows, then the buffer wraps around overwriting previous trace packets.

The base address of the MTB registers is 0x41006000; this address is also written in the CoreSight ROM Table. The offset of each register from the base address is fixed and as defined by the CoreSight MTB-M0+ Technical Reference Manual. The MTB has 4 programmable registers to control the behavior of the trace features:

- POSITION: Contains the trace write pointer and the wrap bit,
- MASTER: Contains the main trace enable bit and other trace control fields,
- FLOW: Contains the WATERMARK address and the AUTOSTOP and AUTOHALT control bits,
- BASE: Indicates where the SRAM is located in the processor memory map. This register is provided to enable auto discovery of the MTB SRAM location, by a debug agent.

See the CoreSight MTB-M0+ Technical Reference Manual for a detailed description of these registers.

7.7.1.1. Write Protect Clear

Name: WPCLR
Offset: 0x00
Reset: 0x000000
Property: –

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access								
Reset								
Bit	7	6	5	4	3	2	1	0
		EIC	RTC	WDT	GCLK	SYSCTRL	PM	
Access		R/W	R/W	R/W	R/W	R/W	R/W	
Reset		0	0	0	0	0	0	

Bit 6 – EIC

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 5 – RTC

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 4 – WDT

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 3 – GCLK

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 2 – SYSCTRL

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 1 – PM

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

7.7.2.2. Write Protect Set

Name: WPSET
Offset: 0x04
Reset: 0x000002
Property: –

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access								
Reset								
Bit	7	6	5	4	3	2	1	0
		MTB			PORT	NVMCTRL	DSU	
Access		R/W			R/W	R/W	R/W	
Reset		0			0	0	1	

Bit 6 – MTB

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 3 – PORT

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 2 – NVMCTRL

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

7.7.3.1. Write Protect Clear

Name: WPCLR
Offset: 0x00
Reset: 0x00800000
Property: –

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
					PTC	DAC	AC	ADC
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0
Bit	15	14	13	12	11	10	9	8
	TC7	TC6	TC5	TC4	TC3	TC2	TC1	TC0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	SERCOM5	SERCOM4	SERCOM3	SERCOM2	SERCOM1	SERCOM0	EVSYN	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	

Bit 19 – PTC

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 18 – DAC

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 17 – AC

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 16 – ADC

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bits 15,14,13,12,11,10,9,8 – TCx

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bits 7,6,5,4,3,2 – SERCOMx

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 1 – EVSYS

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

7.7.3.2. Write Protect Set

Name: WPSET
Offset: 0x04
Reset: 0x00800000
Property: –

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
					PTC	DAC	AC	ADC
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0
Bit	15	14	13	12	11	10	9	8
	TC7	TC6	TC5	TC4	TC3	TC2	TC1	TC0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	SERCOM5	SERCOM4	SERCOM3	SERCOM2	SERCOM1	SERCOM0	EVSYS	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	

Bit 19 – PTC

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 18 – DAC

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 17 – AC

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

8.2. Package Drawings

8.2.1. 64 pin TQFP

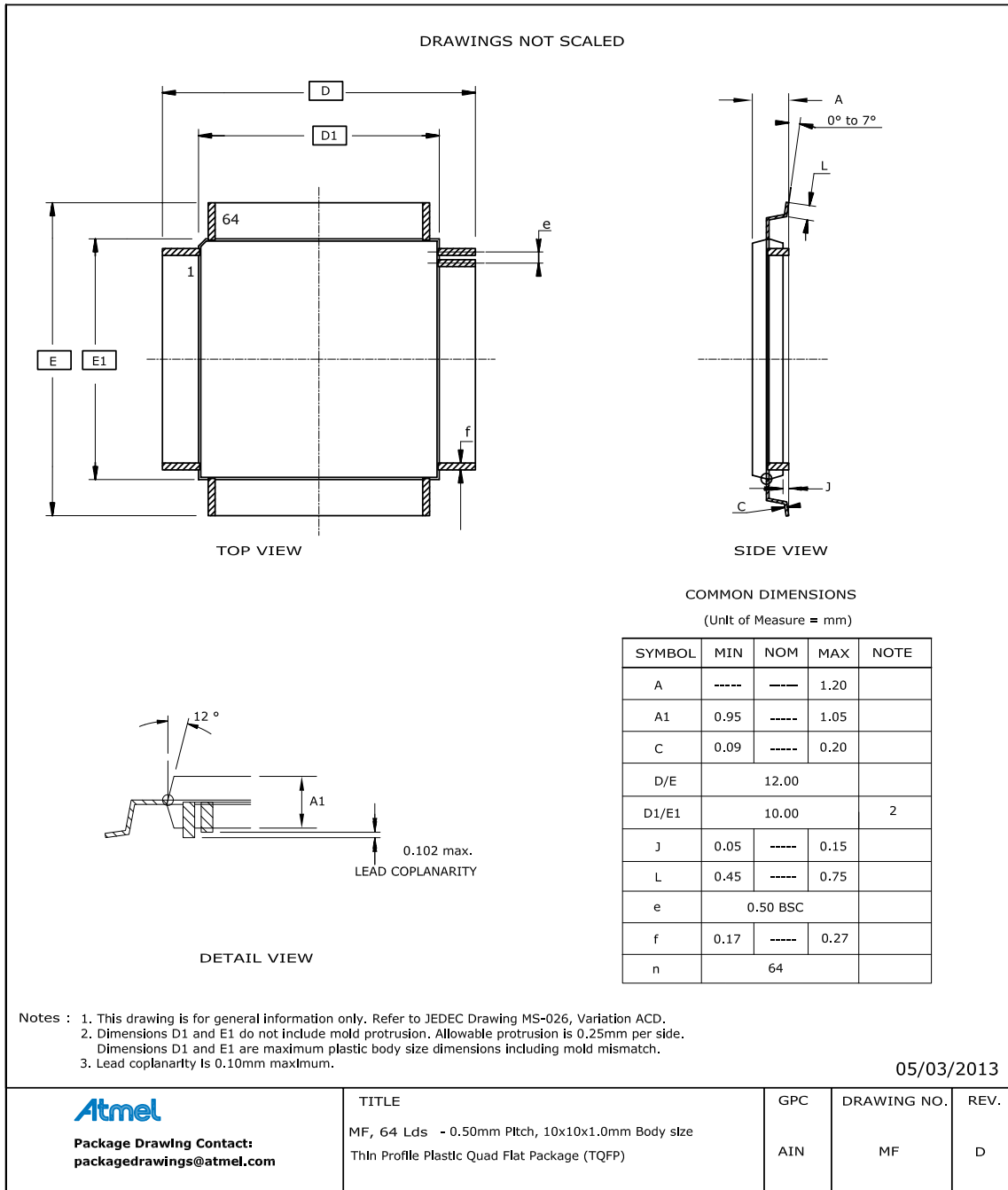


Table 8-2. Device and Package Maximum Weight

300	mg
-----	----

Table 8-3. Package Characteristics

Moisture Sensitivity Level	MSL3
----------------------------	------

Table 8-11. Device and Package Maximum Weight

140	mg
-----	----

Table 8-12. Package Characteristics

Moisture Sensitivity Level	MSL3
----------------------------	------

Table 8-13. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

Table 8-16. Package Reference

JEDEC Drawing Reference	MO-220
JESD97 Classification	E3

8.2.6. 45-ball WLCSP

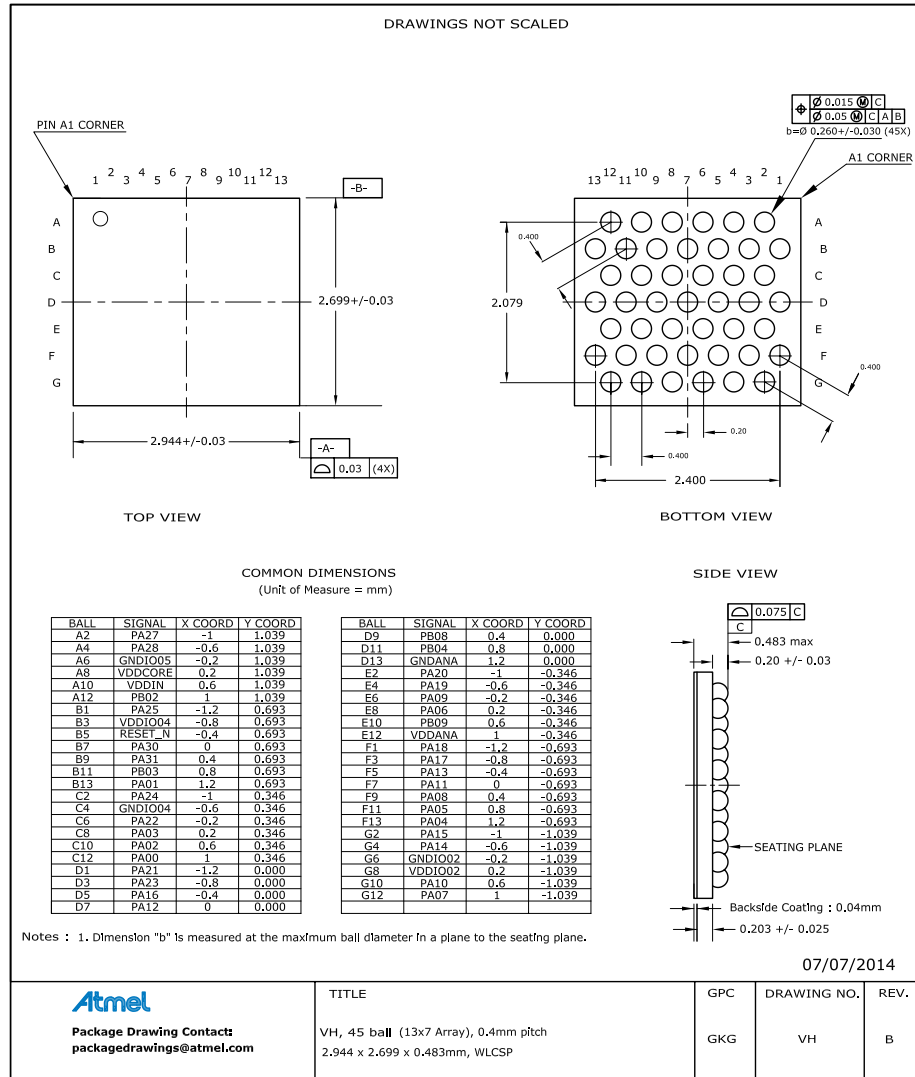


Table 8-17. Device and Package Maximum Weight

7.3	mg
-----	----

Table 8-18. Package Characteristics

Moisture Sensitivity Level	MSL1
----------------------------	------

Table 8-19. Package Reference

JEDEC Drawing Reference	MO-220
JESD97 Classification	E1

8.2.7. 32 pin TQFP

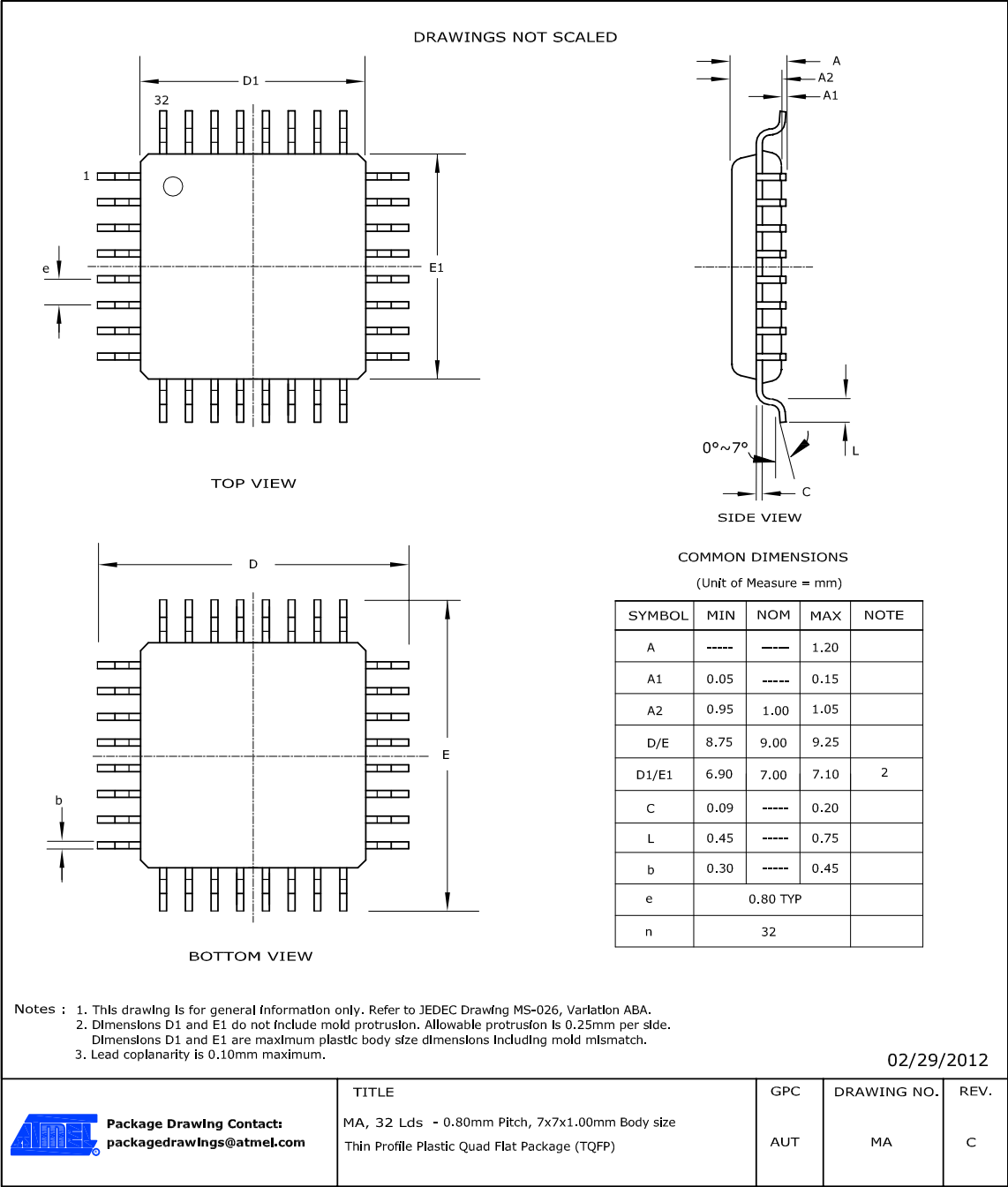


Table 8-20. Device and Package Maximum Weight

100	mg
-----	----

Table 8-21. Package Characteristics

Moisture Sensitivity Level	MSL3
----------------------------	------

Table 8-27. Package Characteristics

Moisture Sensitivity Level	MSL1
----------------------------	------

Table 8-28. Package Reference

JEDEC Drawing Reference	MO-220
JESD97 Classification	E1

8.3. Soldering Profile

The following table gives the recommended soldering profile from J-STD-20.

Table 8-29.

Profile Feature	Green Package
Average Ramp-up Rate (217°C to peak)	3°C/s max.
Preheat Temperature 175°C ±25°C	150-200°C
Time Maintained Above 217°C	60-150s
Time within 5°C of Actual Peak Temperature	30s
Peak Temperature Range	260°C
Ramp-down Rate	6°C/s max.
Time 25°C to Peak Temperature	8 minutes max.

A maximum of three reflow passes is allowed per component.



Atmel Corporation 1600 Technology Drive, San Jose, CA 95110 USA **T:** (+1)(408) 441.0311 **F:** (+1)(408) 436.4200 | **www.atmel.com**

© 2016 Atmel Corporation. / Rev.: Atmel-42129P-SAM D20_Datasheet_Summary-09/2016

Atmel®, Atmel logo and combinations thereof, Enabling Unlimited Possibilities®, and others are registered trademarks or trademarks of Atmel Corporation in U.S. and other countries. ARM®, ARM Connected® logo, and others are the registered trademarks or trademarks of ARM Ltd. Other terms and product names may be trademarks of others.

DISCLAIMER: The information in this document is provided in connection with Atmel products. No license, express or implied, by estoppel or otherwise, to any intellectual property right is granted by this document or in connection with the sale of Atmel products. EXCEPT AS SET FORTH IN THE ATMEL TERMS AND CONDITIONS OF SALES LOCATED ON THE ATMEL WEBSITE, ATMEL ASSUMES NO LIABILITY WHATSOEVER AND DISCLAIMS ANY EXPRESS, IMPLIED OR STATUTORY WARRANTY RELATING TO ITS PRODUCTS INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTY OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT. IN NO EVENT SHALL ATMEL BE LIABLE FOR ANY DIRECT, INDIRECT, CONSEQUENTIAL, PUNITIVE, SPECIAL OR INCIDENTAL DAMAGES (INCLUDING, WITHOUT LIMITATION, DAMAGES FOR LOSS AND PROFITS, BUSINESS INTERRUPTION, OR LOSS OF INFORMATION) ARISING OUT OF THE USE OR INABILITY TO USE THIS DOCUMENT, EVEN IF ATMEL HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. Atmel makes no representations or warranties with respect to the accuracy or completeness of the contents of this document and reserves the right to make changes to specifications and products descriptions at any time without notice. Atmel does not make any commitment to update the information contained herein. Unless specifically provided otherwise, Atmel products are not suitable for, and shall not be used in, automotive applications. Atmel products are not intended, authorized, or warranted for use as components in applications intended to support or sustain life.

SAFETY-CRITICAL, MILITARY, AND AUTOMOTIVE APPLICATIONS DISCLAIMER: Atmel products are not designed for and will not be used in connection with any applications where the failure of such products would reasonably be expected to result in significant personal injury or death ("Safety-Critical Applications") without an Atmel officer's specific written consent. Safety-Critical Applications include, without limitation, life support devices and systems, equipment or systems for the operation of nuclear facilities and weapons systems. Atmel products are not designed nor intended for use in military or aerospace applications or environments unless specifically designated by Atmel as military-grade. Atmel products are not designed nor intended for use in automotive applications unless specifically designated by Atmel as automotive-grade.