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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	38
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 14x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamd20g18a-au

  - Up to five 16-bit Timer/Counters (TC), configurable as either:
    - One 16-bit TC with two compare/capture channels
    - One 8-bit TC with two compare/capture channels
    - One 32-bit TC with two compare/capture channels, by using two TCs
  - 32-bit Real Time Counter (RTC) with clock/calendar function
  - Watchdog Timer (WDT)
  - CRC-32 generator
  - Up to six Serial Communication Interfaces (SERCOM), each configurable to operate as either:
    - USART with full-duplex and single-wire half-duplex configuration
    - Inter-Integrated Circuit (I^2C) up to 400kHz
    - Serial Peripheral Interface (SPI)
  - One 12-bit, 350ksps Analog-to-Digital Converter (ADC) with up to 20 channels
    - Differential and single-ended input
    - 1/2x to 16x programmable gain stage
    - Automatic offset and gain error compensation
    - Oversampling and decimation in hardware to support 13-, 14-, 15- or 16-bit resolution
  - 10-bit, 350ksps Digital-to-Analog Converter (DAC)
  - Two Analog Comparators (AC) with window compare function
  - Peripheral Touch Controller (PTC)
    - 256-Channel capacitive touch and proximity sensing
- I/O
  - Up to 52 programmable I/O pins
- Packages
  - 64-pin TQFP, QFN
  - 64-ball UFBGA
  - 48-pin TQFP, QFN
  - 45-ball WLCSP
  - 32-pin TQFP, QFN
- Operating Voltage
  - 1.62V – 3.63V
- Power Consumption
  - Down to 70µA/MHz in active mode
  - Down to 8µA running the Peripheral Touch Controller

Table of Contents

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAMD20G17A-AU	128K	16K	TQFP48	Tray
ATSAMD20G17A-AUT				Tape & Reel
ATSAMD20G17A-AN				Tray
ATSAMD20G17A-ANT				Tape & Reel
ATSAMD20G17A-MU			QFN48	Tray
ATSAMD20G17A-MUT				Tape & Reel
ATSAMD20G17A-MN				Tray
ATSAMD20G17A-MNT				Tape & Reel
ATSAMD20G17A-UUT			WLCSP45	Tape & Reel
ATSAMD20G18A-AU	256K	32K	TQFP48	Tray
ATSAMD20G18A-AUT				Tape & Reel
ATSAMD20G18A-AN				Tray
ATSAMD20G18A-ANT				Tape & Reel
ATSAMD20G18A-MU			QFN48	Tray
ATSAMD20G18A-MUT				Tape & Reel
ATSAMD20G18A-MN				Tray
ATSAMD20G18A-MNT				Tape & Reel
ATSAMD20G18A-UUT			WLCSP45	Tape & Reel

3.3. SAM D20J

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAMD20J14A-AU	16K	2K	TQFP64	Tray
ATSAMD20J14A-AUT				Tape & Reel
ATSAMD20J14A-AN				Tray
ATSAMD20J14A-ANT				Tape & Reel
ATSAMD20J14A-MU			QFN64	Tray
ATSAMD20J14A-MUT				Tape & Reel
ATSAMD20J14A-MN				Tray
ATSAMD20J14A-MNT				Tape & Reel

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAMD20J15A-AU	32K	4K	TQFP64	Tray
ATSAMD20J15A-AUT				Tape & Reel
ATSAMD20J15A-AN				Tray
ATSAMD20J15A-ANT				Tape & Reel
ATSAMD20J15A-MU			QFN64	Tray
ATSAMD20J15A-MUT				Tape & Reel
ATSAMD20J15A-MN				Tray
ATSAMD20J15A-MNT				Tape & Reel
ATSAMD20J16A-AU	64K	8K	TQFP64	Tray
ATSAMD20J16A-AUT				Tape & Reel
ATSAMD20J16A-AN				Tray
ATSAMD20J16A-ANT				Tape & Reel
ATSAMD20J16A-MU			QFN64	Tray
ATSAMD20J16A-MUT				Tape & Reel
ATSAMD20J16A-MN				Tray
ATSAMD20J16A-MNT				Tape & Reel
ATSAMD20J16A-CU			UFBGA64	Tray
ATSAMD20J16A-CUT				Tape & Reel
ATSAMD20J17A-AU	128K	16K	TQFP64	Tray
ATSAMD20J17A-AUT				Tape & Reel
ATSAMD20J17A-AN				Tray
ATSAMD20J17A-ANT				Tape & Reel
ATSAMD20J17A-MU			QFN64	Tray
ATSAMD20J17A-MUT				Tape & Reel
ATSAMD20J17A-MN				Tray
ATSAMD20J17A-MNT				Tape & Reel
ATSAMD20J17A-CU			UFBGA64	Tray
ATSAMD20J17A-CUT				Tape & Reel

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAMD20J18A-AU	256K	32K	TQFP64	Tray
ATSAMD20J18A-AUT				Tape & Reel
ATSAMD20J18A-AN				Tray
ATSAMD20J18A-ANT				Tape & Reel
ATSAMD20J18A-MU			QFN64	Tray
ATSAMD20J18A-MUT				Tape & Reel
ATSAMD20J18A-MN				Tray
ATSAMD20J18A-MNT				Tape & Reel
ATSAMD20J18A-CU			UFBGA64	Tray
ATSAMD20J18A-CUT				Tape & Reel

3.4. Device Identification

The DSU - Device Service Unit peripheral provides the Device Selection bits in the Device Identification register (DID.DEVSEL) in order to identify the device by software. The device variants have a reset value of DID=0x1001drxx, with the LSB identifying the die number ('d'), the die revision ('r') and the device selection ('xx').

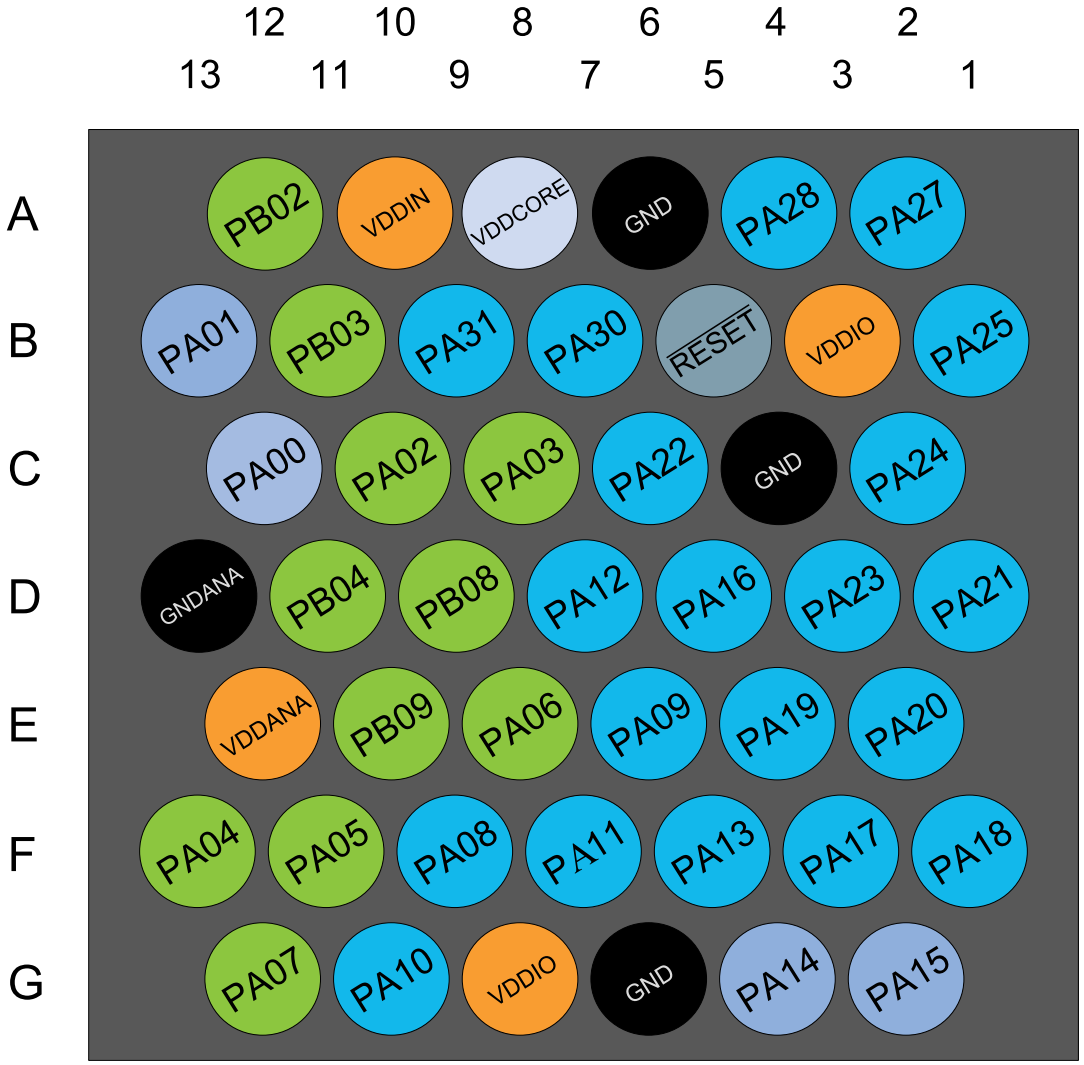
Table 3-1. Device Identification Values

Device Variant	DID.DEVSEL	Device ID (DID)
SAMD20J18C	0x00	0x10001300
SAMD20J18A	0x00	0x10001300
SAMD20J17A	0x01	0x10001301
SAMD20J16A	0x02	0x10001302
SAMD20J15A	0x03	0x10001303
SAMD20J14A	0x04	0x10001304
SAMD20G18A	0x05	0x10001305
SAMD20G17A	0x06	0x10001306
SAMD20G16A	0x07	0x10001307
SAMD20G15A	0x08	0x10001308
SAMD20G14A	0x09	0x10001309
SAMD20E18A	0x0A	0x1000130A
SAMD20E17A	0x0B	0x1000130B
SAMD20E16A	0x0C	0x1000130C
SAMD20E15A	0x0D	0x1000130D

Device Variant	DID.DEVSEL	Device ID (DID)
SAMD20E14A	0x0E	0x1000130E
Reserved	0x0F	
SAMD20G18U	0x10	0x10001310
SAMD20G17U	0x11	0x10001311
Reserved	0x12 - 0xFF	

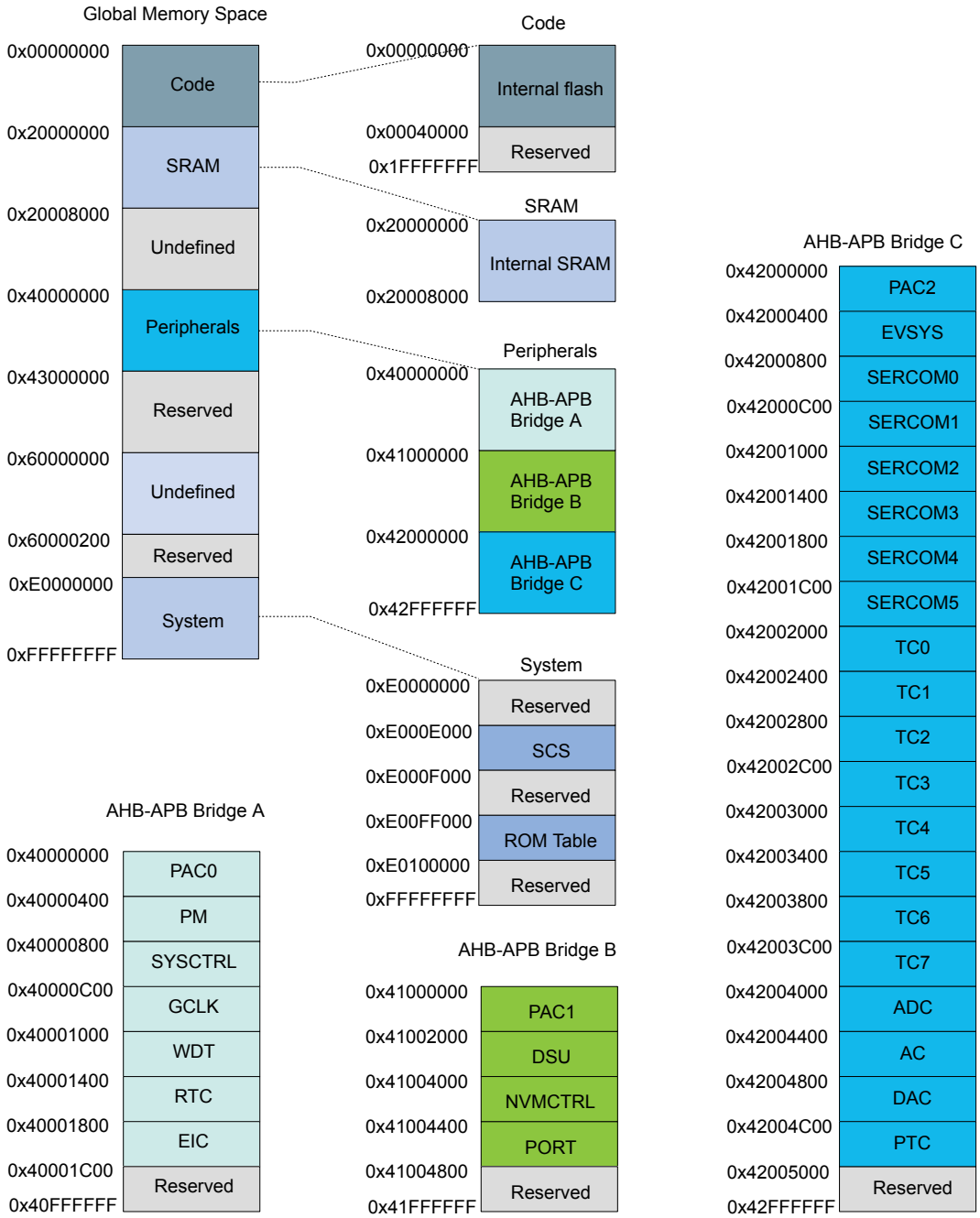
Note: The device variant (last letter of the ordering number) is independent of the die revision (DSU.DID.REVISION): The device variant denotes functional differences, whereas the die revision marks evolution of the die. The device variant denotes functional differences, whereas the die revision marks evolution of the die.

5.2.2. WLCSP45


12 10 8 6 4 2
13 11 9 7 5 3 1
A
B
C
D
E
F
G
PB02 VDDIN VDDCORE GND PA28 PA27
PA01 PB03 PA31 PA30 RESET VDDIO PA25
PA00 PA02 PA03 PA22 GND PA24
GNDANA PB04 PB08 PA12 PA16 PA23 PA21
VDDANA PB09 PA06 PA09 PA19 PA20
PA04 PA05 PA08 PA11 PA13 PA17 PA18
PA07 PA10 VDDIO GND PA14 PA15
DIGITAL PIN
ANALOG PIN
OSCILLATOR
GROUND
INPUT SUPPLY
REGULATED OUTPUT SUPPLY
RESET PIN

6. Product Mapping

Figure 6-1. Product Mapping



This figure represents the full configuration of the SAM D20 device with maximum flash and SRAM capabilities and a full set of peripherals. Refer to the Configuration Summary for details.

Peripheral Source	NVIC Line
DAC – Digital-to-Analog Converter	23
PTC – Peripheral Touch Controller	24

7.3. Micro Trace Buffer

7.3.1. Features

- Program flow tracing for the Cortex-M0+ processor
- MTB SRAM can be used for both trace and general purpose storage by the processor
- The position and size of the trace buffer in SRAM is configurable by software
- CoreSight compliant

7.3.2. Overview

When enabled, the MTB records changes in program flow, reported by the Cortex-M0+ processor over the execution trace interface shared between the Cortex-M0+ processor and the CoreSight MTB-M0+. This information is stored as trace packets in the SRAM by the MTB. An off-chip debugger can extract the trace information using the Debug Access Port to read the trace information from the SRAM. The debugger can then reconstruct the program flow from this information.

The MTB simultaneously stores trace information into the SRAM, and gives the processor access to the SRAM. The MTB ensures that trace write accesses have priority over processor accesses.

The execution trace packet consists of a pair of 32-bit words that the MTB generates when it detects the processor PC value changes non-sequentially. A non-sequential PC change can occur during branch instructions or during exception entry. See the CoreSight MTB-M0+ Technical Reference Manual for more details on the MTB execution trace packet format.

Tracing is enabled when the MASTER.EN bit in the Master Trace Control Register is 1. There are various ways to set the bit to 1 to start tracing, or to 0 to stop tracing. See the CoreSight Cortex-M0+ Technical Reference Manual for more details on the Trace start and stop and for a detailed description of the MTB's MASTER register. The MTB can be programmed to stop tracing automatically when the memory fills to a specified watermark level or to start or stop tracing by writing directly to the MASTER.EN bit. If the watermark mechanism is not being used and the trace buffer overflows, then the buffer wraps around overwriting previous trace packets.

The base address of the MTB registers is 0x41006000; this address is also written in the CoreSight ROM Table. The offset of each register from the base address is fixed and as defined by the CoreSight MTB-M0+ Technical Reference Manual. The MTB has 4 programmable registers to control the behavior of the trace features:

- POSITION: Contains the trace write pointer and the wrap bit,
- MASTER: Contains the main trace enable bit and other trace control fields,
- FLOW: Contains the WATERMARK address and the AUTOSTOP and AUTOHALT control bits,
- BASE: Indicates where the SRAM is located in the processor memory map. This register is provided to enable auto discovery of the MTB SRAM location, by a debug agent.

See the CoreSight MTB-M0+ Technical Reference Manual for a detailed description of these registers.

7.4. High-Speed Bus System

7.4.1. Features

High-Speed Bus Matrix has the following features:

- Symmetric crossbar bus switch implementation
- Allows concurrent accesses from different masters to different slaves
- 32-bit data bus
- Operation at a one-to-one clock frequency with the bus masters

7.4.2. Configuration

Table 7-4. Bus Matrix Masters

Bus Matrix Masters	Master ID
CM0+ - Cortex M0+ Processor	0
DSU - Device Service Unit	1

Table 7-5. Bus Matrix Slaves

Bus Matrix Slaves	Slave ID
Internal Flash Memory	0
AHB-APB Bridge A	1
AHB-APB Bridge B	2
AHB-APB Bridge C	3

7.5. AHB-APB Bridge

The AHB-APB bridge is an AHB slave, providing an interface between the high-speed AHB domain and the low-power APB domain. It is used to provide access to the programmable control registers of peripherals (see *Product Mapping*).

AHB-APB bridge is based on AMBA APB Protocol Specification V2.0 (ref. as APB4) including:

- Wait state support
- Error reporting
- Transaction protection
- Sparse data transfer (byte, half-word and word)

Additional enhancements:

- Address and data cycles merged into a single cycle
- Sparse data transfer also apply to read access

to operate the AHB-APB bridge, the clock (CLK_HPBx_AHB) must be enabled. See *PM – Power Manager* for details.

Figure 7-1. APB Write Access.

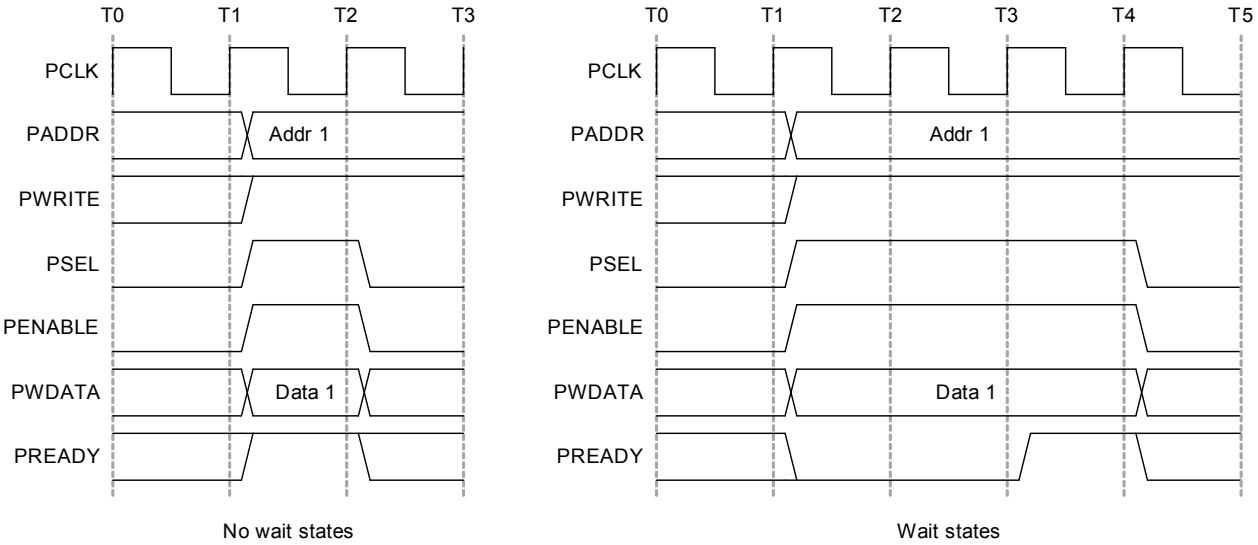
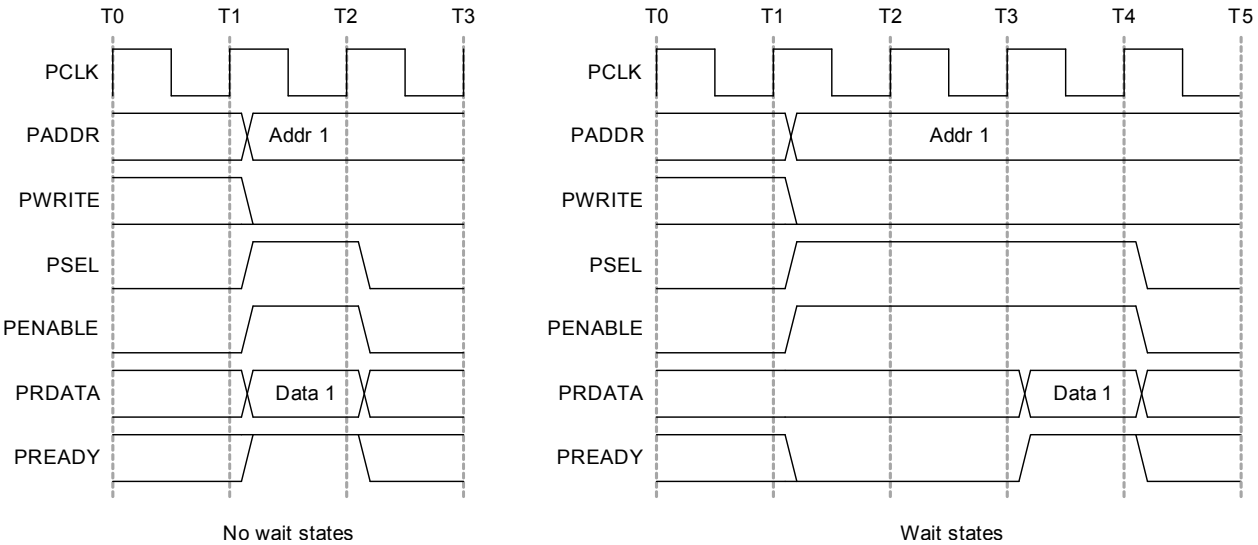


Figure 7-2. APB Read Access.



Related Links

Product Mapping on page 19

7.6. PAC - Peripheral Access Controller

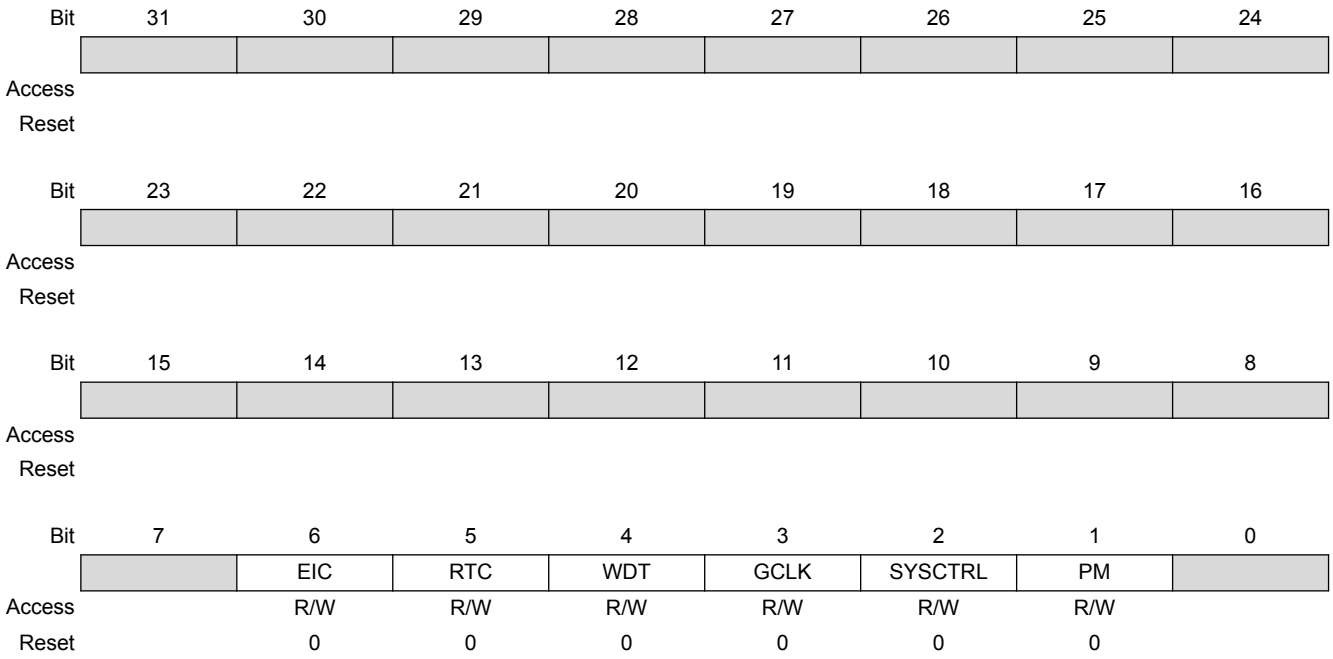
7.6.1. Overview

There is one PAC associated with each AHB-APB bridge. The PAC can provide write protection for registers of each peripheral connected on the same bridge.

The PAC peripheral bus clock (CLK_PACx_APB) can be enabled and disabled in the Power Manager. CLK_PAC0_APB and CLK_PAC1_APB are enabled are reset. CLK_PAC2_APB is disabled at reset. Refer to *PM – Power Manager* for details. The PAC will continue to operate in any sleep mode where the selected clock source is running. Write-protection does not apply for debugger access. When the debugger makes an access to a peripheral, write-protection is ignored so that the debugger can update the register.

7.7.1.2. Write Protect Set

Name: WPSET
Offset: 0x04
Reset: 0x000000
Property: –



Bit 6 – EIC
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 5 – RTC
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 4 – WDT
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

7.7.3.1. Write Protect Clear

Name: WPCLR
Offset: 0x00
Reset: 0x00800000
Property: –

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
					PTC	DAC	AC	ADC
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TC7	TC6	TC5	TC4	TC3	TC2	TC1	TC0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SERCOM5	SERCOM4	SERCOM3	SERCOM2	SERCOM1	SERCOM0	EVSYS	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	

Bit 19 – PTC
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 18 – DAC
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 17 – AC
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 16 – ADC
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bits 15,14,13,12,11,10,9,8 – TCx
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bits 7,6,5,4,3,2 – SERCOMx
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

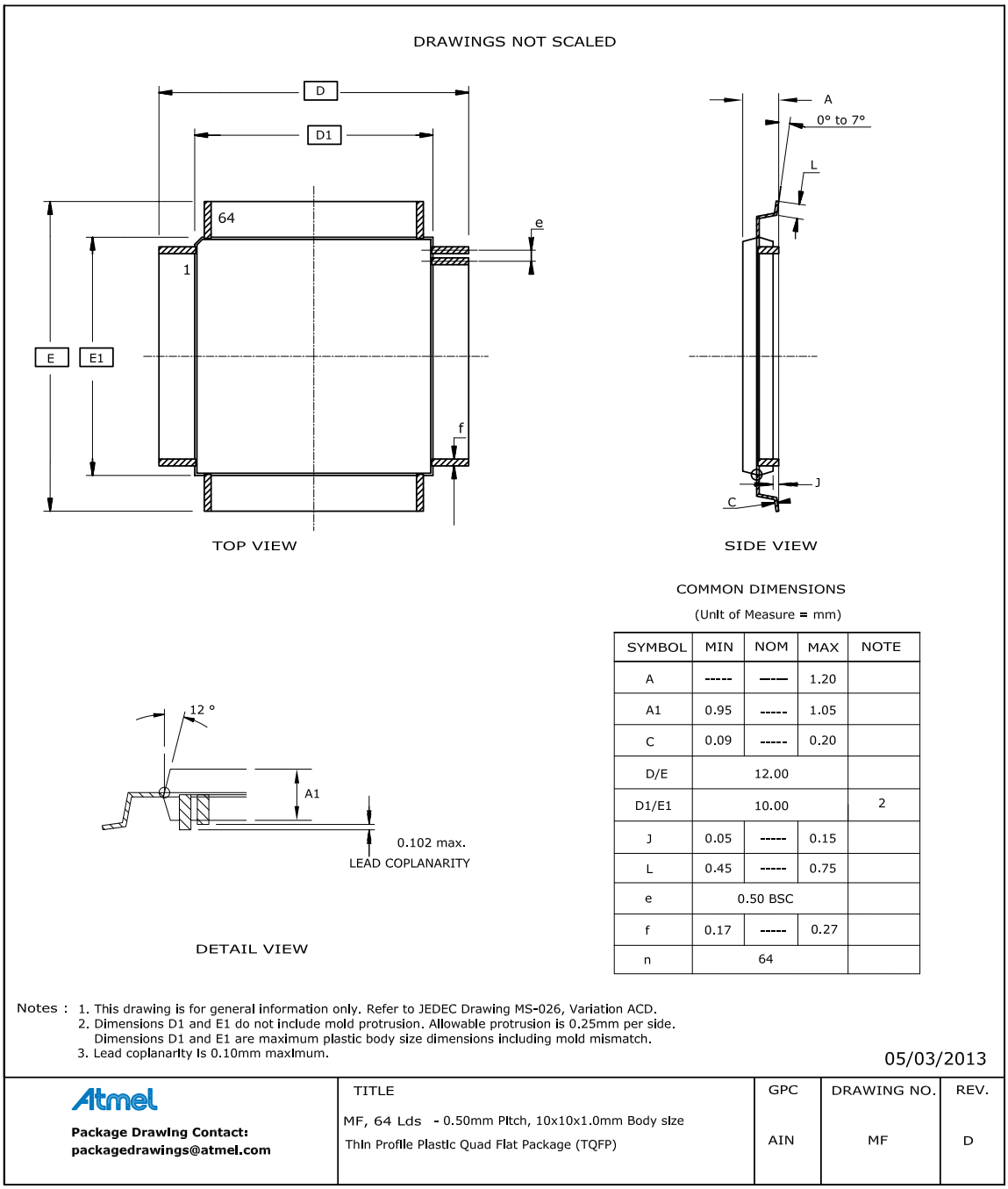
Bit 1 – EVSYS
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

8.2. Package Drawings

8.2.1. 64 pin TQFP



COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-----	-----	1.20	
A1	0.95	-----	1.05	
C	0.09	-----	0.20	
D/E		12.00		
D1/E1		10.00		2
J	0.05	-----	0.15	
L	0.45	-----	0.75	
e		0.50 BSC		
f	0.17	-----	0.27	
n		64		

Notes :
1. This drawing is for general information only. Refer to JEDEC Drawing MS-026, Variation ACD.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

05/03/2013

Atmel Package Drawing Contact: packagedrawings@atmel.com	TITLE MF, 64 Lds - 0.50mm Pitch, 10x10x1.0mm Body size Thin Profile Plastic Quad Flat Package (TQFP)	GPC AIN	DRAWING NO. MF	REV. D

Table 8-2. Device and Package Maximum Weight

300	mg

Table 8-3. Package Characteristics

Moisture Sensitivity Level	MSL3

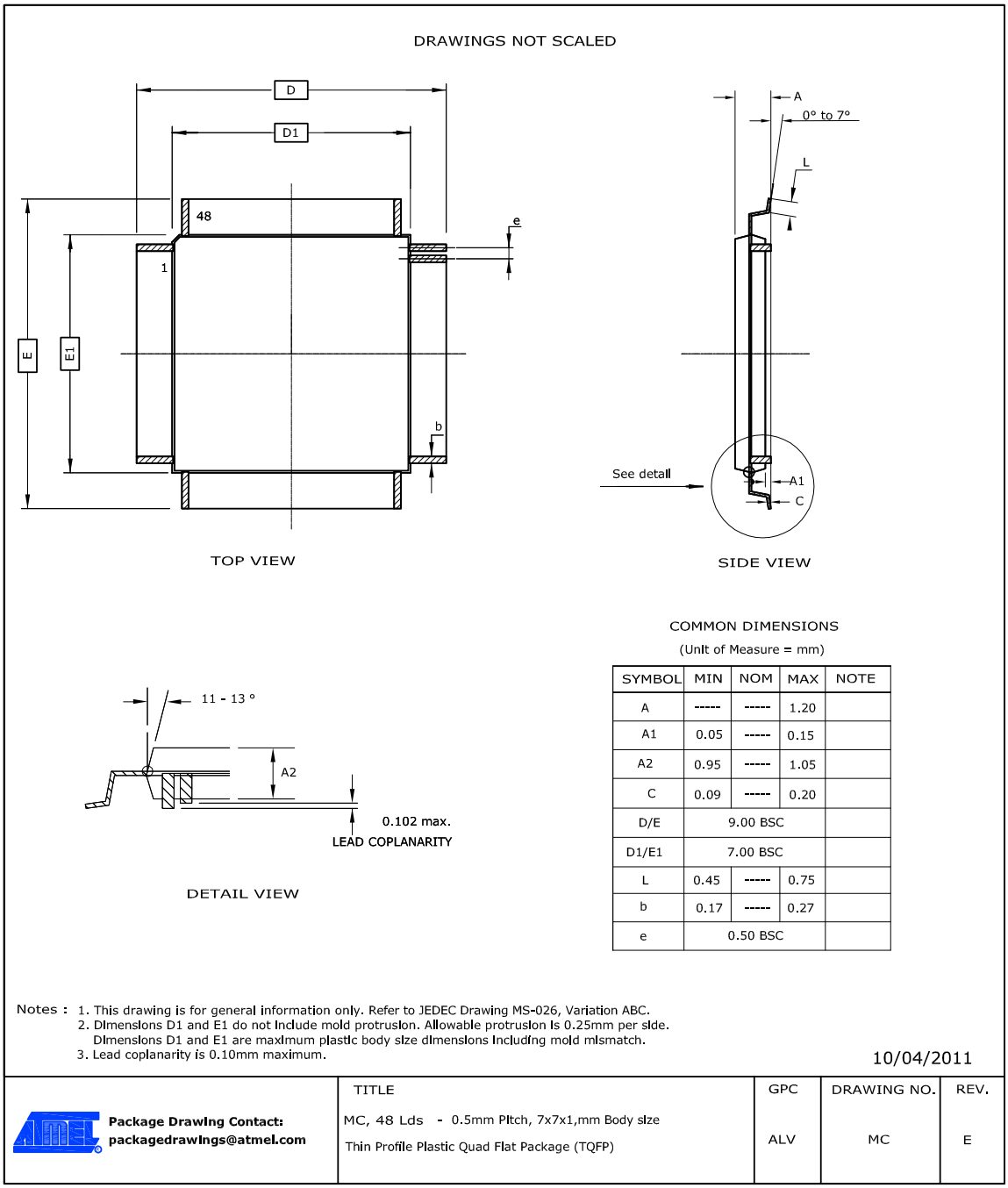
Table 8-9. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 8-10. Package Reference

JEDEC Drawing Reference	MO-220
JESD97 Classification	E8

8.2.4. 48 pin TQFP



COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-----	-----	1.20	
A1	0.05	-----	0.15	
A2	0.95	-----	1.05	
C	0.09	-----	0.20	
D/E		9.00 BSC		
D1/E1		7.00 BSC		
L	0.45	-----	0.75	
b	0.17	-----	0.27	
e		0.50 BSC		

Notes : 1. This drawing is for general information only. Refer to JEDEC Drawing MS-026, Variation ABC.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

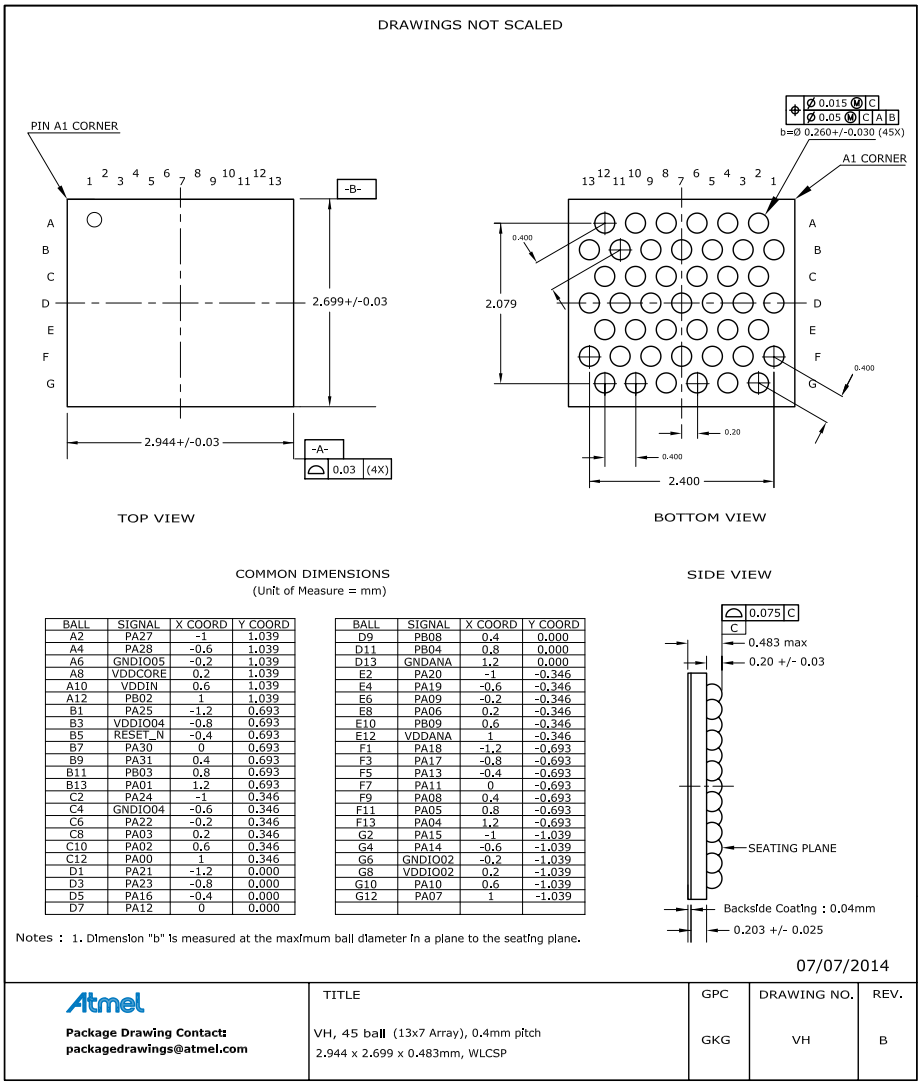
10/04/2011

	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: packagedrawings@atmel.com	MC, 48 Lds - 0.5mm Pitch, 7x7x1,mm Body size Thin Profile Plastic Quad Flat Package (TQFP)	ALV	MC	E

Table 8-16. Package Reference

JEDEC Drawing Reference	MO-220
JESD97 Classification	E3

8.2.6. 45-ball WLCSP



BALL	SIGNAL	X COORD	Y COORD
A2	PA27	-1	1.039
A4	PA28	-0.6	1.039
A6	GNDIO05	-0.2	1.039
A8	VDDCORE	0.2	1.039
A10	VDDIN	0.6	1.039
A12	PB02	1	1.039
B1	PA25	-1.2	0.693
B3	VDDIO04	-0.8	0.693
B5	RESET_N	-0.4	0.693
B7	PA30	0	0.693
B9	PA31	0.4	0.693
B11	PB03	0.8	0.693
B13	PA01	1.2	0.693
C2	PA24	-1	0.346
C4	GNDIO04	-0.6	0.346
C6	PA22	-0.2	0.346
C8	PA03	0.2	0.346
C10	PA02	0.6	0.346
C12	PA00	1	0.346
D1	PA21	-1.2	0.000
D3	PA23	-0.8	0.000
D5	PA16	-0.4	0.000
D7	PA12	0	0.000

BALL	SIGNAL	X COORD	Y COORD
D9	PB08	0.4	0.000
D11	PB04	0.8	0.000
D13	GNDANA	1.2	0.000
E2	PA20	-1	-0.346
E4	PA19	-0.6	-0.346
E6	PA09	-0.2	-0.346
E8	PA06	0.2	-0.346
E10	PB09	0.6	-0.346
E12	VDDANA	1	-0.346
F1	PA18	-1.2	-0.693
F3	PA17	-0.8	-0.693
F5	PA13	-0.4	-0.693
F7	PA11	0	-0.693
F9	PA08	0.4	-0.693
F11	PA05	0.8	-0.693
F13	PA04	1.2	-0.693
G2	PA15	-1	-1.039
G4	PA14	-0.6	-1.039
G6	GNDIO02	-0.2	-1.039
G8	VDDIO02	0.2	-1.039
G10	PA10	0.6	-1.039
G12	PA07	1	-1.039

Table 8-17. Device and Package Maximum Weight

7.3	mg

Table 8-18. Package Characteristics

Moisture Sensitivity Level	MSL1

Table 8-19. Package Reference

JEDEC Drawing Reference	MO-220
JESD97 Classification	E1

8.2.7. 32 pin TQFP

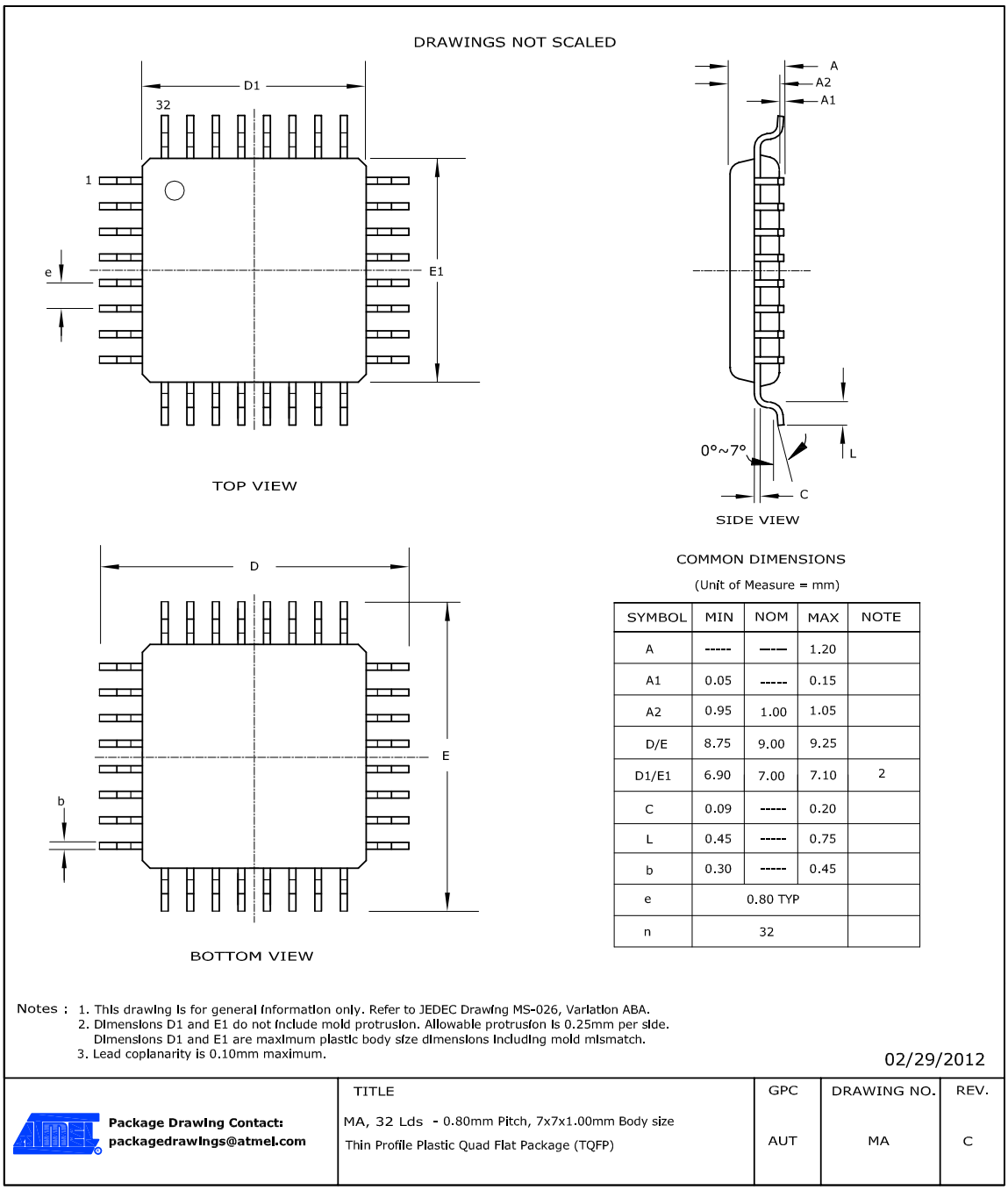


Table 8-20. Device and Package Maximum Weight

100	mg

Table 8-21. Package Charateristics

Moisture Sensitivity Level	MSL3

Table 8-27. Package Characteristics

Moisture Sensitivity Level	MSL1

Table 8-28. Package Reference

JEDEC Drawing Reference	MO-220
JESD97 Classification	E1

8.3. Soldering Profile

The following table gives the recommended soldering profile from J-STD-20.

Table 8-29.

Profile Feature	Green Package
Average Ramp-up Rate (217°C to peak)	3°C/s max.
Preheat Temperature 175°C ±25°C	150-200°C
Time Maintained Above 217°C	60-150s
Time within 5°C of Actual Peak Temperature	30s
Peak Temperature Range	260°C
Ramp-down Rate	6°C/s max.
Time 25°C to Peak Temperature	8 minutes max.

A maximum of three reflow passes is allowed per component.

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