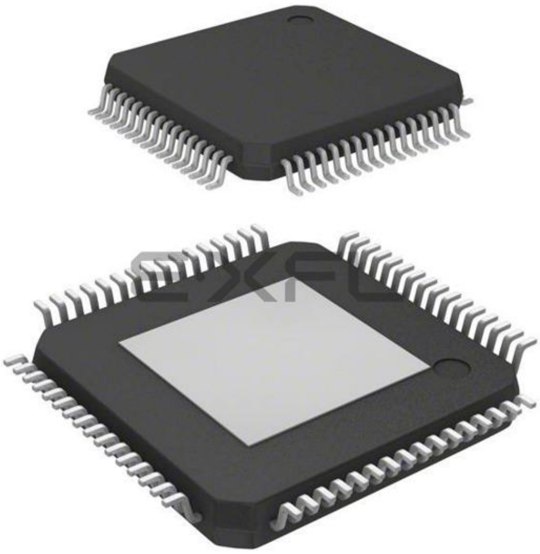
# Microchip Technology - ATSAMD20J14B-AUT Datasheet



## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| **Details** | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0+ |
| Core Size | 32-Bit Single-Core |
| Speed | 48MHz |
| Connectivity | I²C, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, WDT |
| Number of I/O | 52 |
| Program Memory Size | 16KB (16K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 2K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.62V ~ 3.6V |
| Data Converters | A/D 20x12b; D/A 1x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-TQFP Exposed Pad |
| Supplier Device Package | 64-TQFP-EP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/atsamd20j14b-aut |

# Table of Contents

# 1. Description

The Atmel® | SMART™ SAM D20 is a series of low-power microcontrollers using the 32-bit ARM® Cortex®-M0+ processor, and ranging from 32- to 64-pins with up to 256KB Flash and 32KB of SRAM. The SAM D20 devices operate at a maximum frequency of 48MHz and reach 2.46 CoreMark/MHz. They are designed for simple and intuitive migration with identical peripheral modules, hex compatible code, identical linear address map and pin compatible migration paths between all devices in the product series. All devices include intelligent and flexible peripherals, Atmel Event System for inter-peripheral signaling, and support for capacitive touch button, slider and wheel user interfaces.

The SAM D20 devices provide the following features: In-system programmable Flash, eight-channel Event System, programmable interrupt controller, up to 52 programmable I/O pins, 32-bit real-time clock and calendar, up to eight 16-bit Timer/Counters (TC) . The timer/counters can be configured to perform frequency and waveform generation, accurate program execution timing or input capture with time and frequency measurement of digital signals. The TCs can operate in 8- or 16-bit mode, selected TCs can be cascaded to form a 32-bit TC. The series provide up to six Serial Communication Modules (SERCOM) that each can be configured to act as an USART, UART, SPI, $I^2C$ up to 400kHz, up to twenty-channel 350ksps 12-bit ADC with programmable gain and optional oversampling and decimation supporting up to 16-bit resolution, one 10-bit 350ksps DAC, two analog comparators with window mode, Peripheral Touch Controller supporting up to 256 buttons, sliders, wheels and proximity sensing; programmable Watchdog Timer, brown-out detector and power-on reset and two-pin Serial Wire Debug (SWD) program and debug interface.

All devices have accurate and low-power external and internal oscillators. All oscillators can be used as a source for the system clock. Different clock domains can be independently configured to run at different frequencies, enabling power saving by running each peripheral at its optimal clock frequency, and thus maintaining a high CPU frequency while reducing power consumption.

The SAM D20 devices have two software-selectable sleep modes, idle and standby. In idle mode the CPU is stopped while all other functions can be kept running. In standby all clocks and functions are stopped expect those selected to continue running. The device supports SleepWalking. This feature allows the peripheral to wake up from sleep based on predefined conditions, and thus allows the CPU to wake up only when needed, e.g. when a threshold is crossed or a result is ready. The Event System supports synchronous and asynchronous events, allowing peripherals to receive, react to and send events even in standby mode.

The Flash program memory can be reprogrammed in-system through the SWD interface. The same interface can be used for non-intrusive on-chip debug of application code. A boot loader running in the device can use any communication interface to download and upgrade the application program in the Flash memory.

The SAM D20 devices are supported with a full suite of program and system development tools, including C compilers, macro assemblers, program debugger/simulators, programmers and evaluation kits.

## 2. Configuration Summary

| | SAM D20J | SAM D20G | SAM D20E |
|---|---|---|---|
| Pins | 64 | 48 | 32 |
| General Purpose I/O-pins (GPIOs) | 52 | 38 | 26 |
| Flash | 256/128/64/32KB | 256/128/64/32KB | 256/128/64/32KB |
| SRAM | 32/16/8/4/2KB | 32/16/8/4/2KB | 32/16/8/4/2KB |
| Timer Counter (TC) instances | 8 | 6 | 6 |
| Waveform output channels per TC instance | 2 | 2 | 2 |
| Serial Communication Interface (SERCOM) instances | 6 | 6 | 4 |
| Analog-to-Digital Converter (ADC) channels | 20 | 14 | 10 |
| Analog Comparators (AC) | 2 | 2 | 2 |
| Digital-to-Analog Converter (DAC) channels | 1 | 1 | 1 |
| Real-Time Counter (RTC) | Yes | Yes | Yes |
| RTC alarms | 1 | 1 | 1 |
| RTC compare values | One 32-bit value or two 16-bit values | One 32-bit value or two 16-bit values | One 32-bit value or two 16-bit values |
| External Interrupt lines | 16 | 16 | 16 |
| Peripheral Touch Controller (PTC) X and Y lines | 16x16 | 12x10 | 10x6 |
| Maximum CPU frequency | 48MHz | | |
| Packages | QFN<br>TQFP<br>UFBGA | QFN<br>TQFP<br>WLCSP | QFN<br>TQFP |
| Oscillators | 32.768kHz crystal oscillator (XOSC32K)<br>0.4-32MHz crystal oscillator (XOSC)<br>32.768kHz internal oscillator (OSC32K)<br>32KHz ultra-low-power internal oscillator (OSCULP32K)<br>8MHz high-accuracy internal oscillator (OSC8M)<br>48MHz Digital Frequency Locked Loop (DFLL48M) | | |
| Event System channels | 8 | 8 | 8 |
| SW Debug Interface | Yes | Yes | Yes |
| Watchdog Timer (WDT) | Yes | Yes | Yes |

| Ordering Code | FLASH (bytes) | SRAM (bytes) | Package | Carrier Type |
|---|---|---|---|---|
| ATSAMD20E15A-AU | 32K | 4K | TQFP32 | Tray |
| ATSAMD20E15A-AUT | | | | Tape & Reel |
| ATSAMD20E15A-AN | | | | Tray |
| ATSAMD20E15A-ANT | | | | Tape & Reel |
| ATSAMD20E15A-MU | | | QFN32 | Tray |
| ATSAMD20E15A-MUT | | | | Tape & Reel |
| ATSAMD20E15A-MN | | | | Tray |
| ATSAMD20E15A-MNT | | | | Tape & Reel |
| ATSAMD20E16A-AU | 64K | 8K | TQFP32 | Tray |
| ATSAMD20E16A-AUT | | | | Tape & Reel |
| ATSAMD20E16A-AN | | | | Tray |
| ATSAMD20E16A-AFT | | | | Tape & Reel |
| ATSAMD20E16A-MU | | | QFN32 | Tray |
| ATSAMD20E16A-MUT | | | | Tape & Reel |
| ATSAMD20E16A-MN | | | | Tray |
| ATSAMD20E16A-MNT | | | | Tape & Reel |
| ATSAMD20E17A-AU | 128K | 16K | TQFP32 | Tray |
| ATSAMD20E17A-AUT | | | | Tape & Reel |
| ATSAMD20E17A-AN | | | | Tray |
| ATSAMD20E17A-ANT | | | | Tape & Reel |
| ATSAMD20E17A-MU | | | QFN32 | Tray |
| ATSAMD20E17A-MUT | | | | Tape & Reel |
| ATSAMD20E17A-MN | | | | Tray |
| ATSAMD20E17A-MNT | | | | Tape & Reel |
| ATSAMD20E18A-AU | 256K | 32K | TQFP32 | Tray |
| ATSAMD20E18A-AUT | | | | Tape & Reel |
| ATSAMD20E18A-AN | | | | Tray |
| ATSAMD20E18A-AFT | | | | Tape & Reel |
| ATSAMD20E18A-MU | | | QFN32 | Tray |
| ATSAMD20E18A-MUT | | | | Tape & Reel |
| ATSAMD20E18A-MN | | | | Tray |
| ATSAMD20E18A-MNT | | | | Tape & Reel |

| Ordering Code | FLASH (bytes) | SRAM (bytes) | Package | Carrier Type |
|---|---|---|---|---|
| ATSAMD20J15A-AU | 32K | 4K | TQFP64 | Tray |
| ATSAMD20J15A-AUT | | | | Tape & Reel |
| ATSAMD20J15A-AN | | | | Tray |
| ATSAMD20J15A-ANT | | | | Tape & Reel |
| ATSAMD20J15A-MU | | | QFN64 | Tray |
| ATSAMD20J15A-MUT | | | | Tape & Reel |
| ATSAMD20J15A-MN | | | | Tray |
| ATSAMD20J15A-MNT | | | | Tape & Reel |
| ATSAMD20J16A-AU | 64K | 8K | TQFP64 | Tray |
| ATSAMD20J16A-AUT | | | | Tape & Reel |
| ATSAMD20J16A-AN | | | | Tray |
| ATSAMD20J16A-ANT | | | | Tape & Reel |
| ATSAMD20J16A-MU | | | QFN64 | Tray |
| ATSAMD20J16A-MUT | | | | Tape & Reel |
| ATSAMD20J16A-MN | | | | Tray |
| ATSAMD20J16A-MNT | | | | Tape & Reel |
| ATSAMD20J16A-CU | | | UFBGA64 | Tray |
| ATSAMD20J16A-CUT | | | | Tape & Reel |
| ATSAMD20J17A-AU | 128K | 16K | TQFP64 | Tray |
| ATSAMD20J17A-AUT | | | | Tape & Reel |
| ATSAMD20J17A-AN | | | | Tray |
| ATSAMD20J17A-ANT | | | | Tape & Reel |
| ATSAMD20J17A-MU | | | QFN64 | Tray |
| ATSAMD20J17A-MUT | | | | Tape & Reel |
| ATSAMD20J17A-MN | | | | Tray |
| ATSAMD20J17A-MNT | | | | Tape & Reel |
| ATSAMD20J17A-CU | | | UFBGA64 | Tray |
| ATSAMD20J17A-CUT | | | | Tape & Reel |

| Ordering Code | FLASH (bytes) | SRAM (bytes) | Package | Carrier Type |
|---|---|---|---|---|
| ATSAMD20J18A-AU | 256K | 32K | TQFP64 | Tray |
| ATSAMD20J18A-AUT | | | | Tape & Reel |
| ATSAMD20J18A-AN | | | | Tray |
| ATSAMD20J18A-ANT | | | | Tape & Reel |
| ATSAMD20J18A-MU | | | QFN64 | Tray |
| ATSAMD20J18A-MUT | | | | Tape & Reel |
| ATSAMD20J18A-MN | | | | Tray |
| ATSAMD20J18A-MNT | | | | Tape & Reel |
| ATSAMD20J18A-CU | | | UFBGA64 | Tray |
| ATSAMD20J18A-CUT | | | | Tape & Reel |

## 3.4. Device Identification

The DSU - Device Service Unit peripheral provides the Device Selection bits in the Device Identification register (DID.DEVSEL) in order to identify the device by software. The device variants have a reset value of DID=0x1001drxx, with the LSB identifying the die number ('d'), the die revision ('r') and the device selection ('xx').

**Table 3-1. Device Identification Values**

| Device Variant | DID.DEVSEL | Device ID (DID) |
|---|---|---|
| SAMD20J18C | 0x00 | 0x10001300 |
| SAMD20J18A | 0x00 | 0x10001300 |
| SAMD20J17A | 0x01 | 0x10001301 |
| SAMD20J16A | 0x02 | 0x10001302 |
| SAMD20J15A | 0x03 | 0x10001303 |
| SAMD20J14A | 0x04 | 0x10001304 |
| SAMD20G18A | 0x05 | 0x10001305 |
| SAMD20G17A | 0x06 | 0x10001306 |
| SAMD20G16A | 0x07 | 0x10001307 |
| SAMD20G15A | 0x08 | 0x10001308 |
| SAMD20G14A | 0x09 | 0x10001309 |
| SAMD20E18A | 0x0A | 0x1000130A |
| SAMD20E17A | 0x0B | 0x1000130B |
| SAMD20E16A | 0x0C | 0x1000130C |
| SAMD20E15A | 0x0D | 0x1000130D |

## 5.2. SAM D20G

### 5.2.1. QFN48 / TQFP48

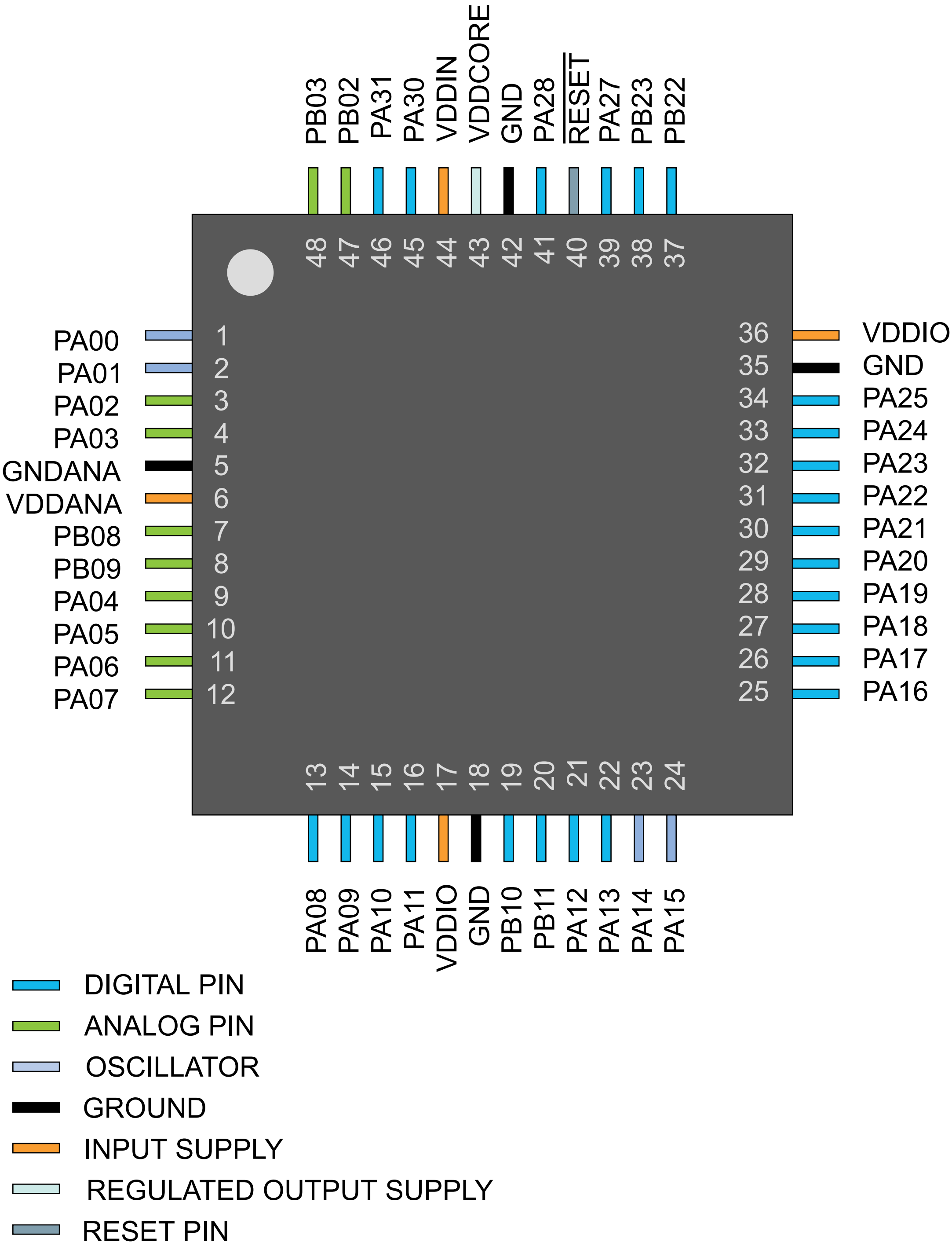
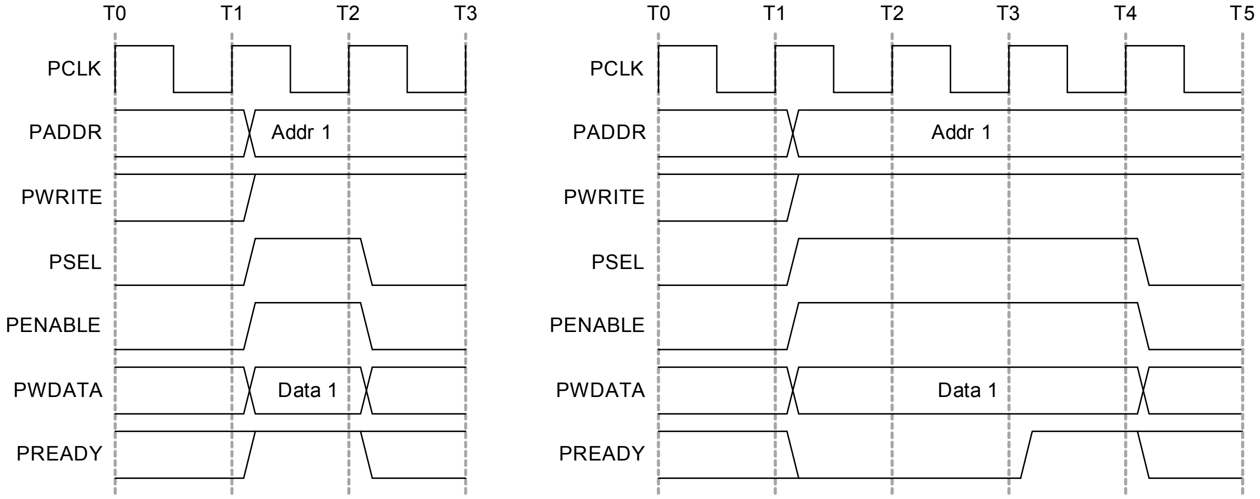


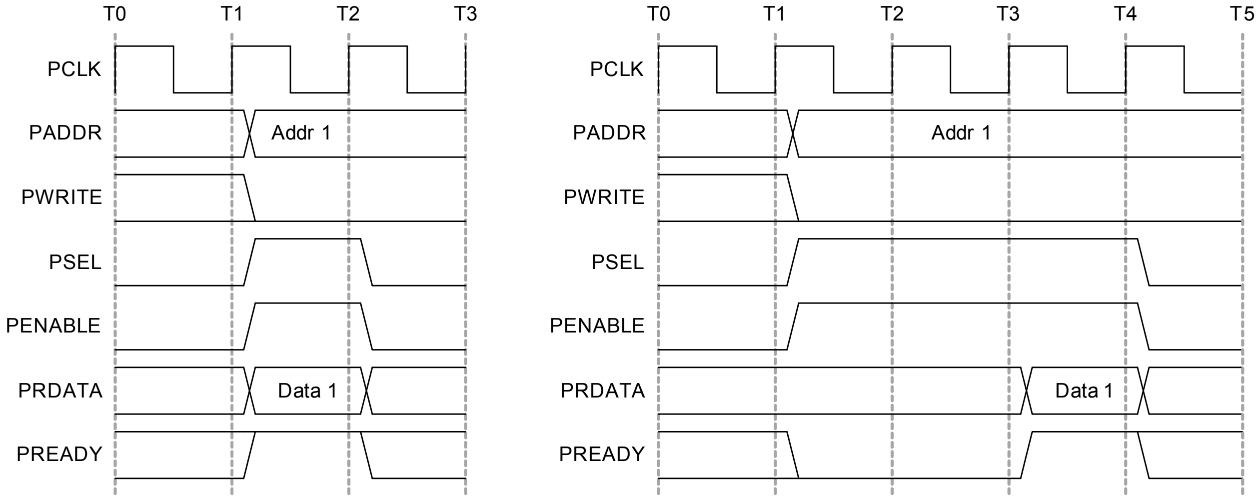
**Figure 7-1. APB Write Access.**



No wait states

Wait states

**Figure 7-2. APB Read Access.**



No wait states

Wait states

**Related Links**

Product Mapping on page 19

## 7.6. PAC - Peripheral Access Controller

### 7.6.1. Overview

There is one PAC associated with each AHB-APB bridge. The PAC can provide write protection for registers of each peripheral connected on the same bridge.

The PAC peripheral bus clock (CLK_PACx_APB) can be enabled and disabled in the Power Manager. CLK_PAC0_APB and CLK_PAC1_APB are enabled are reset. CLK_PAC2_APB is disabled at reset. Refer to *PM – Power Manager* for details. The PAC will continue to operate in any sleep mode where the selected clock source is running. Write-protection does not apply for debugger access. When the debugger makes an access to a peripheral, write-protection is ignored so that the debugger can update the register.

| Value | Description |
|---|---|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

**Bit 3 – GCLK**
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|---|---|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

**Bit 2 – SYSCTRL**
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|---|---|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

**Bit 1 – PM**
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|---|---|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

### 7.7.1.2. Write Protect Set

**Name:** WPSET
**Offset:** 0x04
**Reset:** 0x000000
**Property:** –

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | |
| Access | | | | | | | | |
| Reset | | | | | | | | |

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | |
| Access | | | | | | | | |
| Reset | | | | | | | | |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | |
| Access | | | | | | | | |
| Reset | | | | | | | | |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | | EIC | RTC | WDT | GCLK | SYSCTRL | PM | |
| Access | | R/W | R/W | R/W | R/W | R/W | R/W | |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | |

**Bit 6 – EIC**
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|---|---|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

**Bit 5 – RTC**
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|---|---|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

**Bit 4 – WDT**
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|---|---|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

**Bit 3 – GCLK**
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|---|---|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

**Bit 2 – SYSCTRL**
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|---|---|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

**Bit 1 – PM**
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|---|---|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

### 7.7.2. PAC1 Register Description

| Value | Description |
|---|---|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

**Bit 1 – DSU**
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|---|---|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

### 7.7.3.1. Write Protect Clear

**Name:** WPCLR
**Offset:** 0x00
**Reset:** 0x00800000
**Property:** –

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | |
| Access | | | | | | | | |
| Reset | | | | | | | | |

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| | | | | | PTC | DAC | AC | ADC |
| Access | | | | | R/W | R/W | R/W | R/W |
| Reset | | | | | 0 | 0 | 0 | 0 |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| | TC7 | TC6 | TC5 | TC4 | TC3 | TC2 | TC1 | TC0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | SERCOM5 | SERCOM4 | SERCOM3 | SERCOM2 | SERCOM1 | SERCOM0 | EVSYS | |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

**Bit 19 – PTC**
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|---|---|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

**Bit 18 – DAC**
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|---|---|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

**Bit 17 – AC**
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|---|---|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

**Bit 16 – ADC**
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|---|---|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

**Bits 15,14,13,12,11,10,9,8 – TCx**
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|---|---|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

**Bits 7,6,5,4,3,2 – SERCOMx**
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|---|---|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

**Bit 1 – EVSYS**
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|---|---|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

# 8. Packaging Information

## 8.1. Thermal Considerations

**Related Links**

Junction Temperature on page 39

### 8.1.1. Thermal Resistance Data

The following *table* summarizes the thermal resistance data depending on the package.

**Table 8-1. Thermal Resistance Data**

| Package Type | $\theta_{JA}$ | $\theta_{JC}$ |
|---|---|---|
| 32-pin TQFP | 68.0°C/W | 25.8°C/W |
| 48-pin TQFP | 78.8°C/W | 12.3°C/W |
| 64-pin TQFP | 66.7°C/W | 11.9°C/W |
| 32-pin QFN | 37.2°C/W | 13.1°C/W |
| 48-pin QFN | 33.0°C/W | 11.4°C/W |
| 64-pin QFN | 33.5°C/W | 11.2°C/W |
| 64-ball UFBGA | 67.4°C/W | 12.4°C/W |
| 45-ball WLCSP | 37.0°C/W | 0.36°C/W |

### 8.1.2. Junction Temperature

The average chip-junction temperature, $T_J$, in °C can be obtained from the following:

1. $T_J = T_A + (P_D \times \theta_{JA})$
2. $T_J = T_A + (P_D \times (\theta_{HEATSINK} + \theta_{JC}))$

where:

- $\theta_{JA}$ = Package thermal resistance, Junction-to-ambient (°C/W), see Thermal Resistance Data
- $\theta_{JC}$ = Package thermal resistance, Junction-to-case thermal resistance (°C/W), see Thermal Resistance Data
- $\theta_{HEATSINK}$ = Thermal resistance (°C/W) specification of the external cooling device
- $P_D$ = Device power consumption (W)
- $T_A$ = Ambient temperature (°C)

From the first equation, the user can derive the estimated lifetime of the chip and decide if a cooling device is necessary or not. If a cooling device is to be fitted on the chip, the second equation should be used to compute the resulting average chip-junction temperature $T_J$ in °C.

**Related Links**

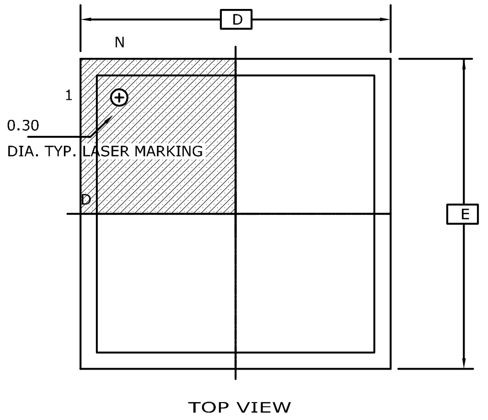
Thermal Considerations on page 39

**Table 8-4. Package Reference**

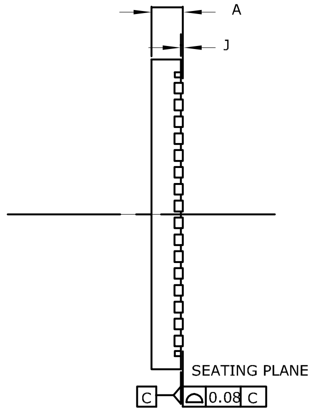
| | |
|---|---|
| JEDEC Drawing Reference | MS-026 |
| JESD97 Classification | E3 |

### 8.2.2. 64 pin QFN

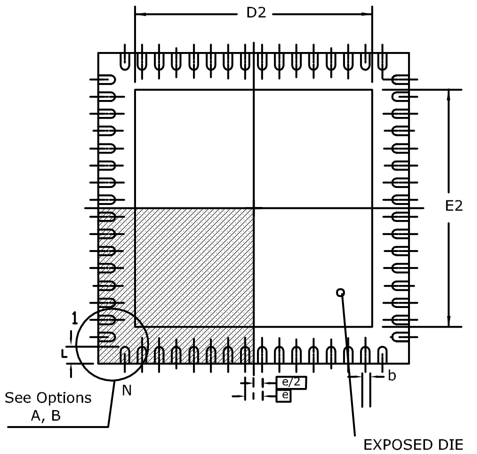
DRAWINGS NOT SCALED



TOP VIEW



SIDE VIEW

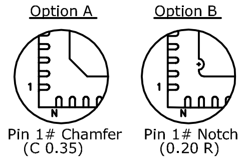


BOTTOM VIEW

COMMON DIMENSIONS

(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | 0.80 | ----- | 1.00 | |
| D/E | | 9.00 BSC | | |
| D2/E2 | 4.60 | 4.70 | 4.80 | |
| J | 0.00 | ----- | 0.05 | |
| b | 0.15 | 0.20 | 0.25 | |
| e | | 0.50 BSC | | |
| L | 0.30 | 0.40 | 0.55 | |
| N | | 64 | | |



Pin 1# Chamfer (C 0.35)

Pin 1# Notch (0.20 R)

Notes :
1. This drawing is for general information only. Refer to JEDEC Drawing MO-220, Variation VMMD-4, for proper dimensions, tolerances, datums, etc.
2. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optical radius on the other end of the terminal, the dimension should not be measured in that radius area.

05/27/2011

| | TITLE | GPC | DRAWING NO. | REV. |
|---|---|---|---|---|
| **Package Drawing Contact:**<br>**packagedrawings@atmel.com** | PA, 64 Leads , 0.50 mm pitch, 9 x 9 x 1 mm<br>Very Thin Quad Flat No Lead Package (VQFN) Sawn | ZST | PA | A |

**Note:** The exposed die attach pad is not connected electrically inside the device.

**Table 8-9. Package Characteristics**

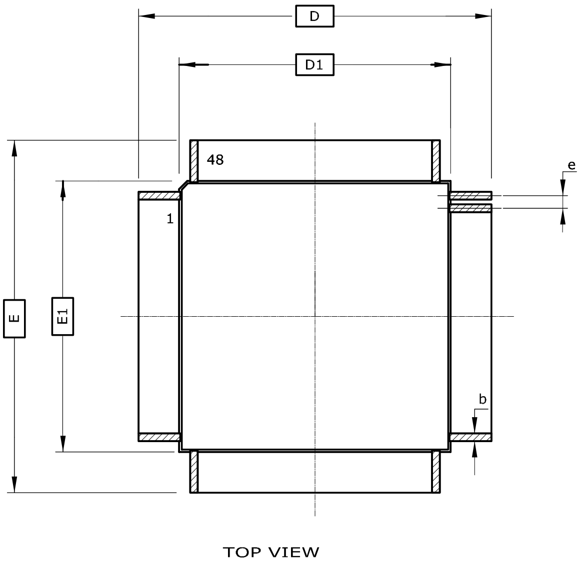
| | |
|---|---|
| Moisture Sensitivity Level | MSL3 |

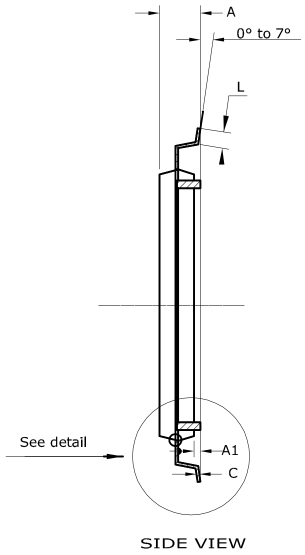
**Table 8-10. Package Reference**

| | |
|---|---|
| JEDEC Drawing Reference | MO-220 |
| JESD97 Classification | E8 |

### 8.2.4. 48 pin TQFP

DRAWINGS NOT SCALED

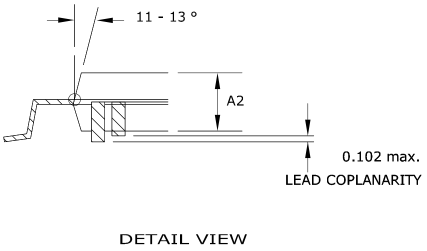




COMMON DIMENSIONS

(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | ----- | ----- | 1.20 | |
| A1 | 0.05 | ----- | 0.15 | |
| A2 | 0.95 | ----- | 1.05 | |
| C | 0.09 | ----- | 0.20 | |
| D/E | | 9.00 BSC | | |
| D1/E1 | | 7.00 BSC | | |
| L | 0.45 | ----- | 0.75 | |
| b | 0.17 | ----- | 0.27 | |
| e | | 0.50 BSC | | |



Notes :
1. This drawing is for general information only. Refer to JEDEC Drawing MS-026, Variation ABC.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

10/04/2011

| | TITLE | GPC | DRAWING NO. | REV. |
|---|---|---|---|---|
| **Package Drawing Contact:**<br>**packagedrawings@atmel.com** | MC, 48 Lds - 0.5mm Pitch, 7x7x1,mm Body size<br>Thin Profile Plastic Quad Flat Package (TQFP) | ALV | MC | E |

Table 8-11. Device and Package Maximum Weight

| | |
|---|---|
| 140 | mg |

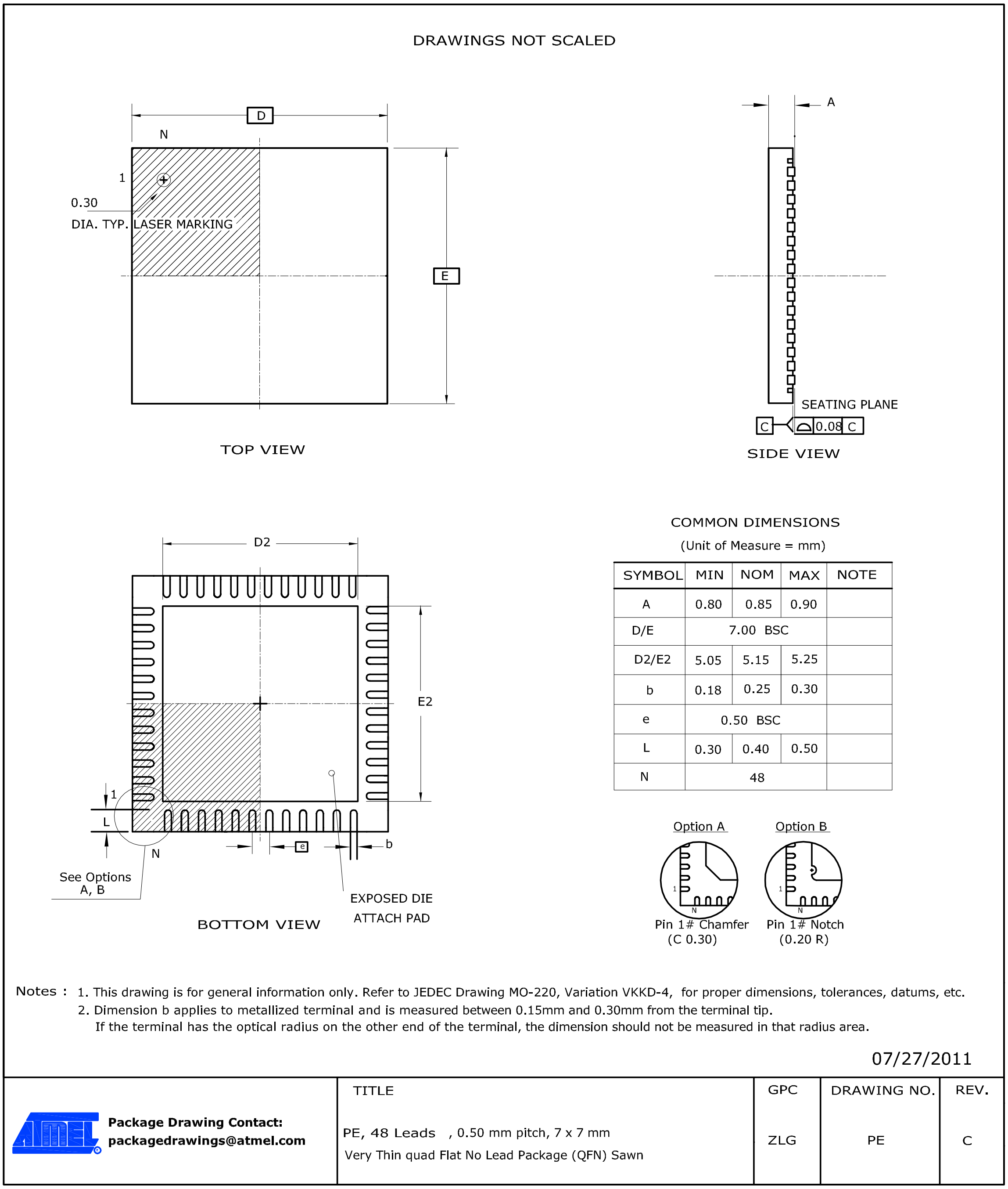
Table 8-12. Package Characteristics

| | |
|---|---|
| Moisture Sensitivity Level | MSL3 |

Table 8-13. Package Reference

| | |
|---|---|
| JEDEC Drawing Reference | MS-026 |
| JESD97 Classification | E3 |

### 8.2.5. 48 pin QFN



COMMON DIMENSIONS

(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | 0.80 | 0.85 | 0.90 | |
| D/E | | 7.00 BSC | | |
| D2/E2 | 5.05 | 5.15 | 5.25 | |
| b | 0.18 | 0.25 | 0.30 | |
| e | | 0.50 BSC | | |
| L | 0.30 | 0.40 | 0.50 | |
| N | | 48 | | |

Notes : 1. This drawing is for general information only. Refer to JEDEC Drawing MO-220, Variation VKKD-4, for proper dimensions, tolerances, datums, etc.
2. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
If the terminal has the optical radius on the other end of the terminal, the dimension should not be measured in that radius area.

07/27/2011

**Package Drawing Contact:**
**packagedrawings@atmel.com**

| TITLE | GPC | DRAWING NO. | REV. |
|---|---|---|---|
| PE, 48 Leads , 0.50 mm pitch, 7 x 7 mm<br>Very Thin quad Flat No Lead Package (QFN) Sawn | ZLG | PE | C |

**Note:** The exposed die attach pad is not connected electrically inside the device.

**Table 8-14. Device and Package Maximum Weight**

| | |
|---|---|
| 140 | mg |

**Table 8-15. Package Characteristics**

| | |
|---|---|
| Moisture Sensitivity Level | MSL3 |

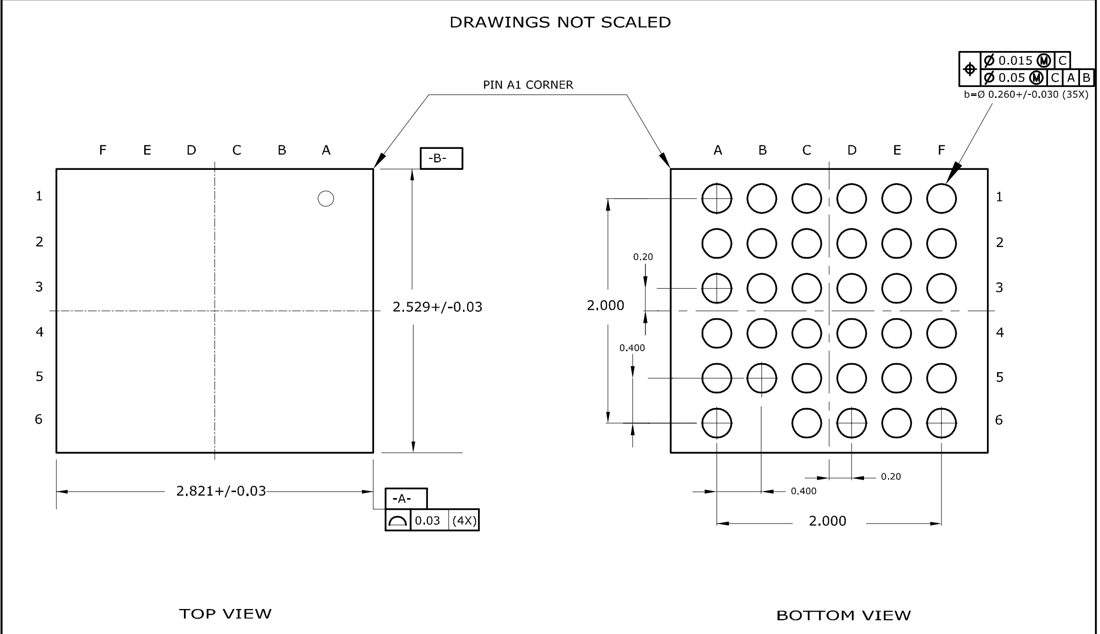
**Table 8-24. Package Characteristics**

| | |
|---|---|
| Moisture Sensitivity Level | MSL3 |

**Table 8-25. Package Reference**

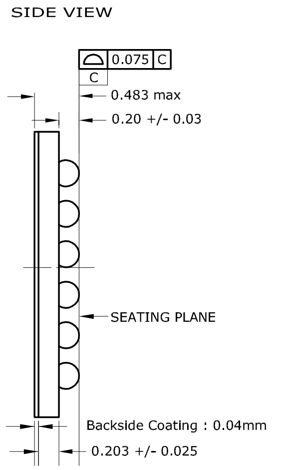
| | |
|---|---|
| JEDEC Drawing Reference | MO-220 |
| JESD97 Classification | E3 |

### 8.2.9. 35 ball WLCSP



COMMON DIMENSIONS
(Unit of Measure = mm)

| BALL | SIGNAL | X COORD | Y COORD |
|---|---|---|---|
| A1 | PA00 | 1 | -1 |
| A2 | PA01 | 0.6 | -0.6 |
| A3 | GNDANA | 0.2 | -0.2 |
| A4 | VDDANA | -0.2 | 0.2 |
| A5 | PA06 | 1 | 0.4 |
| A6 | VDDIO | 1 | 1 |
| B1 | PA30 | 0.6 | -1 |
| B2 | PA31 | 0.2 | -0.6 |
| B3 | PA02 | -0.2 | -0.2 |
| B4 | PA04 | 1 | 0.2 |
| B5 | PA07 | 1 | 0.4 |
| B6 | NO BALL | | |
| C1 | VDDCORE | 0.2 | -1 |
| C2 | VDDIO | -0.2 | -0.6 |
| C3 | PA03 | 1 | -0.2 |
| C4 | PA05 | 1 | 0.2 |
| C5 | PA08 | 0.6 | 0.4 |
| C6 | PA10 | 0.2 | 1 |
| D1 | GND | -0.2 | -1 |
| D2 | PA28 | 1 | -0.6 |
| D3 | GND | 1 | -0.2 |
| D4 | PA11 | 0.6 | 0.2 |
| D5 | PA09 | 0.2 | 0.4 |
| D6 | GND | -0.2 | 1 |
| E1 | RESET_N | 1 | -1 |
| E2 | PA27 | 1 | -0.6 |
| E3 | PA22 | 0.6 | -0.2 |
| E4 | PA17 | 0.2 | 0.2 |
| E5 | PA16 | -0.2 | 0.4 |
| E6 | PA14 | 1 | 1 |
| F1 | PA25 | 1 | -1 |
| F2 | PA24 | 0.6 | -0.6 |
| F3 | PA23 | 0.2 | -0.2 |
| F4 | PA19 | -0.2 | 0.2 |
| F5 | PA18 | 1 | 0.4 |
| F6 | PA15 | 1 | 1 |



Notes : 1. Dimension "b" is measured at the maximum ball diameter in a plane to the seating plane.

01/07/2016

| Atmel | TITLE | GPC | DRAWING NO. | REV. |
|---|---|---|---|---|
| **Package Drawing Contact:**<br>**packagedrawings@atmel.com** | 35 ball - (6X6 Array), 0.4mm pitch<br>2.821 x 2.529 x 0.483mm, WLCSP | GJR | VJ | B |

**Table 8-26. Device and Package Maximum Weight**

| | |
|---|---|
| 6.2 | mg |